



Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT3805/A

FEATURES:

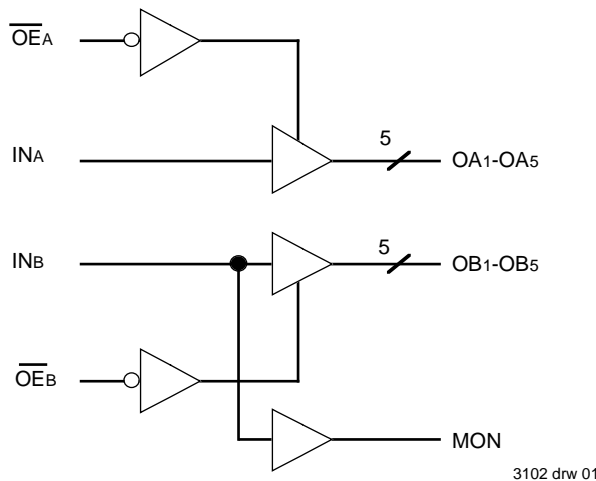
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 1.0ns (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- 'Heartbeat' monitor output
- Available in DIP, SOIC, SSOP, QSOP, Cerpack and LCC packages
- Military product compliant to MIL-STD-883, Class B
- $V_{CC} = 3.3V \pm 0.3V$

DESCRIPTION:

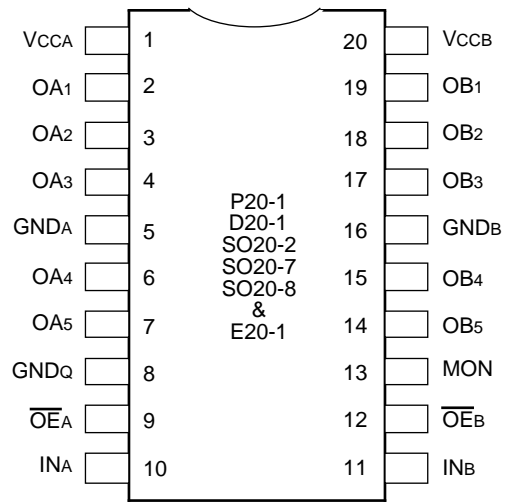
The FCT3805/A is a 3.3 volt, non-inverting clock driver built using advanced dual metal CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The FCT3805/A offers low capacitance inputs with hysteresis.

The FCT3805/A is designed for high speed clock distribution where signal quality and skew are critical. The FCT 3805 also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

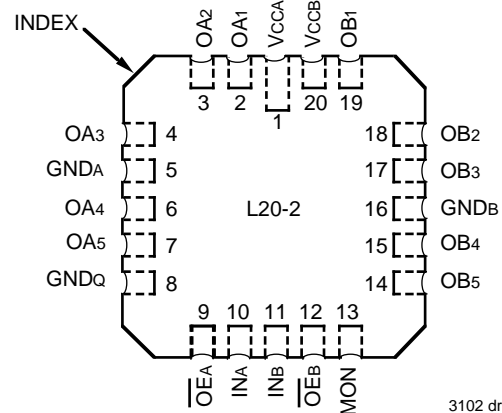
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

OCTOBER 1995

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A, \overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OAn, OBn	Clock Outputs
MON	Monitor Output

3102 tbl 01

FUNCTION TABLE⁽¹⁾

Inputs		Outputs	
$\overline{OE}_A, \overline{OE}_B$	INA, INB	OAn, OBn	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE:

1. H = HIGH, L = LOW, Z = High Impedance

3102 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	-0.5 to Vcc + 0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	-60 to +60	mA

3102 Ink 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- Input terminals.
- Output and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	5.0	pF
COUT	Output Capacitance	VOUT = 0V	3.5	5.0	pF

3102 Ink 04

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2.0	—	5.5	V	
	Input HIGH Level (I/O pins)		2.0	—	$V_{CC}+0.5$		
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V	
I_{IH}	Input HIGH Current (Input pins) ⁽⁶⁾	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁶⁾		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁶⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁶⁾		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁶⁾	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V	
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$	-36	-60	-110	mA	
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$	50	90	200	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	—	—	V
			$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4 ⁽⁵⁾	3.0	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
			$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.50	
I_{OFF}	Input Power Off Leakage ⁽⁶⁾	$V_{CC} = 0\text{V}, V_{IN} \leq 4.5\text{V}$	—	—	± 1	μA	
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$	-60	-135	-240	mA	
V_H	Input Hysteresis	—	—	150	—	mV	
I_{CCL}	Quiescent Power Supply Current	$V_{CC} = \text{Max.},$ $V_{IN} = \text{GND}$ or V_{CC}	COM'L.	—	0.1	10	μA
I_{CCH}			MIL.	—	0.1	100	
I_{CCZ}							

NOTES:

3102 Ink 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}, +25^\circ\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^{(3)}$		—	2.0	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Per Output Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.035	0.06	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_o = 25\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = V_{CC}$ Mon. Output Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.9	1.6	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.9	1.6	
		$V_{CC} = \text{Max.}$ Outputs Open $f_o = 50\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Eleven Outputs Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	20.0	33.0 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	20.0	33.0 ⁽⁵⁾	

NOTES:

3102 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = V_{CC} - 0.6V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (f_o \text{No})$
 $I_{CC} = \text{Quiescent Current (Iccl, Icch and Iccz)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (VIN = Vcc - 0.6V)}$
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$
 $\text{NT} = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_o = \text{Output Frequency}$
 $\text{No} = \text{Number of Outputs at } f_o$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE^(3,4)

Symbol	Parameter	Condition ⁽¹⁾	FCT3805				FCT3805A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	5.8			1.5	5.0			ns
tPHL	INA to OAn, INB to OBn										
tR	Output Rise Time		—	2.0	—		—	2.0	—		ns
tF	Output Fall Time		—	2.0	—		—	2.0	—		ns
tsk(o)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—		—	0.5	—		ns
tsk(p)	Pulse skew: skew between opposite transitions of same output (tPHL-tPLH)		—	1.2	—		—	1.0	—		ns
tsk(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—		—	1.2	—		ns
tPZL	Output Enable Time		1.5	6.5			1.5	6.0			ns
tPZH	OE _A to OAn, OE _B to OBn										
tPLZ	Output Disable Time	1.5	5.5			1.5	5.0			ns	
tPHZ	OE _A to OAn, OE _B to OBn										

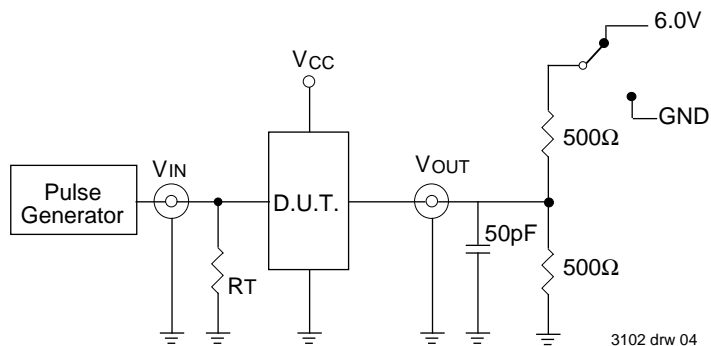
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. tPLH, tPHL, tsk(t) production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to Vcc, operating temperature and process parameters. These propagation delay limits do not imply skew.

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR ALL OUTPUTS



ENABLE AND DISABLE TIME SWITCH POSITION

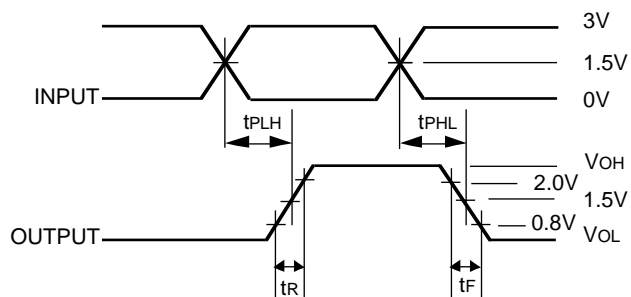
Test	Switch
Disable LOW Enable LOW	6.0V
Disable HIGH Enable HIGH	GND

DEFINITIONS:

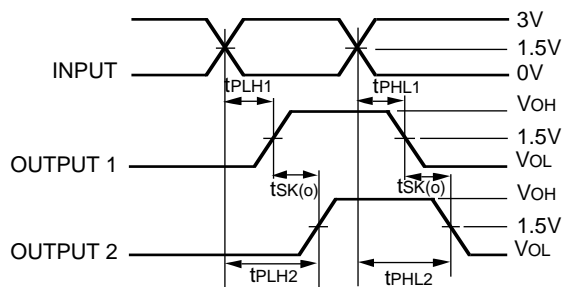
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

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PACKAGE DELAY

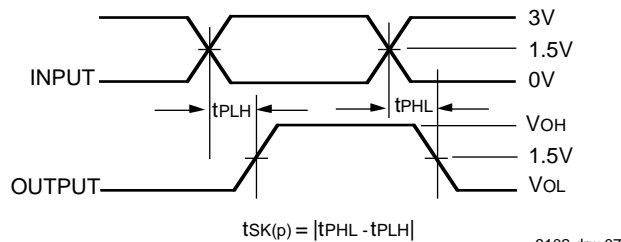


OUTPUT SKEW- tsk(o)

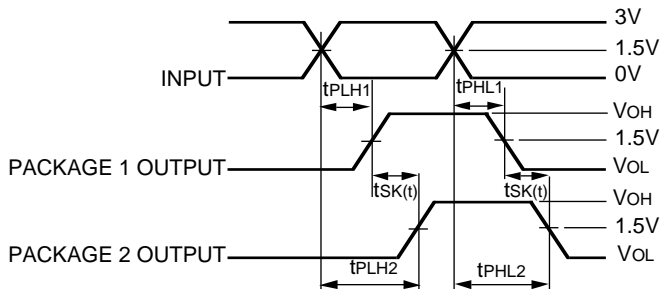


$$t_{SK(o)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

PULSE SKEW- tsk(p)

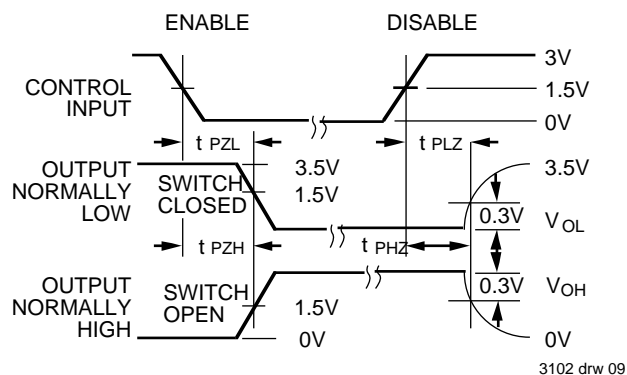


PACKAGE SKEW- tsk(t)



$$t_{SK(t)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

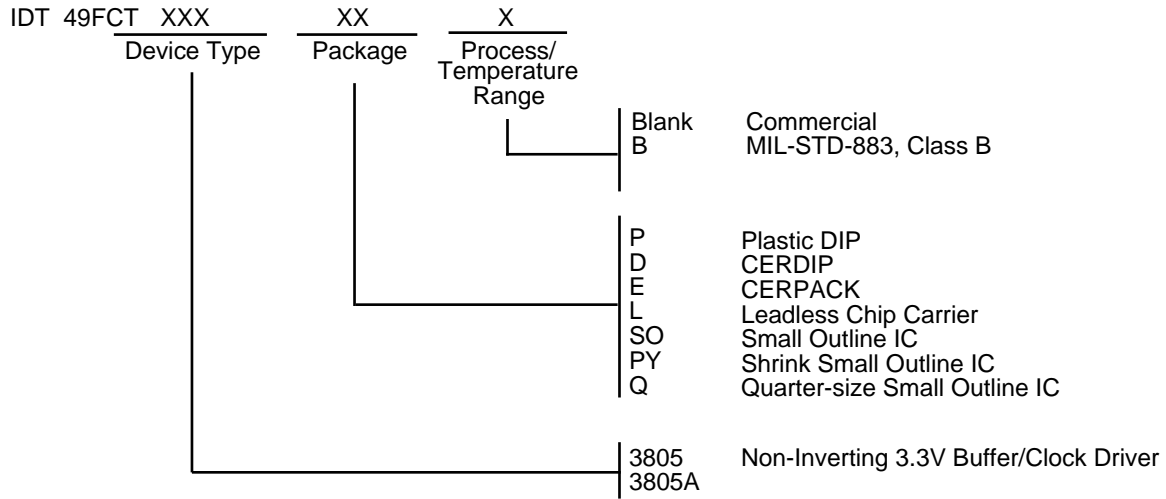
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: $f \leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

ORDERING INFORMATION



3102 drw 10