Data Sheet July 2000 File Number 3019.4

Microprocessor-Compatible, Real-Time Clock

The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Intersil's silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from $^1/_{100}$ seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{ACC}) of 300ns eliminates the need for wait states or software overhead with most microprocessors. Furthermore, an ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts, periodic and alarm. The periodic interrupt (100Hz, 10Hz, etc.) can be programmed by the internal interrupt control register to provide 6 different output signals. The alarm interrupt is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power Down Detector eliminates the need for external components to support the battery back-up function. When a power down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

Features

- 8-Bit, µP Bus Compatible
  - Multiplexed or Direct Addressing
- Regulated Oscillator Supply Ensures Frequency Stability and Low Power
- Time From 1/100 Seconds to 99 Years
- Software Selectable 12/24 Hour Format
- Latched Time Data Ensures No Roll Over During Read
- Full Calendar with Automatic Leap Year Correction
- On-Chip Battery Backup Switchover Circuit
- Access Time Less than 300ns
- 4 Programmable Crystal Oscillator Frequencies Over Industrial Temperature Range
- 3 Programmable Crystal Oscillator Frequencies Over Military Temperature Range
- On-Chip Alarm Comparator and RAM
- Interrupts from Alarm and 6 Selectable Periodic Intervals
- Standby Micro-Power Operation: 1.2µA Typical at 3.0V and 32kHz Crystal

Applications

- Portable and Personal Computers
- Data Logging
- Industrial Control Systems
- Point Of Sale

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

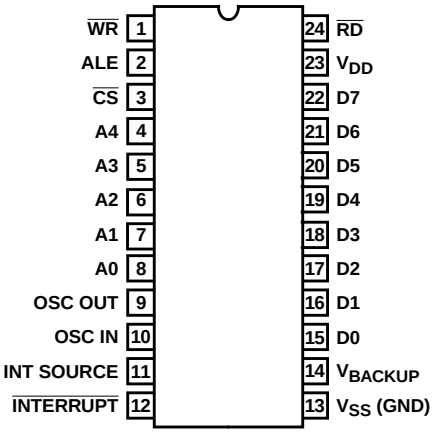
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ICM7170IPG	-40 to 85	24 Ld PDIP	E24.6
ICM7170IDG	-40 to 85	24 Ld SBDIP	D24.6
ICM7170IBG	-40 to 85	24 Ld SOIC	M24.3
ICM7170AIPG	-40 to 85	24 Ld PDIP	E24.6
ICM7170AIBG	-40 to 85	24 Ld SOIC	M24.3

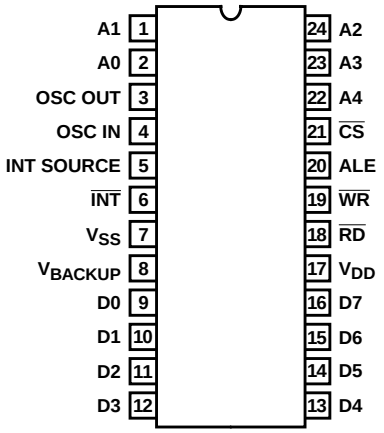
NOTE: "A" Parts Screened to <5µA I_{STBY} at 32kHz.

Pinouts

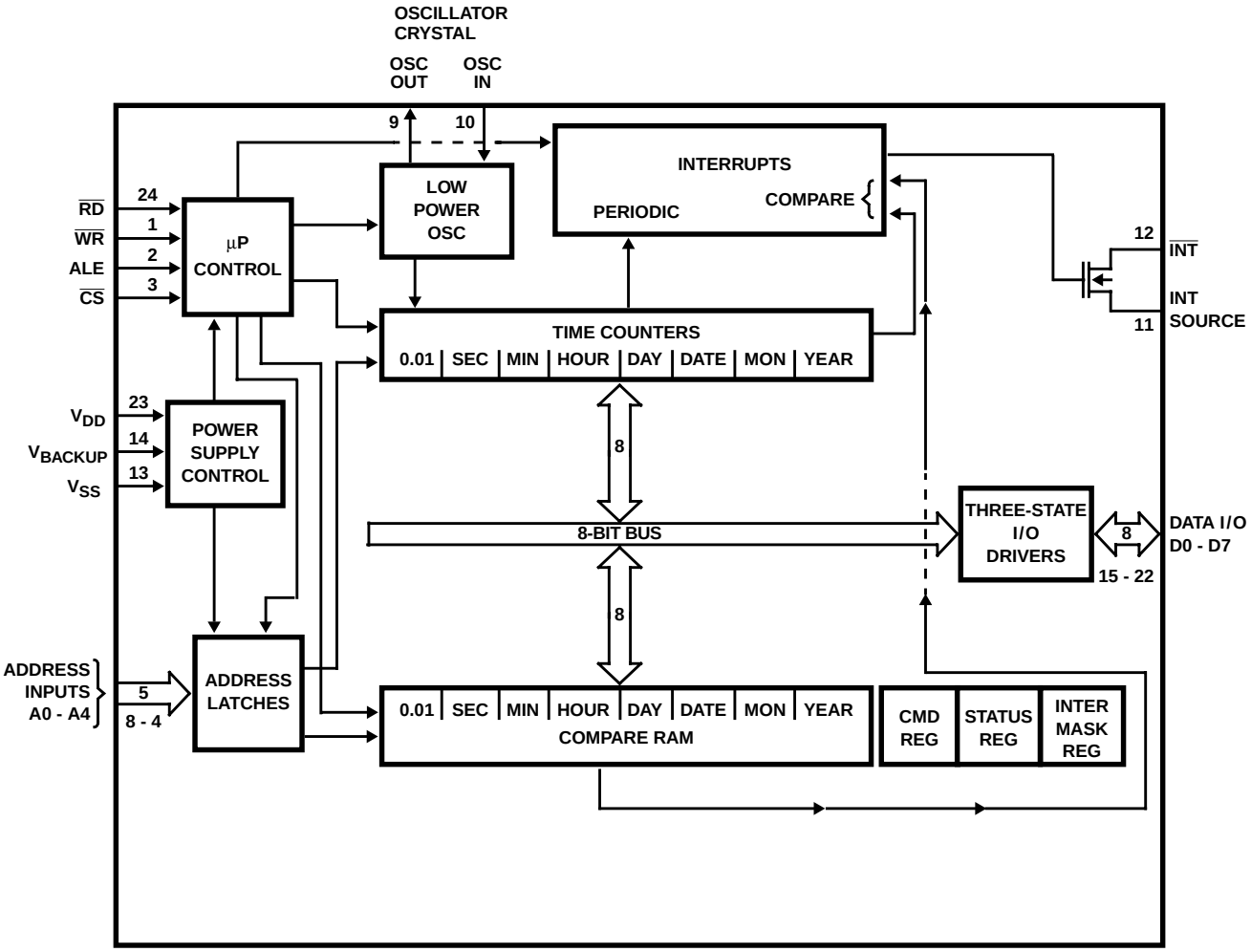
ICM7170
(PDIP, SBDIP)
TOP VIEW



ICM7170
(SOIC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage . . . . . +8.0V
Power Dissipation (Note 1) 500mW
Storage Temperature Range . . . . . -65^oC to 150^oC
Lead Temperature (Soldering 10s) . . . . . 300^oC
Input Voltage (Any Terminal) (Note 2) . . . . V_{DD} +0.3V to V_{SS} -0.3V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	50	N/A
SBDIP Package	75	30
SOIC Package	75	N/A

Maximum Junction Temperature
Plastic Package . . . . . 150^oC
SBDIP Package . . . . . 175^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

Electrical Specifications

$T_A = -40^oC$ to 85^oC, V_{DD} +5V ±10%, V_{BACKUP} V_{DD}, V_{SS} = 0V Unless Otherwise Specified
All I_{DD} specifications include all input and output leakages (ICM7170 and ICM7170A)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Supply Range, V_{DD}	f_{OSC} = 32kHz		1.9	-	5.5	V
	f_{OSC} = 1, 2, 4MHz		2.6	-	5.5	V
Standby Current, $I_{STBY(1)}$	f_{OSC} = 32kHz Pins 1 - 8,15 - 22 and 24 = V_{DD}	ICM7170	-	1.2	20.0	µA
	$V_{DD} = V_{SS}$; $V_{BACKUP} = V_{DD}$ - 3.0V For ICM7170A See General Notes 5	ICM7170A	-	1.2	5.0	µA
Standby Current, $I_{STBY}(2)$	f_{OSC} = 4MHz Pins 1 - 8,15 - 22 and 24 = V_{DD} $V_{DD} = V_{SS}$; $V_{BACKUP} = V_{DD}$ - 3.0V		-	20	150	µA
Operating Supply Current, $I_{DD(1)}$	f_{OSC} = 32kHz, Read/Write Operation at 100Hz		-	0.3	1.2	mA
Operating Supply Current, $I_{DD(2)}$	f_{OSC} = 32kHz, Read/Write Operation at 1MHz		-	1.0	2.0	mA
Input Low Voltage (Except Osc.), V_{IL}	V_{DD} = 5.0V		-	-	0.8	V
Input High Voltage (Except Osc.), V_{IH}	V_{DD} = 5.0V		2.4	-	-	V
Output Low Voltage (Except Osc.), V_{OL}	I_{OL} = 1.6mA		-	-	0.4	V
Output High Voltage Except $\overline{\text{INTERRUPT}}$ (Except Osc.), V_{OH}	I_{OH} = -400µA		2.4	-	-	V
Input Leakage Current, I_{IL}	$V_{IN} = V_{DD}$ or V_{SS}		-10	0.5	+10	µA
Three-State Leakage Current (D0 - D7), $I_{OL}(1)$	$V_O = V_{DD}$ or V_{SS}		-10	0.5	+10	µA
Backup Battery Voltage, $V_{BATTERY}$	f_{OSC} = 1, 2, 4MHz		2.6	-	V_{DD} - 1.3	V
Backup Battery Voltage, $V_{BATTERY}$	f_{OSC} = 32kHz		1.9	-	V_{DD} - 1.3	V
Leakage Current $\overline{\text{INTERRUPT}}$, $I_{OL}(2)$	$V_O = V_{DD}$	INT SOURCE Connected to V_{SS}	-	0.5	10	µA
Capacitance D0 - D7, $C_{I/O}$			-	8	-	pF
Capacitance A0 - A4, $C_{ADDRESS}$			-	6	-	pF