

### DESCRIPTION

The HY62U8512/HY62U8512-I is a high speed, low power and 512K bit CMOS SRAM organized as 64,000 words by 8bit. The HY62U8512 / HY62U8512-I uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

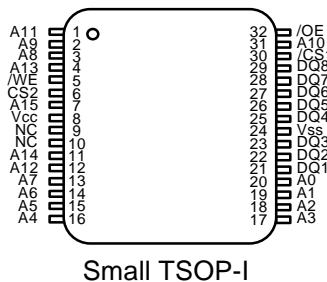
### FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(L/LL-part)
  - 2.0V(min) data retention
- Standard pin configuration
  - 32pin 8x13.4mm Small TSOP-I (Standard)

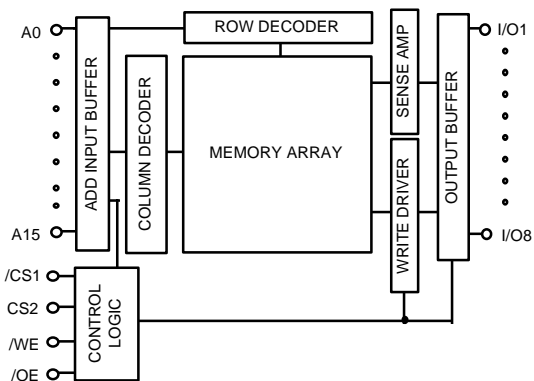
Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)		Temperature (jÉ)
				L	LL	
HY62U8512	3.0	85*/100/120	5	50	10	0~70(Normal)
HY62U8512-I	3.0	85*/100/120	5	50	10	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature  
 2. Current value is max.  
 3. \* measured with 30pF test load

### PIN CONNECTION



### BLOCK DIAGRAM



### PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS1	Chip Select 1	A0 ~ A15	Address Input
CS2	Chip Select 2	I/O1 ~ I/O8	Data Input/Output
/WE	Write Enable	Vcc	Power(3.0V)
/OE	Output Enable	Vss	Ground

### ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62U8512LST	85*/100/120	L-part		Small TSOP-I(Standard)
HY62U8512LLST	85*/100/120	LL-part		Small TSOP-I(Standard)
HY62U8512LST-I	85*/100/120	L-part	E.T.	Small TSOP-I(Standard)
HY62U8512LLST-I	85*/100/120	LL-part	E.T.	Small TSOP-I(Standard)

Note 1. E.T. : Extended Temperature, Blank : Normal Temperature  
 2. \* measured with 30pF test load.

**ABSOLUTE MAXIMUM RATING (1)**

Symbol	Parameter	Rating	Unit	Remark
V <sub>CC</sub> , V <sub>IN</sub> , V <sub>OUT</sub>	Power Supply, Input/Output Voltage	-0.5 to 4.6	V	
T <sub>A</sub>	Operating Temperature	0 to 70	°C	HY62U8512
		-40 to 85	°C	HY62U8512-I
T <sub>STG</sub>	Storage Temperature	-65 to 125	°C	
P <sub>D</sub>	Power Dissipation	1.0	W	
I <sub>OUT</sub>	Data Output Current	50	mA	
T <sub>SOLDER</sub>	Lead Soldering Temperature & Time	260•10	°C•sec	

**Note**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**RECOMMENDED DC OPERATING CONDITION**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	2.7	3.0	3.3	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3(1)	-	0.4	V

**Note :**

- V<sub>IL</sub> = -1.5V for pulse width less than 30ns at 3.0V

**TRUTH TABLE**

/CS1	CS2	/WE	/OE	MODE	I/O OPERATION
H	X	X	X	Standby	High-Z
X	L	X	X		High-Z
L	H	H	H	Output Disabled	High-Z
L	H	H	L	Read	Data Out
L	H	L	X	Write	Data In

**Note :**

- H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=don't care

## DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 3.0V ±40%, T<sub>A</sub> = 0°C to 70°C(Normal)/ -40°C to 85°C(E.T.), unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> & V <sub>IN</sub> & V <sub>CC</sub>	-1	-	1	uA	
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> & V <sub>OUT</sub> & V <sub>CC</sub> , /CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-1	-	1	uA	
I <sub>CC</sub>	Operating Power Supply Current	/CS1 = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	3	5	mA	
I <sub>CC1</sub>	Average Operating Current	/CS1 = V <sub>IL</sub> CS2 = V <sub>IH</sub> , Min Duty Cycle = 100%, I <sub>I/O</sub> = 0mA	-	20	30	mA	
I <sub>SB</sub>	TTL Standby Current (TTL Input)	/CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub>	-	-	0.5	mA	
I <sub>SB1</sub>	Standby Current (CMOS Input)	/CS1 & V <sub>CC</sub> - 0.2V	L	-	1	50	uA
		CS2 & 0.2V or CS2 & V <sub>CC</sub> - 0.2V	LL	-	0.5	10	uA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	-	-	0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.2	-	-	V	

Note : Typical values are at V<sub>CC</sub> = 3.0V, T<sub>A</sub> = 25°C

## AC CHARACTERISTICS

V<sub>CC</sub> = 3.0V ±40%, T<sub>A</sub> = 0°C to 70°C(Normal)/ -40°C to 85°C(E.T.), unless otherwise specified

#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	t <sub>RC</sub>	Read Cycle Time	85	-	100	-	120	-	ns
2	t <sub>AA</sub>	Address Access Time	-	85	-	100	-	120	ns
3	t <sub>ACS</sub>	Chip Select Access Time	-	85	-	100	-	120	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	45	-	50	-	60	ns
5	t <sub>CLZ</sub>	Chip Select to Output in Low Z	10	-	10	-	20	-	ns
6	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	10	-	ns
7	t <sub>CHZ</sub>	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns
8	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	30	0	30	0	40	ns
9	t <sub>OH</sub>	Output Hold from Address Change	10	-	10	-	20	-	ns
WRITE CYCLE									
10	t <sub>WC</sub>	Write Cycle Time	85	-	100	-	120	-	ns
11	t <sub>CW</sub>	Chip Selection to End of Write	70	-	80	-	100	-	ns
12	t <sub>AW</sub>	Address Valid to End of Write	70	-	80	-	100	-	ns
13	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	0	-	ns
14	t <sub>WP</sub>	Write Pulse Width	55	-	60	-	85	-	ns
15	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	ns
16	t <sub>WHZ</sub>	Write to Output in High Z	0	30	0	30	0	50	ns
17	t <sub>DW</sub>	Data to Write Time Overlap	40	-	45	-	50	-	ns
18	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	5	-	ns

### AC TEST CONDITIONS

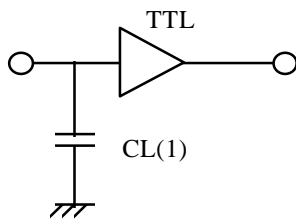
$T_A = 0; \dot{E}$  to  $70; \dot{E}$ (Normal) /  $-40; \dot{E}$  to  $85; \dot{E}$ (E.T.), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load
	CL* = 30pF + 1TTL Load

Note

\* : Test load is 30pF for 85ns device.

### AC TEST LOADS



Note : 1 Including jig and scope capacitance

### CAPACITANCE

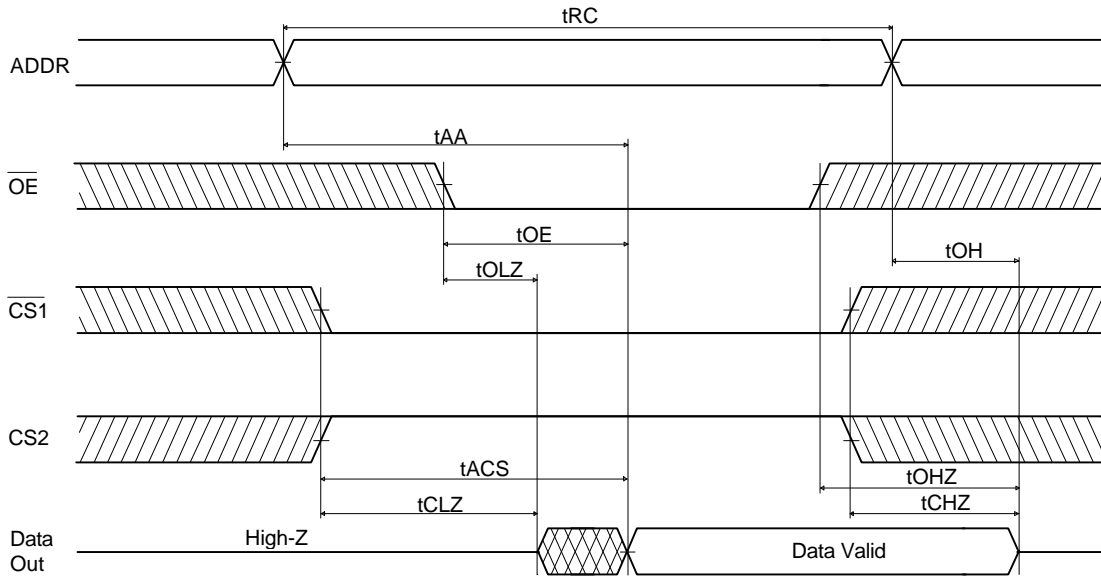
(Temp =  $25; \dot{E}$ , f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COU	Output Capacitance	V <sub>I/O</sub> = 0V	8	pF

Note : These parameters are sampled and not 100% tested

**TIMING DIAGRAM**

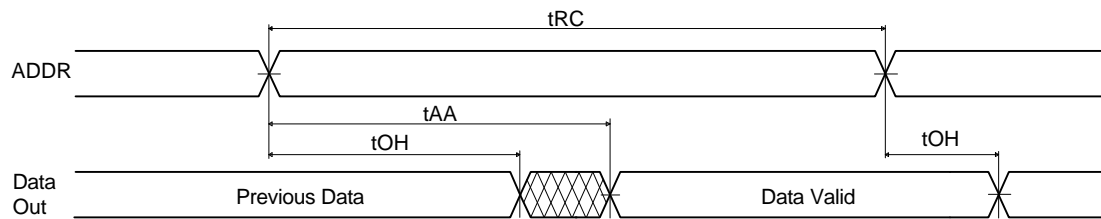
**READ CYCLE 1**



**Note(READ CYCLE):**

1.  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition,  $t_{CHZ}$  max. is less than  $t_{CLZ}$  min. both for a given device and from device to device.
3.  $\overline{WE}$  is high for the read cycle.

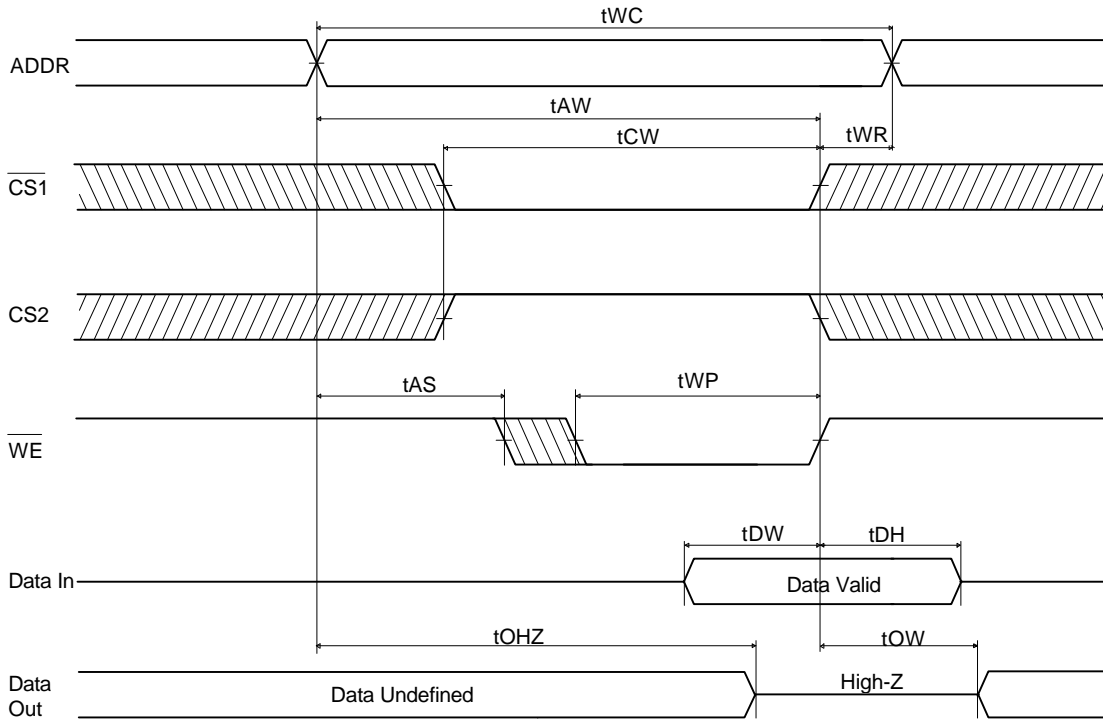
**READ CYCLE 2**



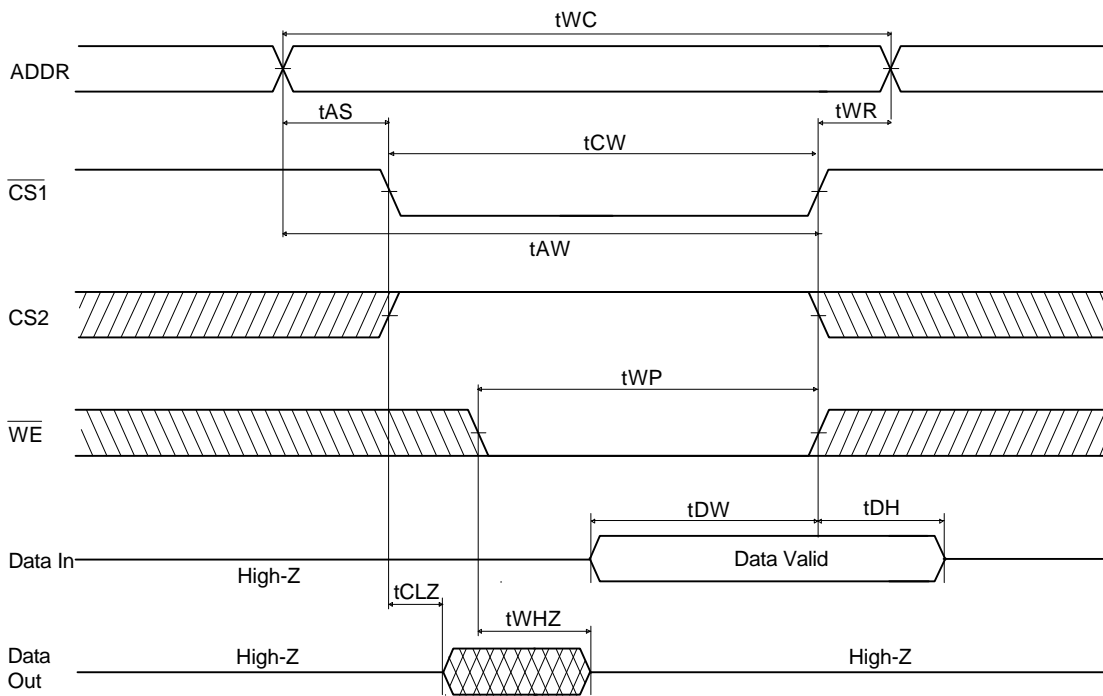
**Note(READ CYCLE):**

1.  $\overline{WE}$  is high for the read cycle.
2. Device is continuously selected  $\overline{CS1} = V_{IL}$ ,  $CS2 = V_{IH}$ .
3.  $\overline{OE} = V_{IL}$ .

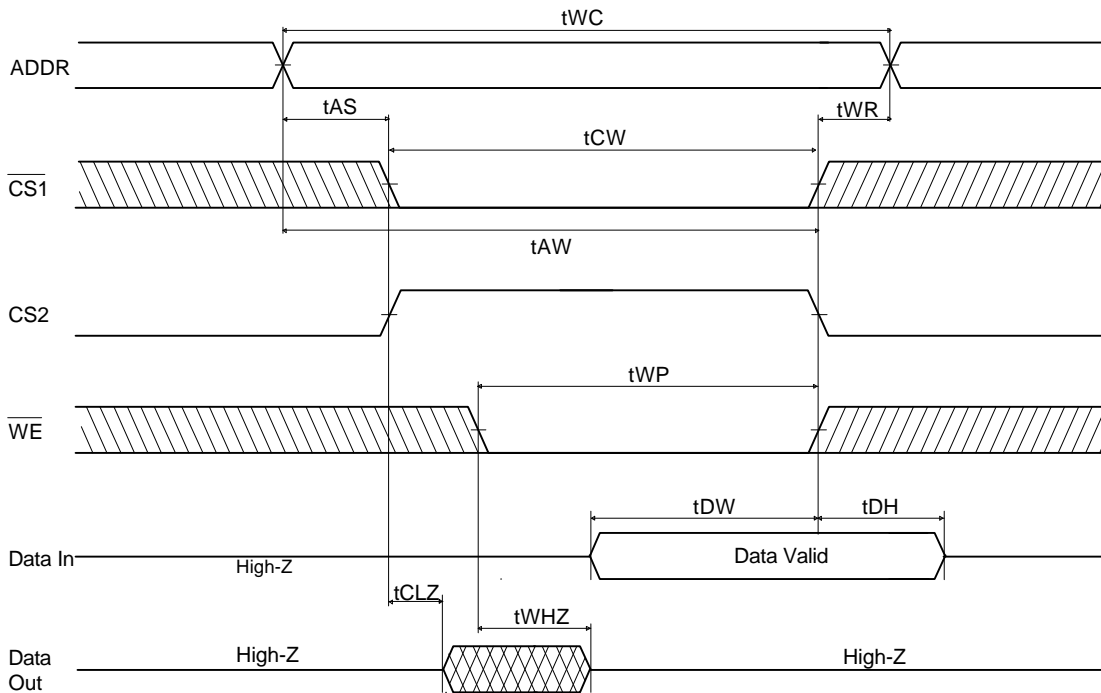
**WRITE CYCLE 1 (/WE Controlled)**



**WRITE CYCLE 2 (/CS1 Controlled)**



**WRITE CYCLE 3 (CS2 Controlled)**



**Notes(WRITE CYCLE):**

1. A write occurs during the overlap of a low /CS1, CS2 and low /WE. A write begins at the latest transition among /CS1 going low, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 low and /WE going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of /CS1 going low or CS2 going high to the end of write .
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends as /CS1, or /WE going high, and  $t_{WR}$  is applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7.  $D_{out}$  is the read data of the new address.
8. When /CS1 is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

### DATA RETENTION ELECTRIC CHARACTERISTIC

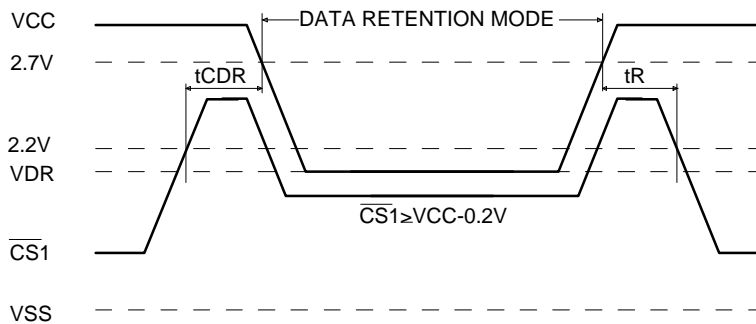
$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Normal) /  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  (E.T.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
VDR	Vcc for Data Retention	$\overline{\text{CS}}1 \leq V_{\text{CC}} - 0.2\text{V}$ , $\text{CS}2 \leq 0.2\text{V}$ or, $\overline{\text{CS}}1 \leq V_{\text{CC}} - 0.2\text{V}$ , $V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{CC}}$	2.0	-	-	V	
ICCDR	Data Retention Current	$V_{\text{CC}} = 3.0\text{V}$ , $\overline{\text{CS}}1 \leq V_{\text{CC}} - 0.2\text{V}$ , $\text{CS}2 \leq 0.2\text{V}$ or $V_{\text{CC}} - 0.2\text{V}$ , $V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{CC}}$	L	-	1	50	$\mu\text{A}$
			LL	-	0.5	10	$\mu\text{A}$
tCDR	Chip Deselect to Data Retention Time		0	-	-	ns	
tR	Operating Recovery Time		tRC(2)	-	-	ns	

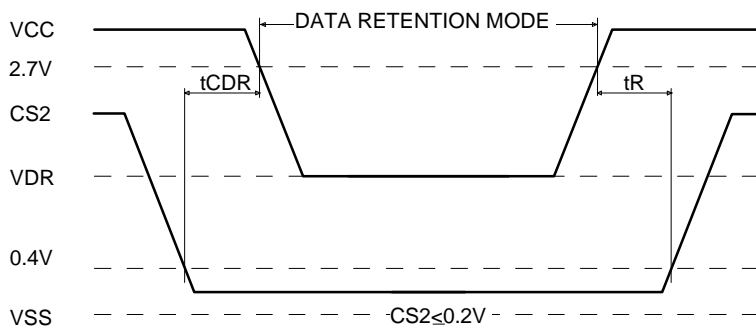
Notes:

1. Typical values are under the condition of  $T_A = 25^\circ\text{C}$ .
2. tRC is read cycle time.

### DATA RETENTION TIMING DIAGRAM 1



### DATA RETENTION TIMING DIAGRAM 2



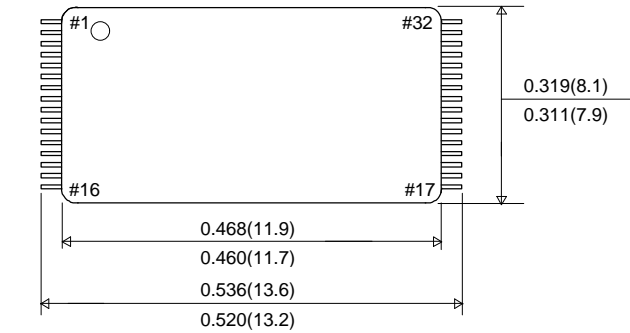
### RELIABILITY SPEC.

TEST MODE		TEST SPEC.
ESD	HBM	$\leq 2000\text{V}$
	MM	$\leq 250\text{V}$
LATCH - UP		$\leq 100\text{mA}$
		$\leq 100\text{mA}$



**PACKAGE INFORMATION**

32pin 8x13.4mm Thin Small Outline Package Standard(ST)



UNIT : INCH(mm)

