Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Crosstalk (7.0MHz) ..... <-56dB**
- **Fast access Time (Max. Over Temp.)..... 500ns**
- **TTL Compatible**

Applications

- **Wideband Switching**
- **Radar**
- **TV Video**
- **ECM**

Description

The HI-524/883 is a four channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 6.8MHz. The chip includes a 1 of 4 decoder for channel selection and an Enable input to inhibit all channels (chip select).

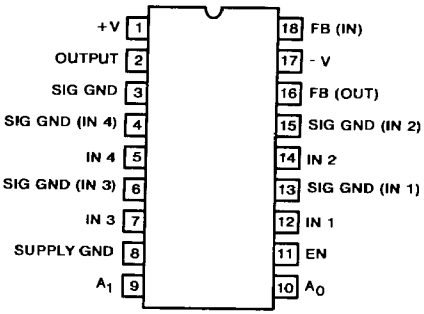
Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure that Crosstalk is less than -56dB at 7MHz.

The HI-524/883 is designed to operate into a wideband buffer amplifer such as the Harris HA-2541/883. The multiplexer chip includes two "on" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

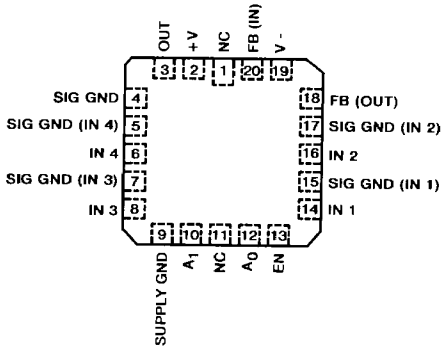
The HI-524/883 is well suited to the rapid switching of video and other wideband singals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin Ceramic DIP or 20 pad LCC and operates on ±15V supplies.

Pinouts

HI1-524/883 (CERAMIC DIP)
TOP VIEW

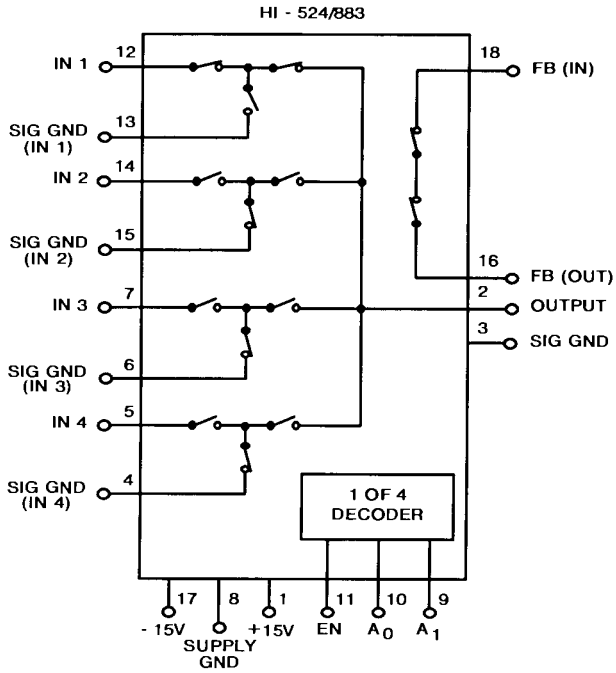


HI4-524/883 (CERAMIC LCC)
TOP VIEW



5 CMOS ANALOG MULTIPLEXERS

Functional Diagram



TRUTH TABLE

A1	A0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

***CHANNEL 1 IS SHOWN SELECTED IN THE DIAGRAM**

NOTE: Pin Numbers Refer to DIP Package Only.

Absolute Maximum Ratings

Voltage Between Supply Pins 33V
$+V_{SUPPLY}$ to Ground ..... +16.5V
$-V_{SUPPLY}$ to Ground ..... -16.5V
Analog Input Voltage
$+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Digital Input Voltage
$+V_{EN}$, $+V_A$ ..... +6V
$-V_{EN}$, $-V_A$ ..... -6V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... +275°C
Junction Temperature ..... +175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
Ceramic DIP Package ..... 22°C/W
Ceramic LCC Package ..... 19°C/W
Thermal Resistance, Junction-to-Ambient (θ_{ja})
Ceramic DIP Package ..... 81°C/W
Ceramic LCC Package ..... 76°C/W
Power Dissipation (at +75°C)
Ceramic DIP Package 1.23W
Ceramic LCC Package 1.32W
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package ..... 12.3mW/°C
Ceramic LCC Package ..... 13.2mW/°C
ESD Classification ..... ≤2000V

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Analog Input Voltage (V_S) ..... ±10V
Logic Level Low (V_{AL}) ..... 0V to 0.8V
Logic Level High (V_{AH}) ..... 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{AH} = 2.4V, V_{AL} = +0.8V, Unless Otherwise Specified

D.C.PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect all Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
	I_{IL}	Measure Inputs Sequentially, Connect All Unused Inputs to +5V	1, 2, 3	+25°C, +125°C, -55°C	-20	20	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = 10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = 10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{D(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = 10V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$-I_{D(ON)}$	V_S = V_D = -10V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Positive Supply Current	I(+)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I (+)	1, 2, 3	+25°C, +125°C, -55°C	-	25	mA
Negative Supply Current	I(-)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I (-)	1, 2, 3	+25°C, +125°C, -55°C	-23	-	mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	25	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-23	-	mA
Switch "ON" Resistance	R_{DS}	V_S = 0V I_D = ±100µA	1, 2, 3	+25°C, +125°C, -55°C	-	1500	Ω
Digital Input Threshold Characteristics	V_{AL}		1, 2, 3	+25°C +125°C, -55°C	-	0.8	V
	V_{AH}		1, 2, 3	+25°C +125°C, -55°C	2.4	-	V

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PEFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{AH} = 2.4, V_{AL} = 0.8V, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 500Ω, C_L = 12.5pF	9	+25°C	10	-	ns
			10	+125°C	2	-	ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 12.5pF	9	+25°C	-	300	ns
			10,11	+125°C, -55°C	-	500	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 500Ω, C_L = 12.5pF	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	500	ns
	$t_{OFF(EN)}$	R_L = 500Ω, C_L = 12.5pF	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	500	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{AH} = 2.4, V_{AL} = 0.8V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	C_A	V+ = V- = 0V, f = 1MHz	1	+25°C	-	7	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V, f = 1MHz	1	+25°C	-	10	pF
Capacitance: Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	1	+25°C	-	6	pF
Bandwidth (-3dB)	BW	V_S = 3Vp-p	1	+25°C	6.8	-	MHz
Crosstalk	C_t	V_S = 7MHz, 3Vp-p	1	+25°C	-56	-	dB
Break-Before-Make Time Delay	t_D	R_L = 500Ω, C_L = 12.5pF	1	-55°C	2	-	ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2, & 3)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

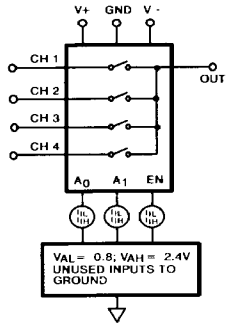
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

NOTE: 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon intial design release and upon design changes which would affect these characteristics.

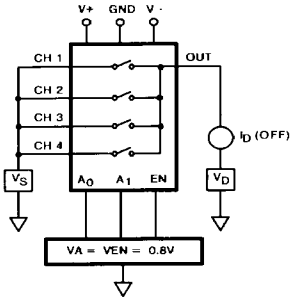
CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Test Circuits

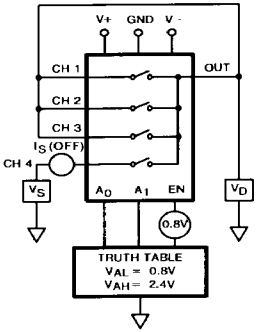
INPUT LEAKAGE CURRENT



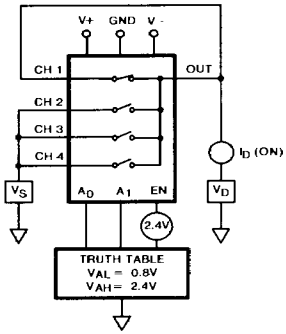
$I_{D(OFF)}$



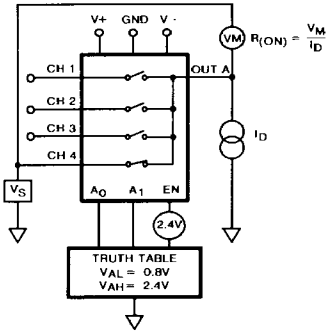
$I_{S(OFF)}$



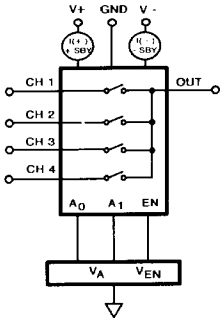
$I_{D(ON)}$



R_{DS}

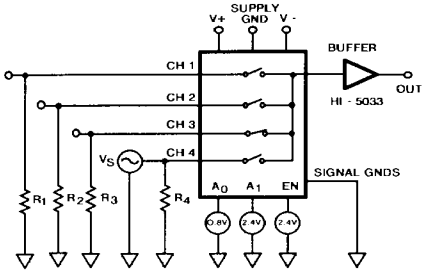


SUPPLY CURRENTS



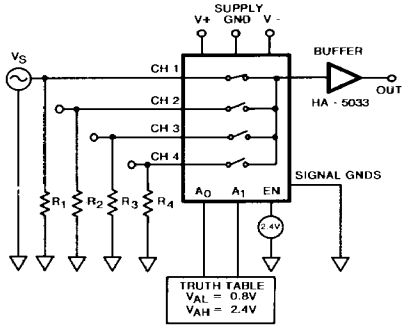
SBY: V_A = 0.8V, V_{EN} = 0.8V
OPERATIONAL: V_{EN} = 2.4V, V_A = All Combinations are Sequenced

CROSSTALK



NOTE: R_1 thru R_4 = 75Ω
Worst Case is Channel Selected with Input On Channel 4

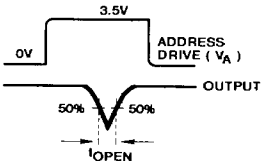
BANDWIDTH



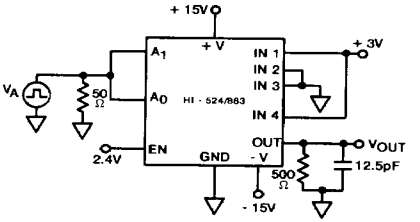
NOTES: R_1 thru R_4 = 75Ω
V_S Applied to Each Channel Separately, Worst Case is Recorded

Switching Waveforms

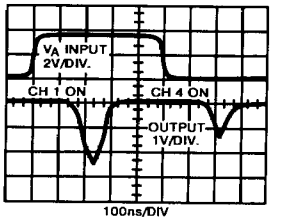
ADDRESS DRIVE



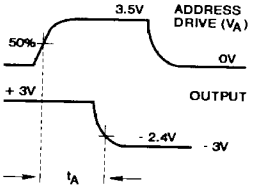
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



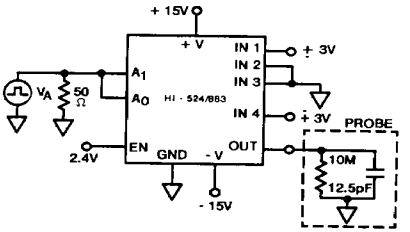
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



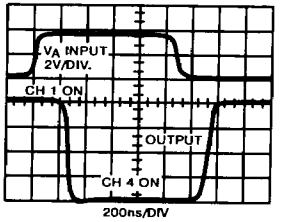
ADDRESS DRIVE



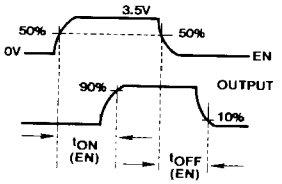
ACCESS TIME



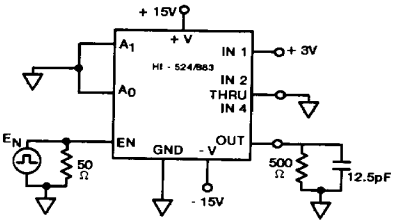
ACCESS TIME



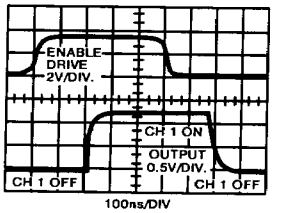
ENABLE DRIVE



ENABLE DELAY $t_{ON(EN)}$, t_{OFF} (EN)

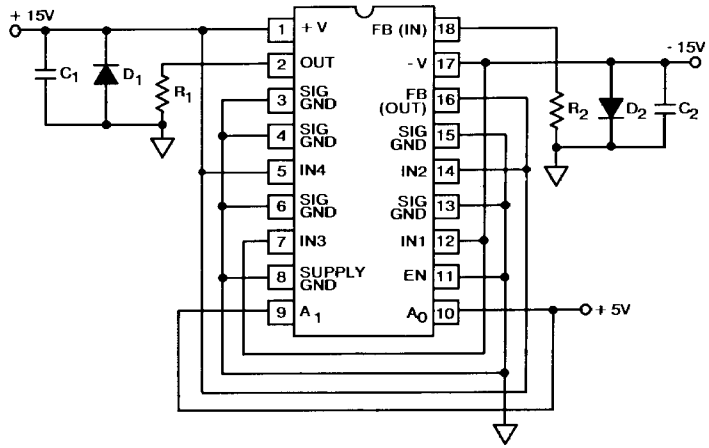


ENABLE DELAY $t_{ON(EN)}$, t_{OFF} (EN)

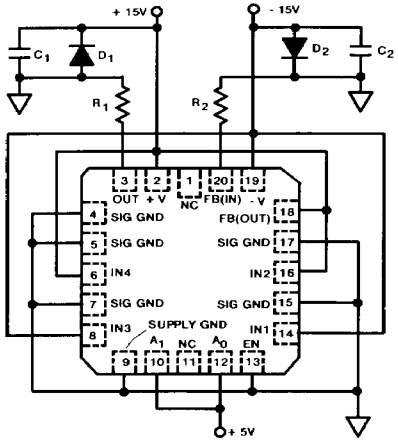


Burn-In Circuits

HA-524/883 CERAMIC DIP



HA-524/883 CERAMIC LCC

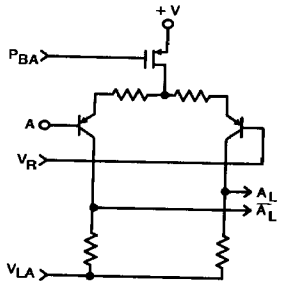


NOTES:

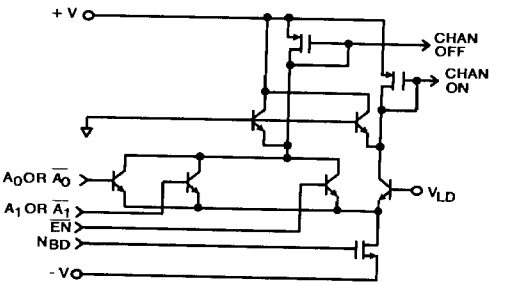
R_1 = 10kΩ, ±5%, 1/4 or1/2W (Per Socket)
R_2 = 10kΩ, ±5%, 1/4 or 1/2W (Per Socket)
C_1 = 0.01µF/Socket or 0.1µF/Row, (min.)
C_2 = 0.01µF/Socket or 0.1µF/Row, (min.)
$D_1 = D_2$ = 1N4002 or Equivalent/Board

Schematic Diagrams

ADDRESS/ENABLE INPUT BUFFER

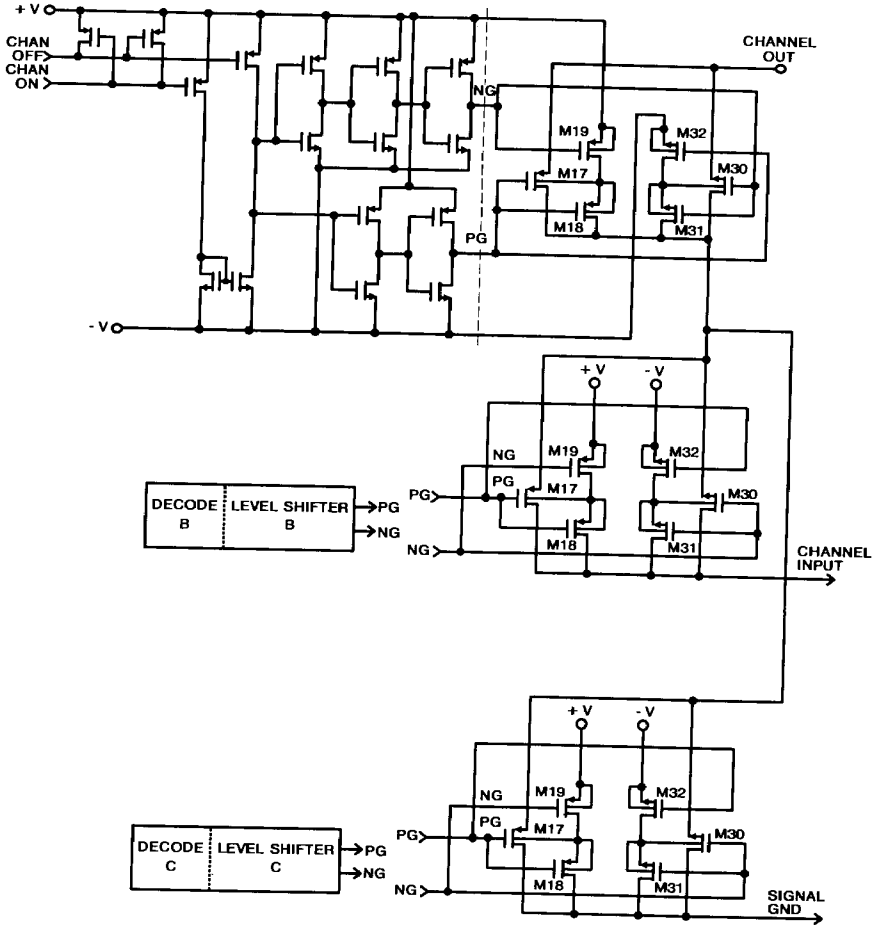


A-DECODE



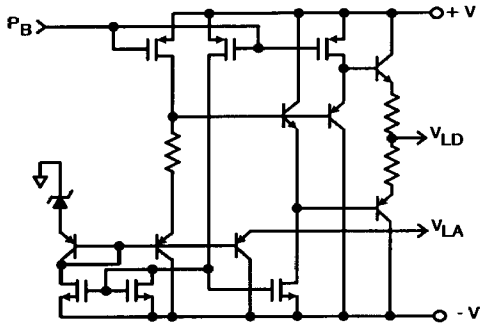
A-LEVEL SHIFTER

A-SWITCH CELL

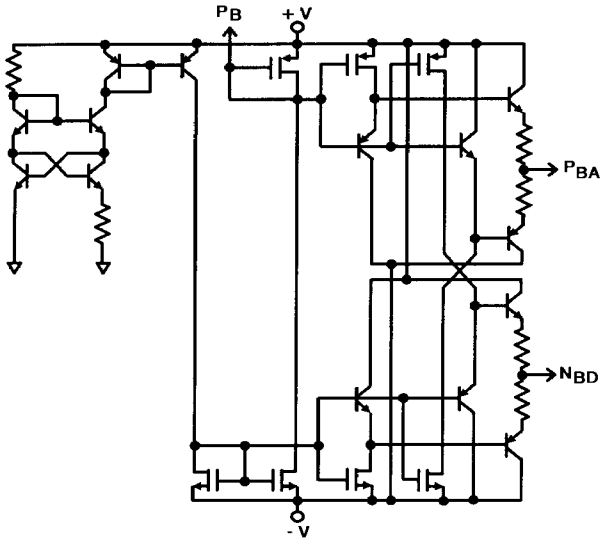


Schematic Diagrams (Continued)

REFERENCE VOLTAGES



BIAS



Die Characteristics

DIE DIMENSIONS:
146 x 89 x 19 mils
(3710 x 2260 x 483 µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$2 \times 10^5 A/cm^2$

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

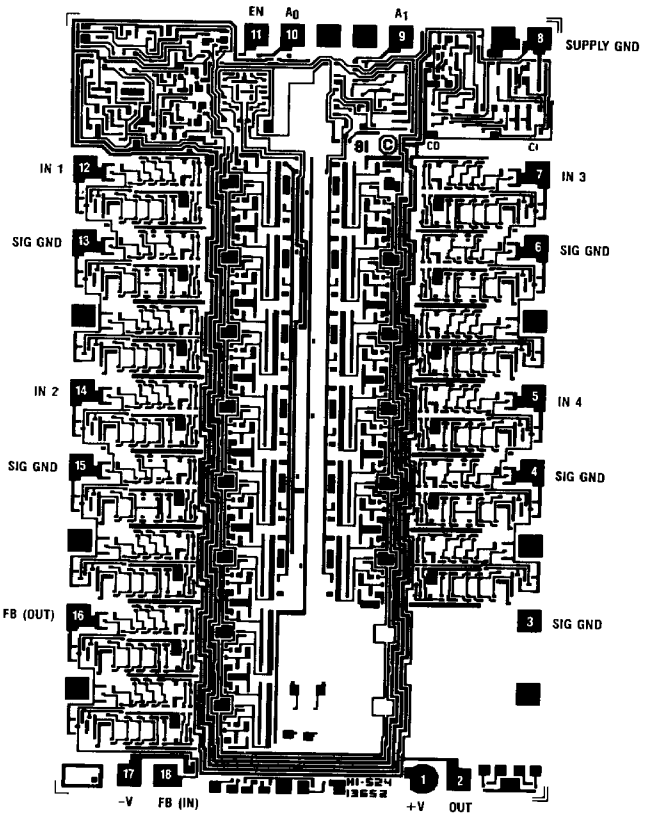
TRANSISTOR COUNT: 599

PROCESS: CMOS-DI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

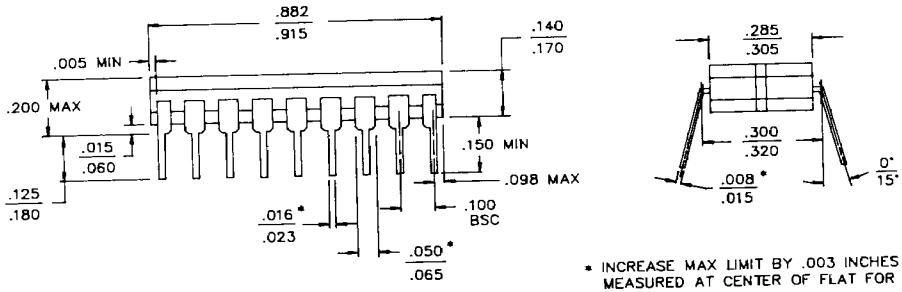
HI-524/883



NOTE: Pin Numbers Correspond to DIP Package Only.

Packaging†

18 PIN CERAMIC DIP

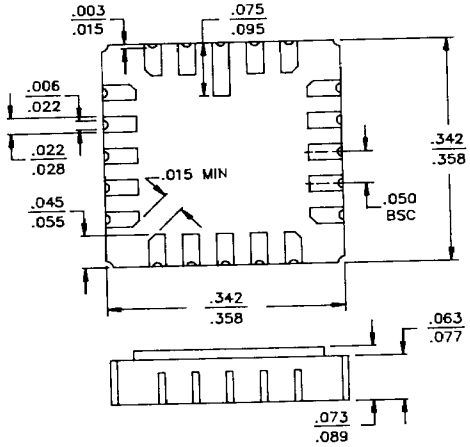


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

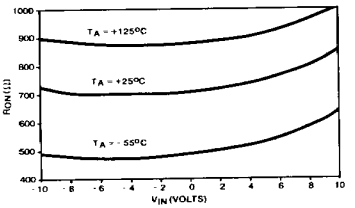
† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

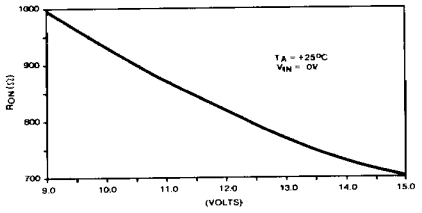
Typical Performance Characteristics

Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +2.4V, V_{AL} = 0.8V, Pin Numbers Refer to DIP.

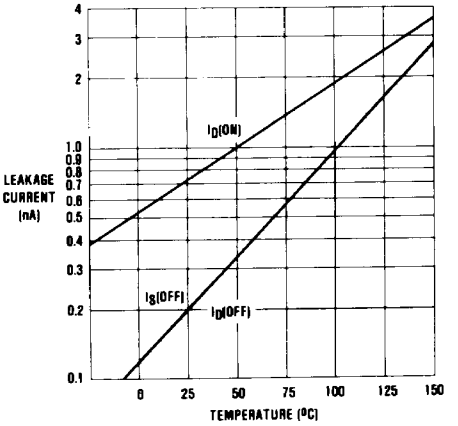
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



ON RESISTANCE vs. SUPPLY VOLTAGE

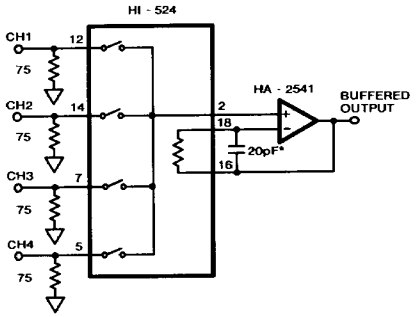


LEAKAGE CURRENT vs. TEMPERATURE



Applications

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



*Capacitor value may be selected to optimize AC performance.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ± 100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel "ON" resistance, to minimize offset voltage due to the buffer's bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These swiches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback and the amplifier remains stable.

All HI-524 package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors (0.1 to 1.0µF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.