HY62UF16100/ HY62QF16100/ HY62EF16100/ HY62SF16100 Series 64Kx16bit full CMOS SRAM

PRELIMINARY

DESCRIPTION

The HY62UF16100 / HY62QF16100 / HY62EF16100 / HY62SF16100 is a high speed, super low power and 1M bit full CMOS SRAM organized as 65,536 words by 16bit. The HY62UF16100 / HY62QF16100 / HY62EF16100 / HY62SF16100 uses high performance full CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.5V.

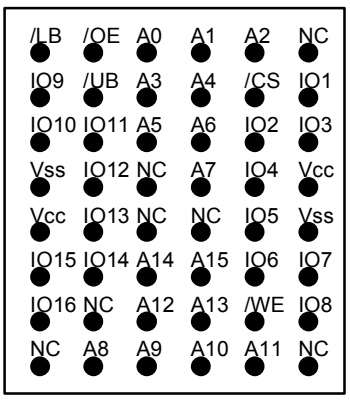
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL/SL-part)
  - 1.5V(min) data retention
- Standard pin configuration
  - 48ball uBGA

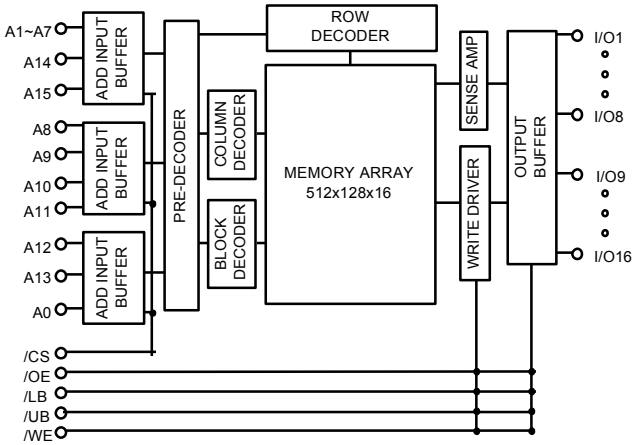
Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)		Temperature (••)
				LL	SL	
HY62UF16100	3.0	70/85/100	15	5	1	0~70(Normal)
HY62UF16100-I	3.0	70/85/100	15	5	1	-40~85(E.T.)
HY62QF16100	2.5	85/100/120	10	5	1	0~70(Normal)
HY62QF16100-I	2.5	85/100/120	10	5	1	-40~85(E.T.)
HY62EF16100	2.0	100/120/150	10	5	1	0~70(Normal)
HY62EF16100-I	2.0	100/120/150	10	5	1	-40~85(E.T.)
HY62SF16100	1.8	120/150/200	10	5	1	0~70(Normal)
HY62SF16100-I	1.8	120/150/200	10	5	1	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Funtion	Pin Name	Pin Funtion
/CS	Chip Select	I/O1~I/O16	Data Input/Output
/WE	Write Enable	A0~A15	Address Input
/OE	Output Enable	Vcc	Power(3.0V/2.5V/2.0V/1.8V)
/LB	Low Byte Control(I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control(I/O9~I/O16)	NC	No Connection

ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62UF16100LLM	70/85/100	LL-part		uBGA
HY62UF16100SLM	70/85/100	SL-part		uBGA
HY62UF16100LLM-I	70/85/100	LL-part	E.T.	uBGA
HY62UF16100SLM-I	70/85/100	SL-part	E.T.	uBGA
HY62QF16100LLM	85/100/120	LL-part		uBGA
HY62QF16100SLM	85/100/120	SL-part		uBGA
HY62QF16100LLM-I	85/100/120	LL-part	E.T.	uBGA
HY62QF16100SLM-I	85/100/120	SL-part	E.T.	uBGA
HY62EF16100LLM	100/120/150	LL-part		uBGA
HY62EF16100SLM	100/120/150	SL-part		uBGA
HY62EF16100LLM-I	100/120/150	LL-part	E.T.	uBGA
HY62EF16100SLM-I	100/120/150	SL-part	E.T.	uBGA
HY62SF16100LLM	120/150/200	LL-part		uBGA
HY62SF16100SLM	120/150/200	SL-part		uBGA
HY62SF16100LLM-I	120/150/200	LL-part	E.T.	uBGA
HY62SF16100SLM-I	120/150/200	SL-part	E.T.	uBGA

Note 1. E.T. : Extended Temperature, Blank : Normal Temperature

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{IN}, V_{OUT}	Input/Output Voltage	-0.2 to 3.6	V	
V_{CC}	Power Supply	-0.2 to 4.0	V	
T_A	Operating Temperature	0 to 70	••	HY62UF16100
				HY62QF16100
				HY62EF16100
				HY62SF16100
		-40 to 85	••	HY62UF16100-I
				HY62QF16100-I
				HY62EF16100-I
				HY62SF16100-I
T_{STG}	Storage Temperature	-55 to 150	••	
P_D	Power Dissipation	1.0	W	
T_{SOLDER}	Lead Soldering Temperature & Time	260•5	•••sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Product	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	HY62UF16100-(I)	2.7	3.0	3.3	V
		HY62QF16100-(I)	2.2	2.5	2.8	V
		HY62EF16100-(I)	1.8	2.0	2.2	V
		HY62SF16100-(I)	1.6	1.8	2.0	
Vss	Ground	HY62UF16100-(I) HY62QF16100-(I) HY62EF16100-(I) HY62SF16100-(I)	0	0	0	V
V_{IH}	Input High Voltage	HY62UF16100-(I)	2.2	-	Vcc+0.2	V
		HY62QF16100-(I)	2.0	-	Vcc+0.2	V
		HY62EF16100-(I)	1.6	-	Vcc+0.2	V
		HY62SF16100-(I)	1.4		Vcc+0.2	V
V_{IL}	Input Low Voltage	HY62UF16100-(I) HY62QF16100-(I) HY62EF16100-(I) HY62SF16100-(I)	-0.2(1)	-	0.4	V

Note : 1. VIL = -1.5V for pulse width less than 30ns

TRUTH TABLE

/CS	/WE	/OE	/LB	/UB	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	Not Selected	Hi-Z	Hi-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disabled	Hi-Z	Hi-Z	Icc
L	X	X	H	H		Hi-Z	Hi-Z	
L	H	L	L	H	Read	D_{OUT}	Hi-Z	Icc
			H	L		Hi-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	Hi-Z	Icc
			H	L		Hi-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

Note:
1. H=V_{IH}, L=V_{IL}, X=don't care
2. UB, LB(Upper, Lower Byte enable)
   These active LOW inputs allow individual bytes to be written or read.
   When LB is LOW, data is written or read to the lower byte, I/O 1 -I/O 8.
   When UB is LOW, data is written or read to the Upper byte, I/O 9 -I/O 16.

DC ELECTRICAL CHARACTERISTICS

Vcc = 3.0V•• 10%/2.5V•• 10%/2.0V•• 10%/1.8V•• 10%, T_A = 0•• to 70•• (Normal)/ -40•• to 85•• (E.T.)

Sym	Parameter		Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		Vss •• V_{IN} •• Vcc		-1	-	1	uA
I_{LO}	Output Leakage Current		Vss •• V_{OUT} •• Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL} /UB = V_{IH} or /LB = V_{IH}		-1	-	1	uA
Icc	Operating Power Supply Current		/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA	Vcc = 3.0V	-	8	15	mA
				Vcc = 2.5V/2V/ 1.8V	-	5	10	mA
I_{CC1}	Average Operating Current	HY62UF16100-(I)	/CS = V_{IL}, Min Duty Cycle = 100% $I_{I/O}$ = 0mA		-	-	80	mA
		HY62QF16100-(I)			-	-	60	mA
		HY62EF16100-(I)			-	-	40	mA
		HY62SF16100-(I)			-	-	35	mA
I_{SB}	TTL Standby Current (TTL Input)	HY62UF16100-(I)	/CS = V_{IH}		-	-	0.5	mA
		HY62QF16100-(I)			-	-	0.3	mA
		HY62EF16100-(I)			-	-	0.3	mA
		HY62SF16100-(I)			-	-	0.3	mA
I_{SB1}	Standby Current (CMOS Input)		/CS •• Vcc - 0.2V	SL	-	0.05	1	uA
				LL	-	-	5	uA
V_{OL}	Output Low Voltage		Vcc = 3.0V	I_{OL} = 2.1mA	-	-	0.4	V
			Vcc = 2.5V	I_{OL} = 0.5mA				
			Vcc = 2.0V	I_{OL} = 0.33mA				
			Vcc = 1.8V	I_{OL} = 0.26mA				
V_{OH}	Output High Voltage	HY62UF16100-(I)	Vcc = 3.0V	I_{OH} = -1.0mA	2.2	-	-	V
		HY62QF16100-(I)	Vcc = 2.5V	I_{OH} = -0.5mA	2.0	-	-	V
		HY62EF16100-(I)	Vcc = 2.0V	I_{OH} = -0.44mA	1.6	-	-	V
		HY62SF16100-(I)	Vcc = 1.8V	I_{OH} = -0.44mA	1.4	-	-	V

Note : Typical values are at Vcc = 3.0V/2.5V/2.0V/1.8V, T_A = 25••

AC CHARACTERISTICS

Vcc = 3.0V••10%, TA = 0•• to 70••(Normal)/ -40•• to 85••(E.T.), unless otherwise specified

#	Symbol	Parameter	-70		-85		-10		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	40	-	45	-	50	ns
5	tBA	/LB, /UB Access Time	-	40	-	45	-	50	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	10	-	20	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	5	-	10	-	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	30	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	30	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	30	0	30	ns
12	tOH	Output Hold from Address Change	10	-	10	-	15	-	ns
	WRITE CYCLE								
13	tWC	Write Cycle Time	70	-	85	-	100	-	ns
14	tCW	Chip Selection to End of Write	60	-	70	-	80	-	ns
15	tAW	Address Valid to End of Write	60	-	70	-	80	-	ns
16	tBW	/LB, /UB Valid to End of Write	60	-	70	-	80	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	50	-	55	-	75	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	25	0	30	0	35	ns
21	tDW	Data to Write Time Overlap	30	-	35	-	45	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	5	-	5	-	10	-	ns

Vcc = 2.5V••10%, TA = 0•• to 70••(Normal)/ -40•• to 85••(E.T.), unless otherwise specified

#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	60	ns
5	tBA	/LB, /UB Access Time	-	45	-	50	-	60	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	20	-	20	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	5	-	10	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	10	-	10	-	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	40	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	30	0	40	ns
12	tOH	Output Hold from Address Change	10	-	15	-	15	-	ns
	WRITE CYCLE								
13	tWC	Write Cycle Time	85	-	100	-	120	-	ns
14	tCW	Chip Selection to End of Write	70	-	80	-	100	-	ns
15	tAW	Address Valid to End of Write	70	-	80	-	100	-	ns
16	tBW	/LB, /UB Valid to End of Write	70	-	80	-	100	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	55	-	75	-	85	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	30	0	35	0	40	ns
21	tDW	Data to Write Time Overlap	35	-	45	-	50	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	5	-	10	-	10	-	ns

Vcc = 2.0V••10%, T_A = 0•• to 70••(Normal)/ -40•• to 85••(E.T.), unless otherwise specified

#	Symbol	Parameter	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	100	-	120	-	150	-	ns
2	tAA	Address Access Time	-	100	-	120	-	150	ns
3	tACS	Chip Select Access Time	-	100	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	50	-	60	-	75	ns
5	tBA	/LB, /UB Access Time	-	50	-	60	-	75	ns
6	tCLZ	Chip Select to Output in Low Z	20	-	20	-	20	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	10	-	10	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	10	-	10	-	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	40	0	50	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	40	0	50	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	40	0	50	ns
12	tOH	Output Hold from Address Change	15	-	15	-	15	-	ns
	WRITE CYCLE								
13	tWC	Write Cycle Time	100	-	120	-	150	-	ns
14	tCW	Chip Selection to End of Write	80	-	100	-	120	-	ns
15	tAW	Address Valid to End of Write	80	-	100	-	120	-	ns
16	tBW	/LB, /UB Valid to End of Write	80	-	100	-	120	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	75	-	85	-	100	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	35	0	40	0	50	ns
21	tDW	Data to Write Time Overlap	45	-	50	-	60	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	10	-	10	-	10	-	ns

Vcc = 1.8V••10%, TA = 0•• to 70••(Normal)/ -40•• to 85••(E.T.), unless otherwise specified

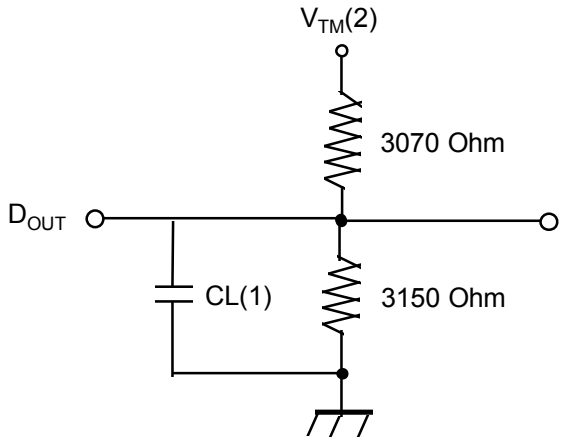
#	Symbol	Parameter	-12		-15		-20		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	120	-	150	-	200	-	ns
2	tAA	Address Access Time	-	120	-	150	-	200	ns
3	tACS	Chip Select Access Time	-	120	-	150	-	200	ns
4	tOE	Output Enable to Output Valid	-	60	-	75	-	100	ns
5	tBA	/LB, /UB Access Time	-	60	-	75	-	100	ns
6	tCLZ	Chip Select to Output in Low Z	20	-	20	-	30	-	ns
7	tOLZ	Output Enable to Output in Low Z	10	-	10	-	15	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	10	-	10	-	15	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	40	0	50	0	60	ns
10	tOHZ	Out Disable to Output in High Z	0	40	0	50	0	60	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	40	0	50	0	60	ns
12	tOH	Output Hold from Address Change	15	-	15	-	30	-	ns
	WRITE CYCLE								
13	tWC	Write Cycle Time	120	-	150	-	200	-	ns
14	tCW	Chip Selection to End of Write	100	-	120	-	170	-	ns
15	tAW	Address Valid to End of Write	100	-	120	-	170	-	ns
16	tBW	/LB, /UB Valid to End of Write	100	-	120	-	170	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	85	-	100	-	135	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	60	0	70	0	80	ns
21	tDW	Data to Write Time Overlap	50	-	60	-	80	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	10	-	15	-	15	-	ns

AC TEST CONDITIONS

TA = 0•• to 70••(Normal) / -40•• to 85••(E.T.), unless otherwise specified

PARAMETER		Value
Input Pulse Level	HY62UF16100-(I)	0.4V to 2.2V
	HY62QF16100-(I)	0.4V to 2.2V
	HY62EF16100-(I)	0.4V to 1.8V
	HY62SF16100-(I)	0.4V to 1.6V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level	HY62UF16100-(I)	1.5V
	HY62QF16100-(I)	1.1V
	HY62EF16100-(I)	0.9V
	HY62SF16100-(I)	0.8V
Output Load		CL = 30pF + 1TTL Load

AC TEST LOADS



Note
1. Including jig and scope capacitance
2. V_{TM} = 2.8V for Vcc = 3.0V : HY62UF16100-(I)
   V_{TM} = 2.3V for Vcc = 2.5V : HY62QF16100-(I)
   V_{TM} = 1.8V for Vcc = 2.0V : HY62EF16100-(I)
   V_{TM} = 1.6V for Vcc = 1.8V : HY62SF16100-(I)

CAPACITANCE

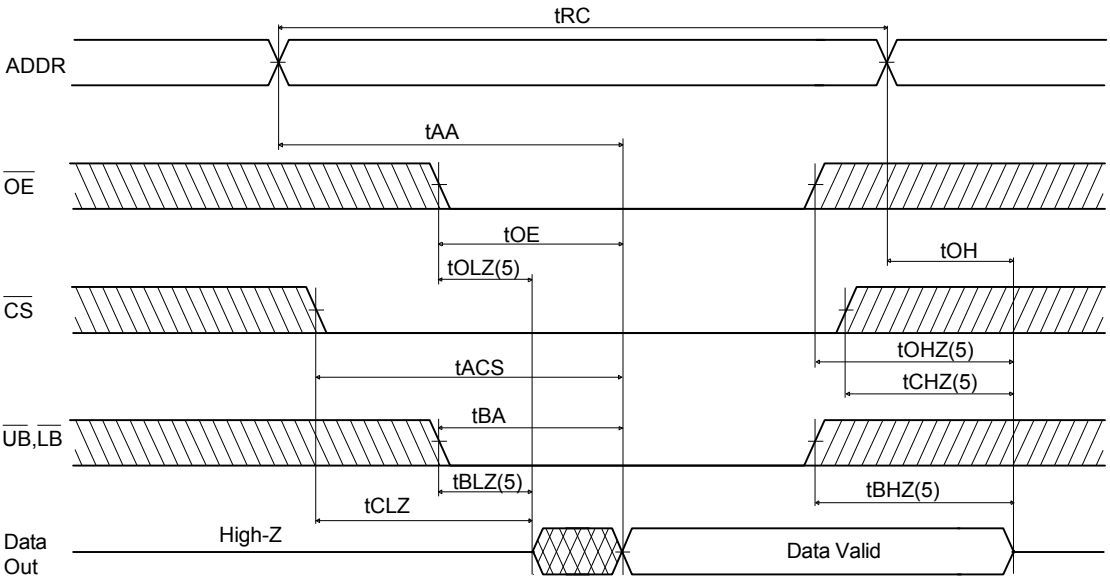
(Temp = 25••, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance(Add, /CS, /WE, /OE)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance(I/O)	$V_{I/O}$ = 0V	10	pF

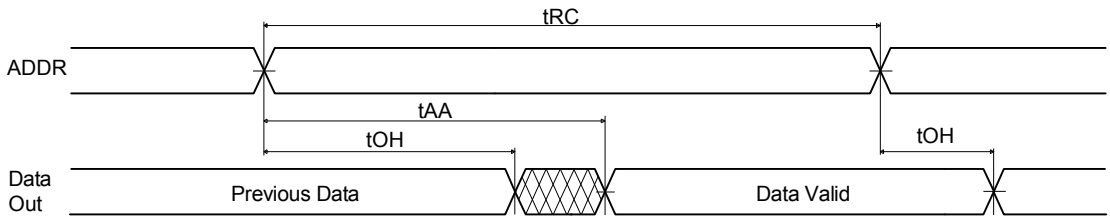
Note : These parameters are sampled and not 100% tested

TIMING DIAGRAM

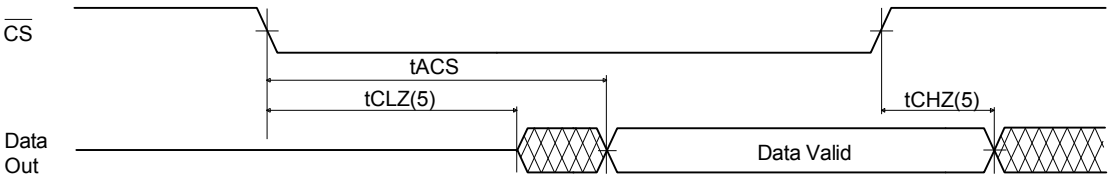
READ CYCLE 1(Note 1)



READ CYCLE 2(Note 1,2,4)

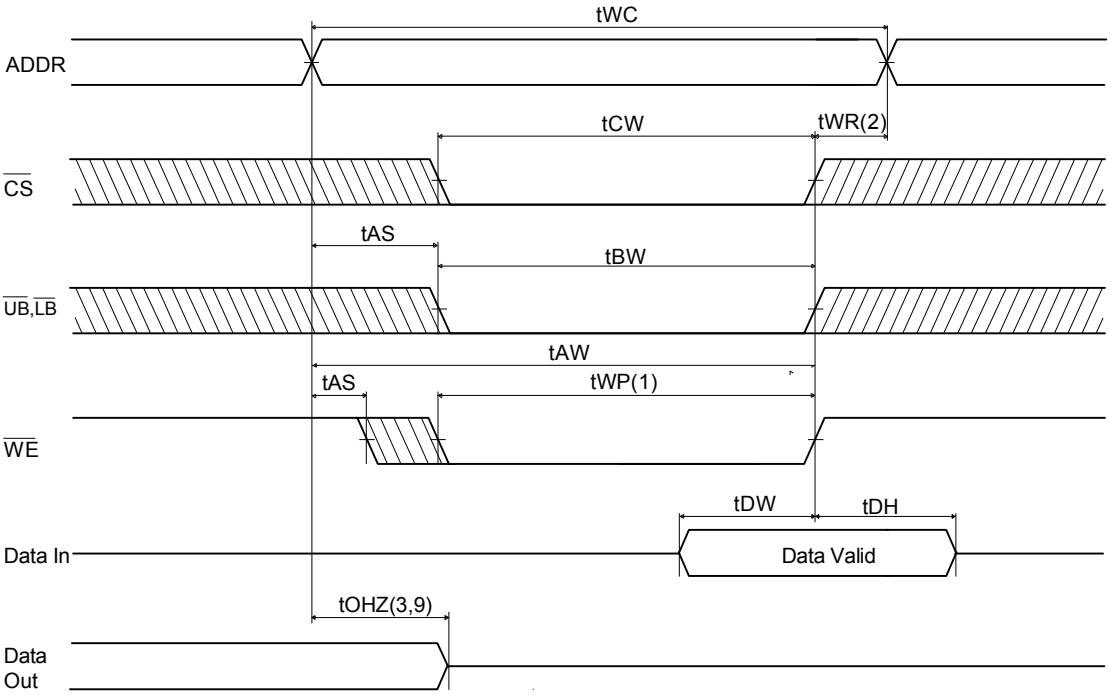


READ CYCLE 3(Note 1,3,4)

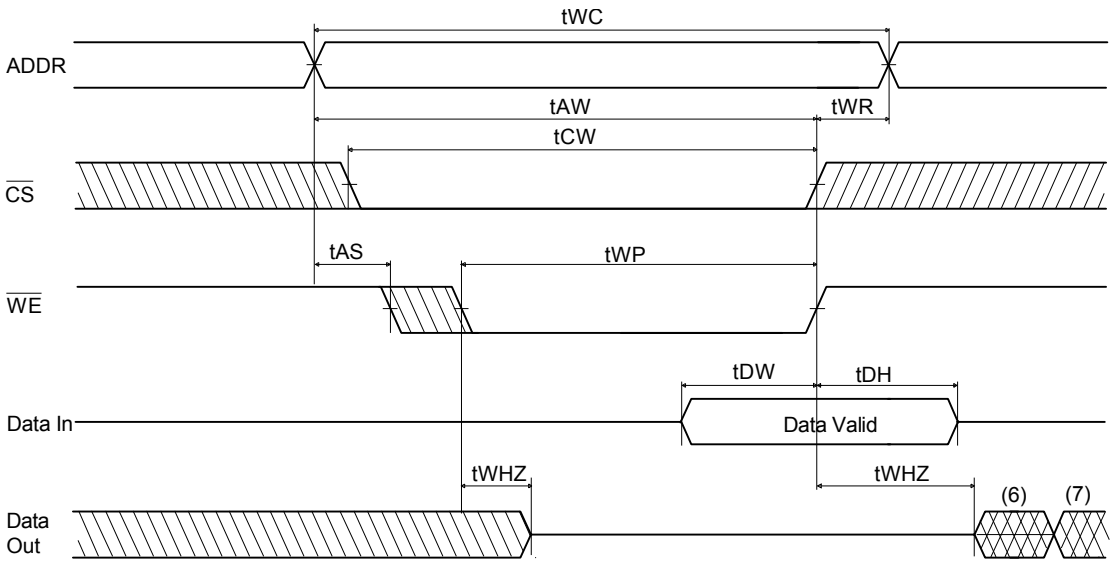


Notes:
1. /WE is high for the Read Cycle.
2. Device is continuously selected. /CS = V_{IL}
3. Address valid is prior to or coincident with /CS transition low
4. /OE = V_{IL}
5. Transition is measured + 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2 (Note 5)



Notes:
1. A write occurs during the overlap(tWP) of a low /CS and low /WE .
2. tWR is measured from the earlier of /CS, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low(/OE=V_{IL})
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. If /CS is low during this period, I/O pins are in the output state.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured +200mV from steady state.
   This parameter is sampled and not 100% tested.

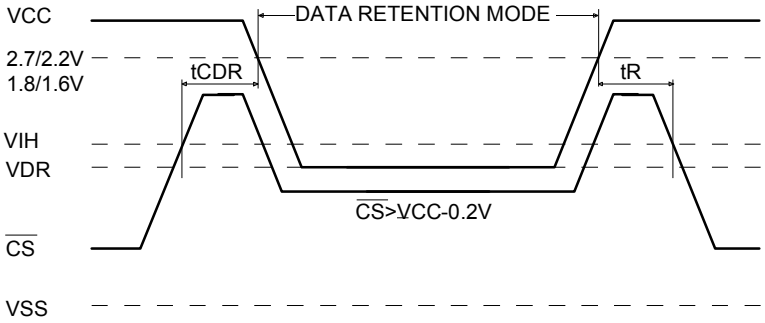
DATA RETENTION ELECTRIC CHARACTERISTIC

T_A=0•• to 70••(Normal)/-40•• to 85••(E.T.)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention	/CS••Vcc - 0.2V		1.5	-	3.3	V
I_{CCDR}	Data Retention Current	Vcc=2.0V, /CS••Vcc - 0.2V,	LL	-	-	5	uA
		Vss••V_{IN}••Vcc	SL	-	-	1	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time			$tRC_{(2)}$	-	-	ns

Notes:
1. Typical values are under the condition of T_A = 25••.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM



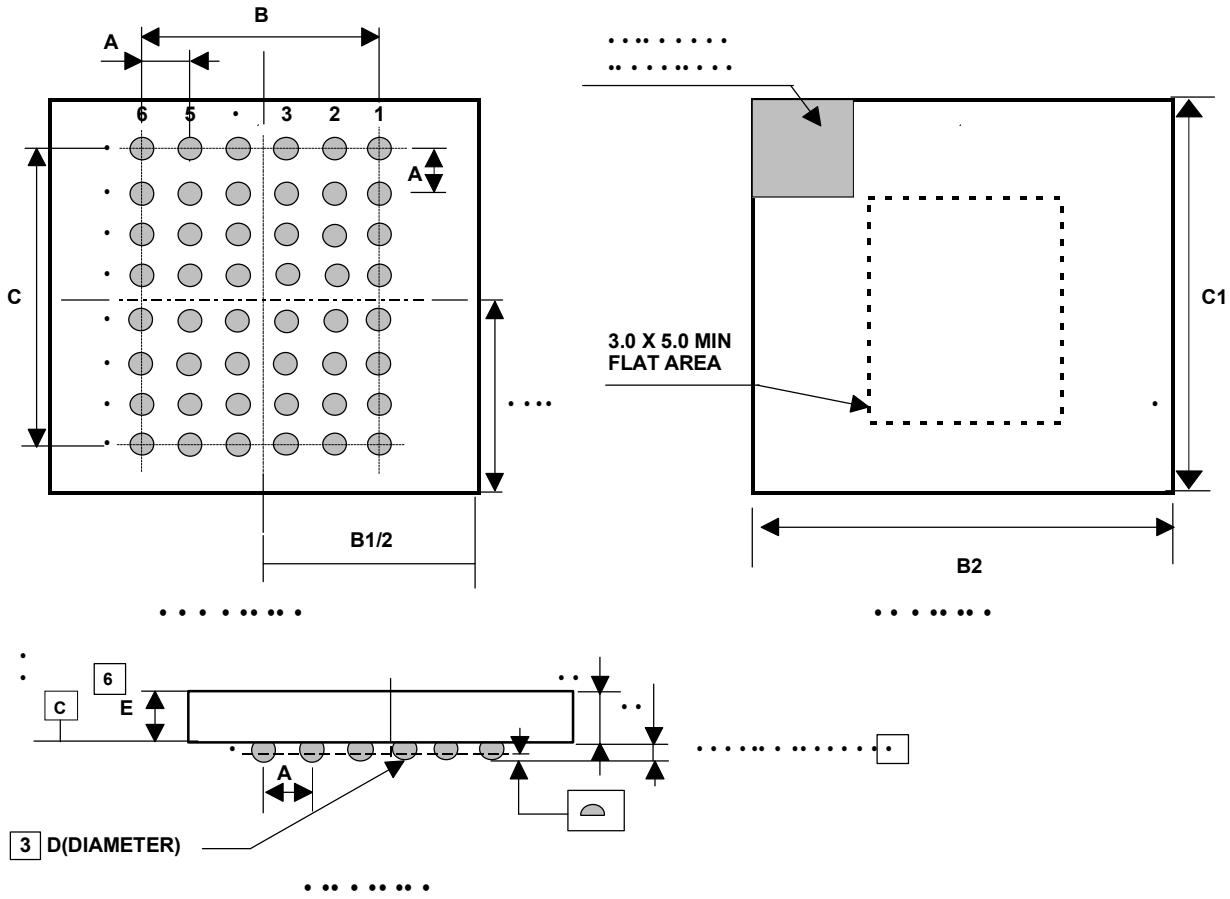
Note :
1. 2.7V : HY62UF16100 and HY62UF16100-I
   2.2V : HY62QF16100 and HY62QF16100-I
   1.8V : HY62EF16100 and HY62EF16100-I
   1.6V : HY62SF16100 and HY62SF16100-I

RELIABILITY SPEC.

TEST MODE		TEST SPEC.
ESD	HBM	•• 2000V
	MM	•• 250V
LATCH - UP		•• -100mA
		••100mA

PACKAGE INFORMATION

48ball Micro Ball Grid Array Package(M)



Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	-	3.75	-
B1	6.4	6.5	6.6
C	-	5.25	-
C1	6.1	6.2	6.3
D	0.25	0.3	0.35
E	0.79	0.8	0.81
E1	-	0.55	-
E2	0.2	0.25	0.3
r	-	-	0.08

Note

1. DIMENSIONING and TOLERANCING PER ASME Y14. SM-1994.
2. ALL DIMENSION ARE MILLIMETERS.
3. DIMENSION ••D•• IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. SOLDER BALL ARRAY MAY BE DEPOPULATED BY OMISSION BALLS FROM A FULL MATRIX NO SHIFTING OF MATRIX PATTERN IS ALLOWED.
6. THIS IS A CONTROLLING DIMENSION.