

# HM658128A Series

131072-word × 8-bit High Speed CMOS Pseudo Static  
RAM

# HITACHI

Rev. 8.0  
Jun. 5, 1995

The Hitachi HM658128A is a pseudo-static RAM organized as 131,072-word × 8-bit. HM658128A realizes low power consumption and high speed access time by employing 1.3 μm CMOS process technology. The HM658128A supports 3 refresh functions: address refresh, auto refresh and self refresh. Low power version dissipates only 350 μW (typ)/500 μW (typ) in self refresh mode and retains the data with battery. The HM658128A is pin-compatible with 1-Mbit static RAM.

## Features

- Single 5 V (± 10%)
- High speed
  - Access time  
CE Access time: 80/100/120 ns
  - Cycle time  
Random read/  
Write cycle time: 130/160/190 ns
- Low power:
  - Active: 300 mW (typ)
  - Standby: 350 μW (typ) (LL-version)  
500 μW (typ) (L-version)
- All inputs and outputs TTL compatible
- Non multiplexed address
- 512 refresh cycles (8 ms)
- Refresh functions
  - Address refresh
  - Automatic refresh
  - Self refresh

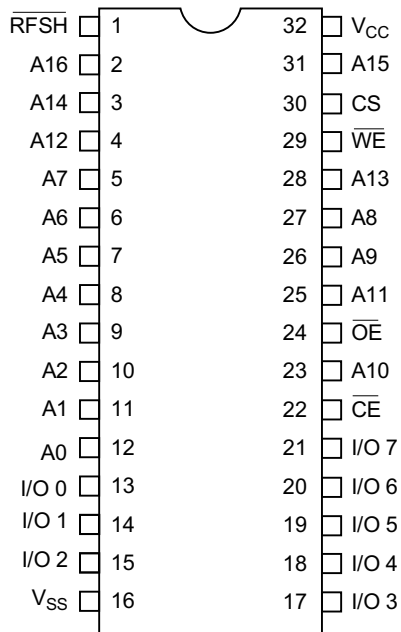
## Ordering Information

Type No.	Access time	Package
HM658128ALP-8	80 ns	600-mil 32-pin plastic DIP (DP-32)
HM658128ALP-10	100 ns	
HM658128ALP-12	120 ns	
HM658128ALP-8L	80 ns	
HM658128ALP-10L	100 ns	
HM658128ALP-12L	120 ns	
HM658128ALFP-8	80 ns	32-pin plastic SOP (FP-32D)
HM658128ALFP-10	100 ns	
HM658128ALFP-12	120 ns	
HM658128ALFP-8L	80 ns	
HM658128ALFP-10L	100 ns	
HM658128ALFP-12L	120 ns	
HM658128ALT-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP
HM658128ALT-10	100 ns	
HM658128ALT-12	120 ns	
HM658128ALT-8L	80 ns	(TFP-32D)
HM658128ALT-10L	100 ns	
HM658128ALT-12L	120 ns	
HM658128ALR-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP
HM658128ALR-10	100 ns	
HM658128ALR-12	120 ns	
HM658128ALR-8L	80 ns	reverse type (TFP-32DR)
HM658128ALR-10L	100 ns	
HM658128ALR-12L	120 ns	

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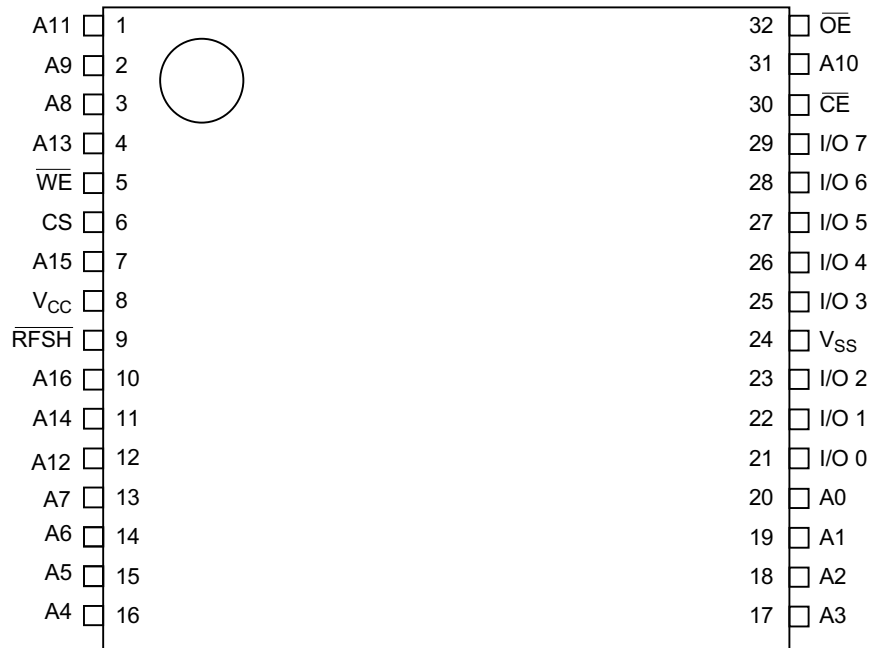
## Pin Arrangement

### HM658128ALP/ALFP Series



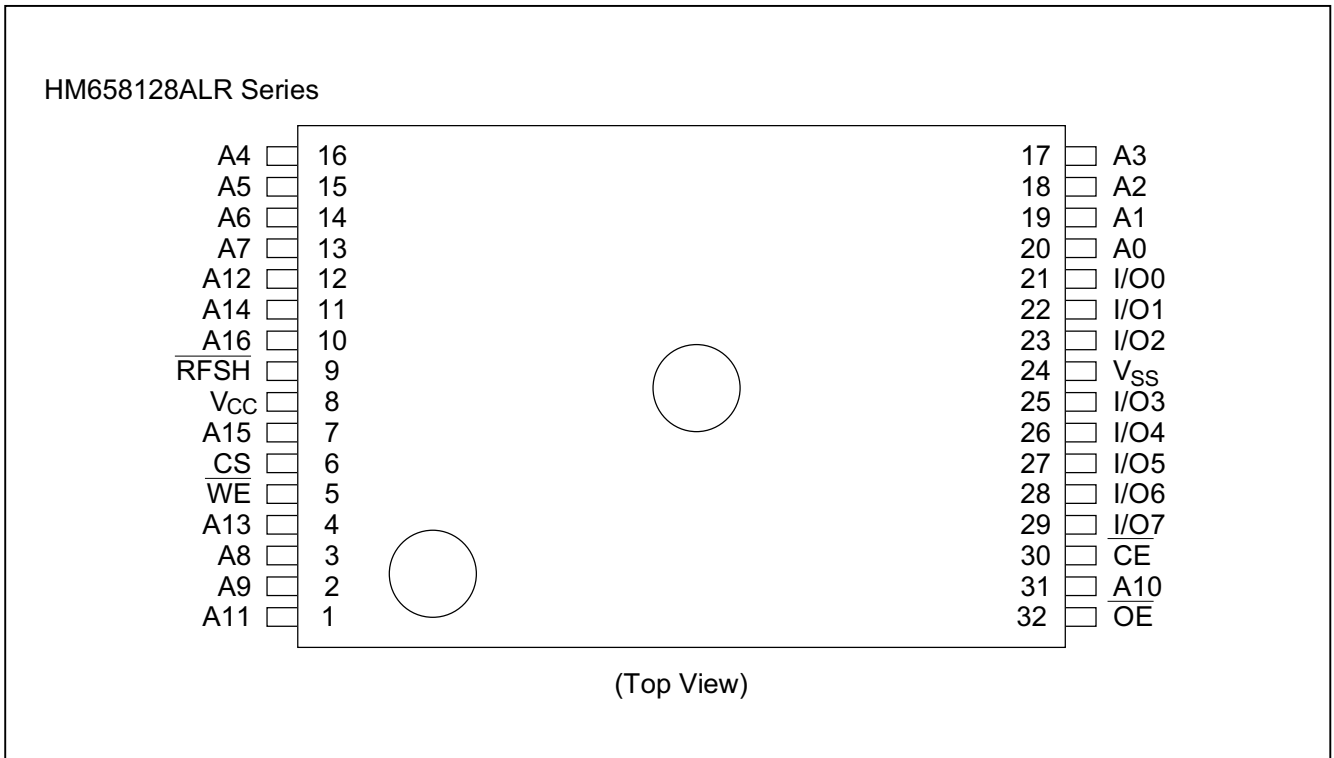
(Top View)

### HM658128ALT Series



(Top View)

Pin Arrangement (cont)

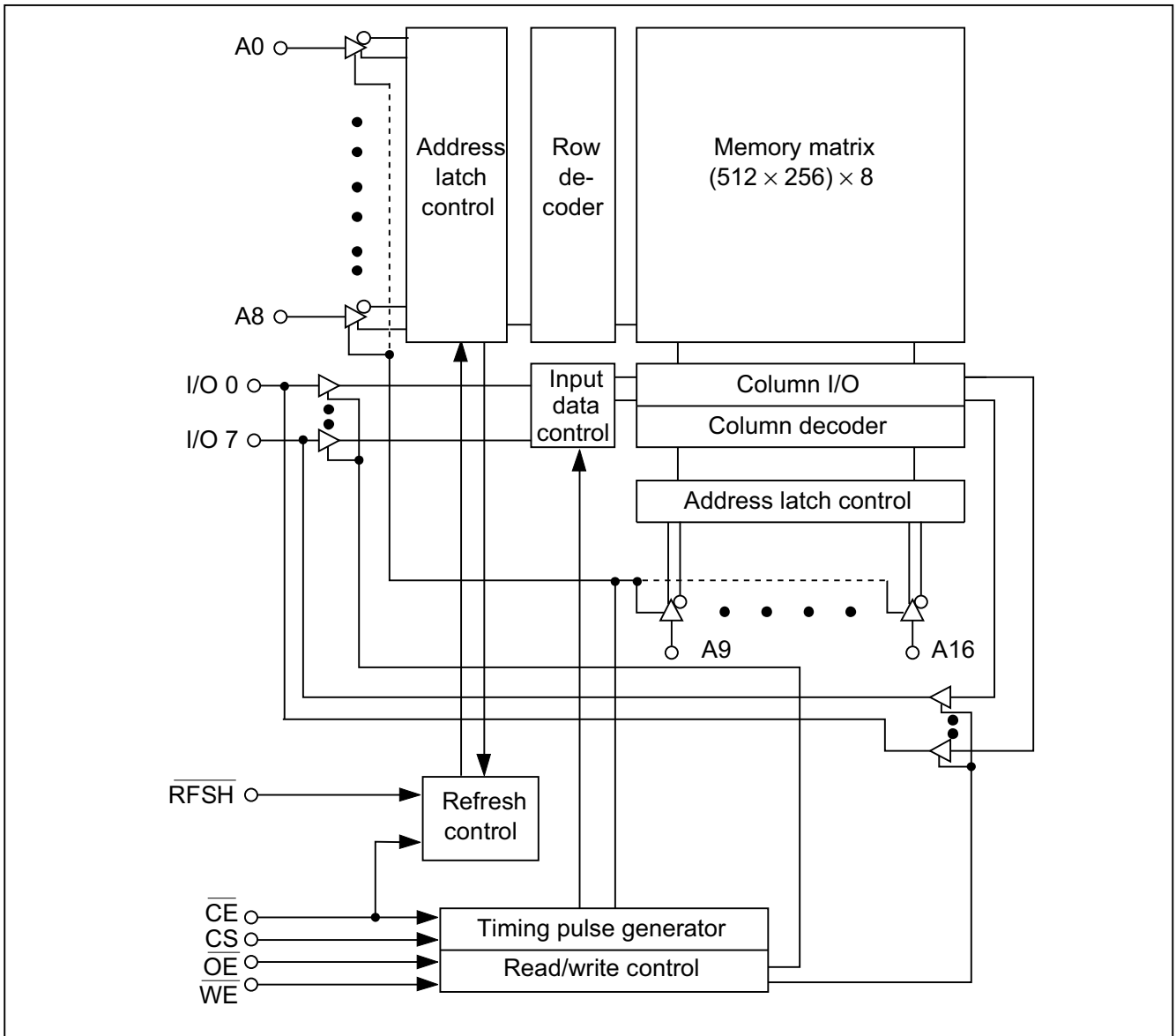


Pin Description

Symbol	Pin name
A0 to A16	Address inputs
I/O0 to I/O7	Data input/output
RFSH	Refresh
CE	Chip enable
OE	Output enable
WE	Write enable
CS	Chip select
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

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## Block Diagram



## Truth Table

$\overline{CE}$	CS at $\overline{CE}$ going low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O pin	Mode
L	H	X*1	L	H	Low-Z	Read
L	H	X	X	L	High-Z	Write
L	H	X	H	H	High-Z	—
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh
H	X	H	X	X	High-Z	Standby

Notes: 1. X means H or L.

**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to $V_{SS}$	$V_T$	-1.0 to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

**Recommended DC Operating Conditions ( $T_a = 0$  to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
	$V_{SS}$	0	0	0	V	
Input voltage	$V_{IH}$	2.2	—	6.0	V	
	$V_{IL}$	-0.5	—	0.8	V	1

Note: 1.  $V_{IL}$  min = -3.0 V for pulse width  $\leq 10$  ns.

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### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Operating power supply current	I <sub>CC1</sub>	—	60	85	mA	I <sub>I/O</sub> = 0 mA t <sub>cyc</sub> = min.	
Standby power supply current	I <sub>SB1</sub>	—	1	2	mA	$\overline{CE} = V_{IH}$ RFSH = V <sub>IH</sub> , Vin ≥ 0 V	
Standby power supply current	I <sub>SB2</sub>	—	100	200	μA	$\overline{CE} \geq V_{CC} - 0.2 V$ RFSH ≥ V <sub>CC</sub> - 0.2 V, Vin ≥ 0 V	1
			70	100	μA	$\overline{CE} \geq V_{CC} - 0.2 V$ RFSH ≥ V <sub>CC</sub> - 0.2 V, Vin ≥ 0 V	2
Operating power supply current in self refresh mode	I <sub>CC2</sub>	—	1	2	mA	$\overline{CE} = V_{IH}$ RFSH = V <sub>IL</sub> , Vin ≥ 0 V	1, 2
	I <sub>CC3</sub>	—	100	200	μA	$\overline{CE} \geq V_{CC} - 0.2 V$ RFSH ≤ 0.2 V, Vin ≥ 0 V	1
			70	100	μA	$\overline{CE} \geq V_{CC} - 0.2 V$ RFSH ≤ 0.2 V, Vin ≥ 0 V	2
Input leakage current	I <sub>LI</sub>	-10	—	10	μA	V <sub>CC</sub> = 5.5 V Vin = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	-10	—	10	μA	$\overline{OE} = V_{IH}$ V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA	
	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1 mA	

- Notes: 1. This characteristics is guaranteed only for L-version.  
2. This characteristics is guaranteed only for LL-version.

### Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	C <sub>in</sub>	—	8	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>I/O</sub>	—	10	pF	V <sub>I/O</sub> = 0 V

Note: This Parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ )

**Test Conditions**

- Input pulse levels: 2.4 V, 0.4 V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2 V, 0.8 V
- Reference level:  $V_{OH} = 2.0\text{ V}$ ,  $V_{OL} = 0.8\text{ V}$
- Output load: 1 TTL and 100 pF (including scope and jig)

		HM658128A							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Random read or write cycle time	$t_{RC}$	130	—	160	—	190	—	ns	
Random read-modify-write cycle time	$t_{RWC}$	190	—	220	—	260	—	ns	
Chip enable access time	$t_{CEA}$	—	80	—	100	—	120	ns	
Output enable access time	$t_{OEA}$	—	30	—	30	—	40	ns	
Chip disable to output in high-Z	$t_{CHZ}$	0	30	0	30	0	35	ns	1, 2
Chip enable to output in low-Z	$t_{CLZ}$	20	—	20	—	20	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	—	25	—	25	—	30	ns	1, 2
Output enable to output in low-Z	$t_{OLZ}$	0	—	0	—	0	—	ns	2
Chip enable pulse width	$t_{CE}$	80 n	10 $\mu$	100 n	10 $\mu$	120 n	10 $\mu$	s	
Chip enable precharge time	$t_P$	40	—	50	—	60	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	0	—	ns	
Address hold time	$t_{AH}$	30	—	30	—	35	—	ns	
Read command setup time	$t_{RCS}$	0	—	0	—	0	—	ns	
Read command hold time	$t_{RCH}$	0	—	0	—	0	—	ns	
$\overline{\text{RFSH}}$ hold time	$t_{RHC}$	15	—	15	—	15	—	ns	
$\overline{\text{RFSH}}$ delay time for standby	$t_{RCD}$	—	5	—	5	—	5	ns	10
Chip select setup time	$t_{CSS}$	0	—	0	—	0	—	ns	
Chip select hold time	$t_{CSH}$	30	—	30	—	35	—	ns	
Write command pulse width	$t_{WP}$	30	—	30	—	35	—	ns	
Chip enable to end of write	$t_{CW}$	80	—	100	—	120	—	ns	
Data in to end of write	$t_{DW}$	25	—	25	—	30	—	ns	
Data in hold time for write	$t_{DH}$	0	—	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	5	—	ns	2
Write to output in high-Z	$t_{WHZ}$	—	25	—	25	—	30	ns	1, 2
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	ns	6

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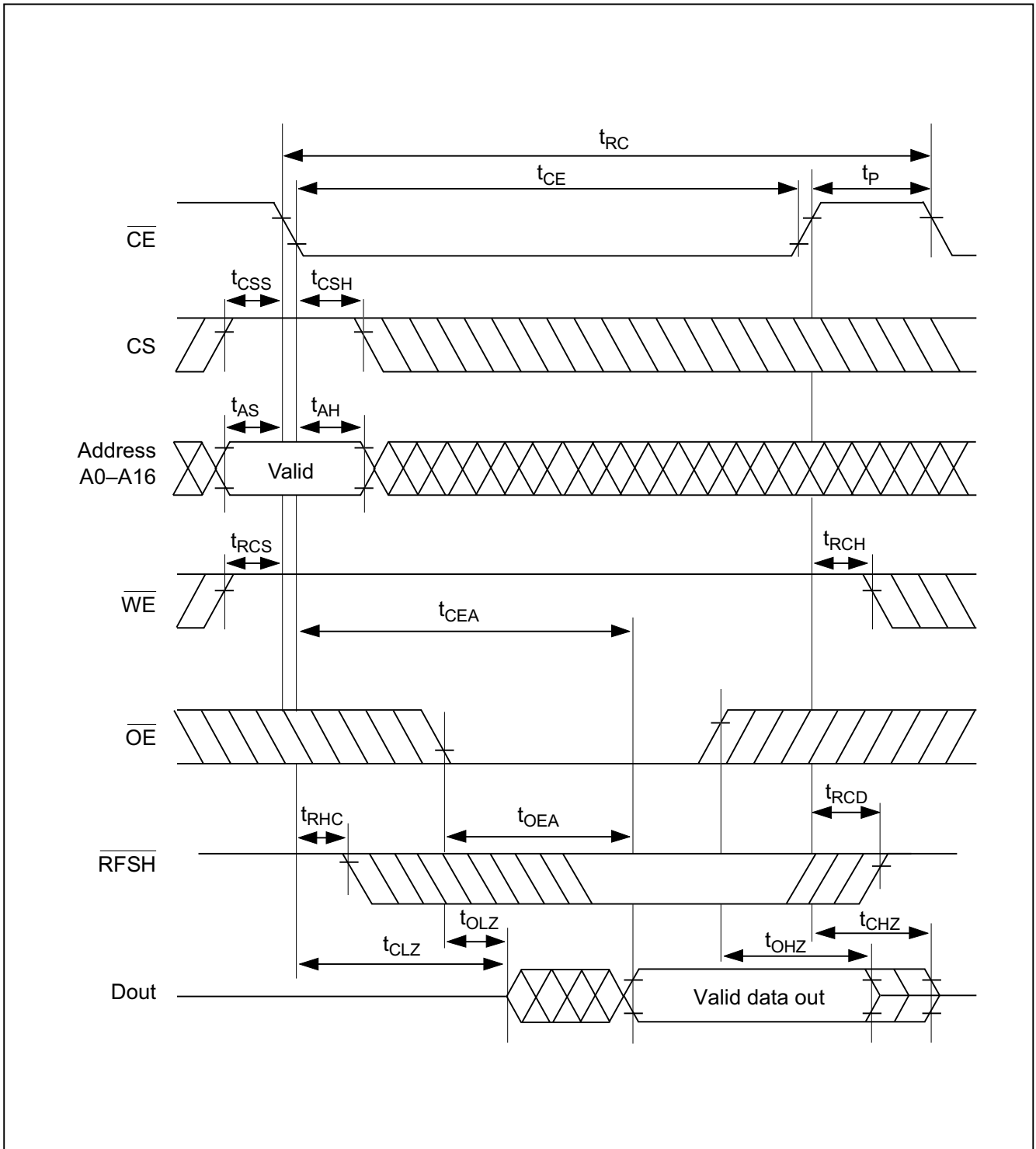
### AC Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 5\text{ V} \pm 10\%$ ) (cont)

Parameter	Symbol	HM658128A						Unit	Note
		-8		-10		-12			
		Min	Max	Min	Max	Min	Max		
Refresh command delay time	$t_{\text{RFD}}$	40	—	50	—	60	—	ns	
Refresh precharge time	$t_{\text{FP}}$	40	—	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	$t_{\text{FAP}}$	80 n	8 $\mu$	80 n	8 $\mu$	80 n	8 $\mu$	s	
Automatic refresh cycle time	$t_{\text{FC}}$	130	—	160	—	190	—	ns	
Refresh command pulse width for self refresh	$t_{\text{FAS}}$	8	—	8	—	8	—	$\mu\text{s}$	
Refresh reset time for self refresh	$t_{\text{RFS}}$	130	—	160	—	190	—	ns	
Refresh reset time for auto refresh	$t_{\text{RFA}}$	0	—	0	—	0	—	ns	
Refresh period (512 cycles)	$t_{\text{REF}}$	—	8	—	8	—	8	ms	

- Notes:
- $t_{\text{CHZ}}$ ,  $t_{\text{OHZ}}$  and  $t_{\text{WHZ}}$  are defined as the time at which the output achieves the open circuit conditions.
  - $t_{\text{CHZ}}$ ,  $t_{\text{CLZ}}$ ,  $t_{\text{OHZ}}$ ,  $t_{\text{OLZ}}$ ,  $t_{\text{WHZ}}$  and  $t_{\text{OW}}$  are sampled under the condition of  $t_{\text{T}} = 5\text{ ns}$  and not 100% tested.
  - A write occurs during the overlap of a low  $\overline{\text{CE}}$  and a low  $\overline{\text{WE}}$ . Write ends at the earlier of  $\overline{\text{WE}}$  going high or  $\overline{\text{CE}}$  going high.
  - If the  $\overline{\text{CE}}$  low transition occurs simultaneously with or latter from the  $\overline{\text{WE}}$  low transition, the output buffers remain in high impedance state.
  - In write cycle,  $\overline{\text{OE}}$  or  $\overline{\text{WE}}$  must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to  $\overline{\text{OE}}$  or  $\overline{\text{WE}}$  turning on output buffers.
  - Transition time  $t_{\text{T}}$  is measured between  $V_{\text{IH min}}$  and  $V_{\text{IL max}}$ .
  - After power-up, pause more than 100  $\mu\text{s}$  and execute at least 8 initialization cycles.
  - 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15  $\mu\text{s}$  after self refresh, in order to meet the refresh specification of 8 ms and 512 cycles.
  - At the end of self refresh, refresh reset time ( $t_{\text{RFS}}$ ) is required to reset the internal self refresh operation of the RAM. During  $t_{\text{RFS}}$ ,  $\overline{\text{CE}}$  and  $\overline{\text{RFSH}}$  must be kept high. If auto refresh follows self refresh, low transition of  $\overline{\text{RFSH}}$  at the beginning of auto refresh must not occur during  $t_{\text{RFS}}$  period.
  - If  $t_{\text{p}}$  is larger than 60 ns,  $t_{\text{RCD}}$  can be 8  $\mu\text{s}$  maximum.

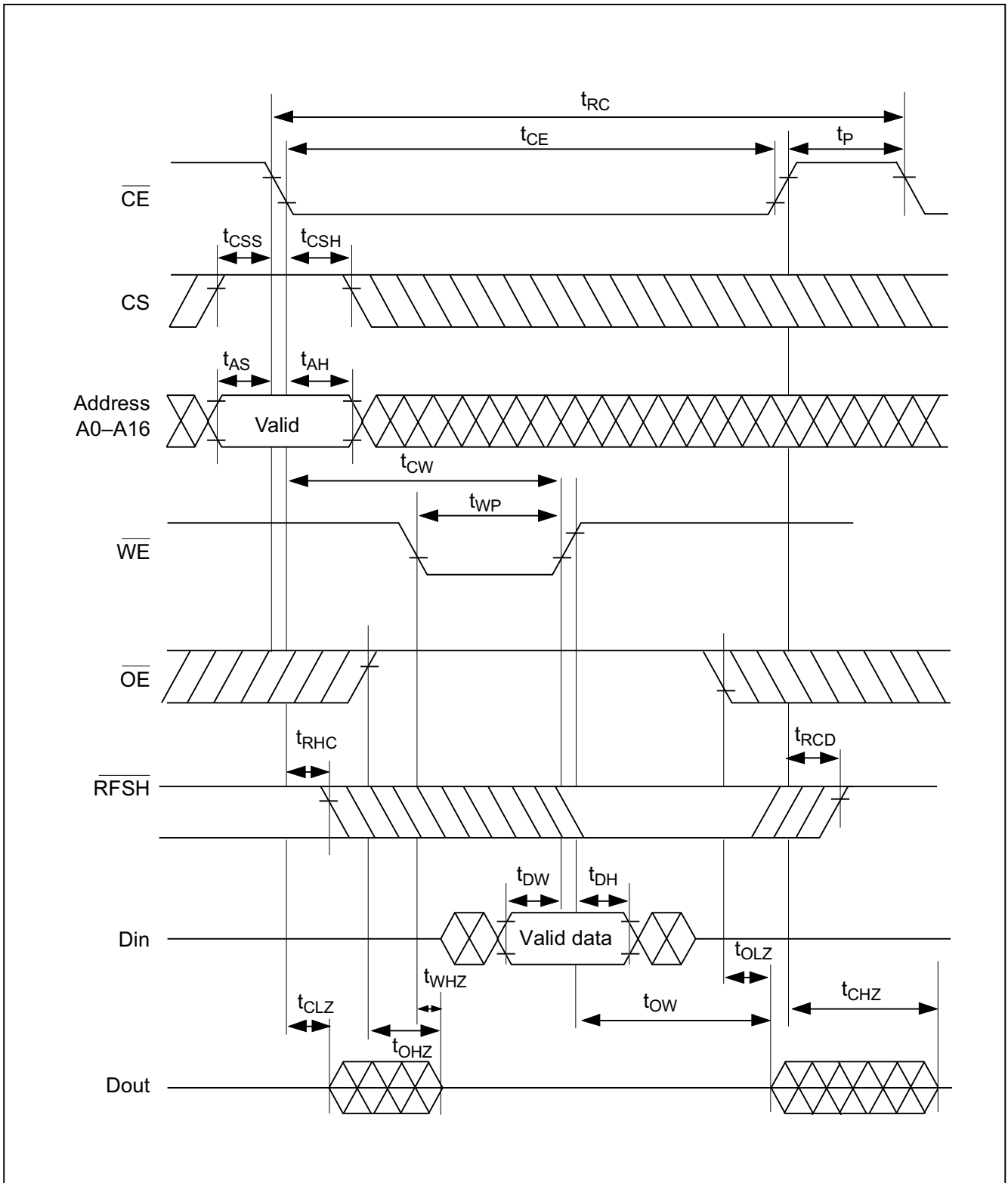
Timing Waveforms

Read Cycle

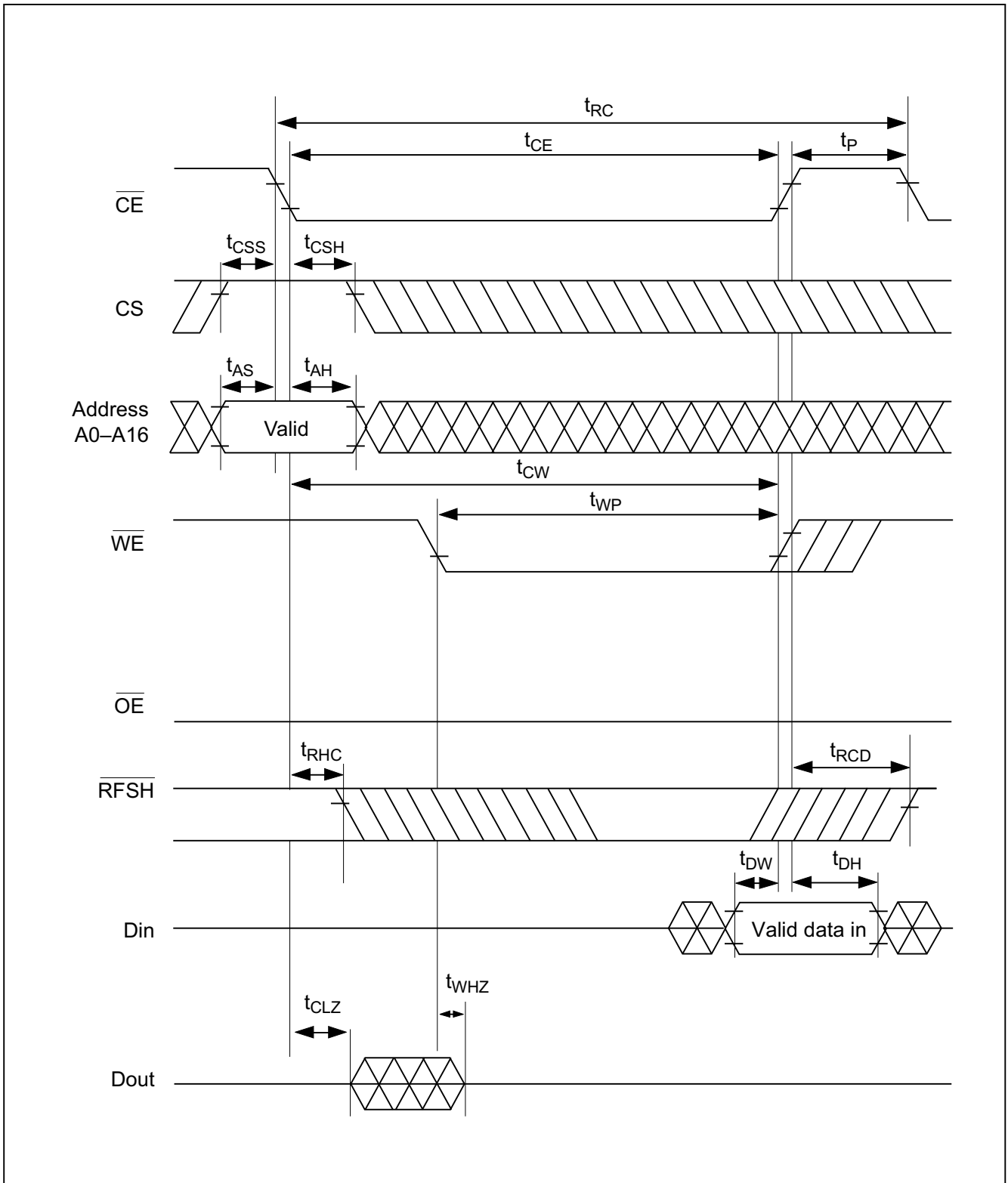


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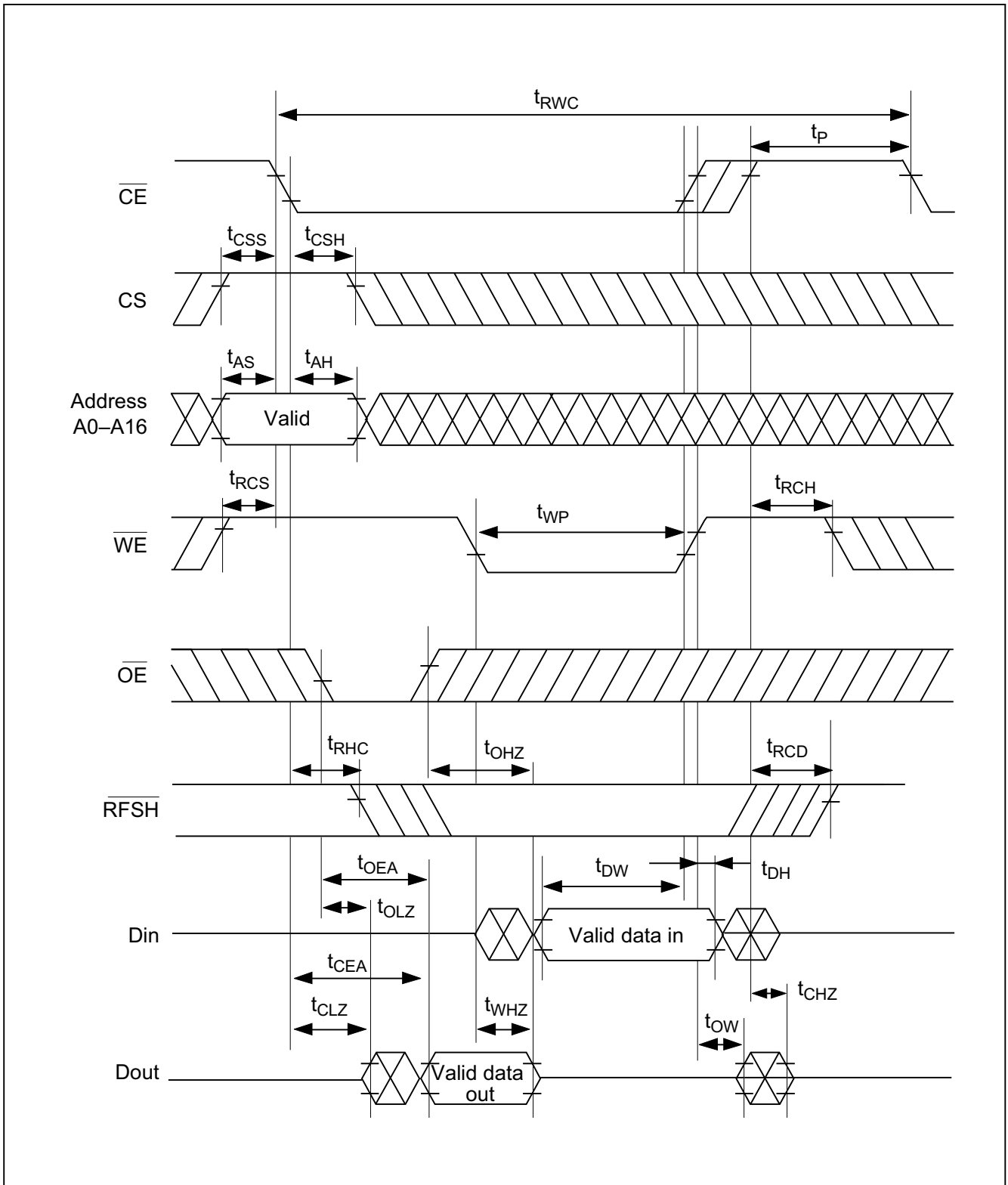
## Write Cycle 1 ( $\overline{OE}$ clock)



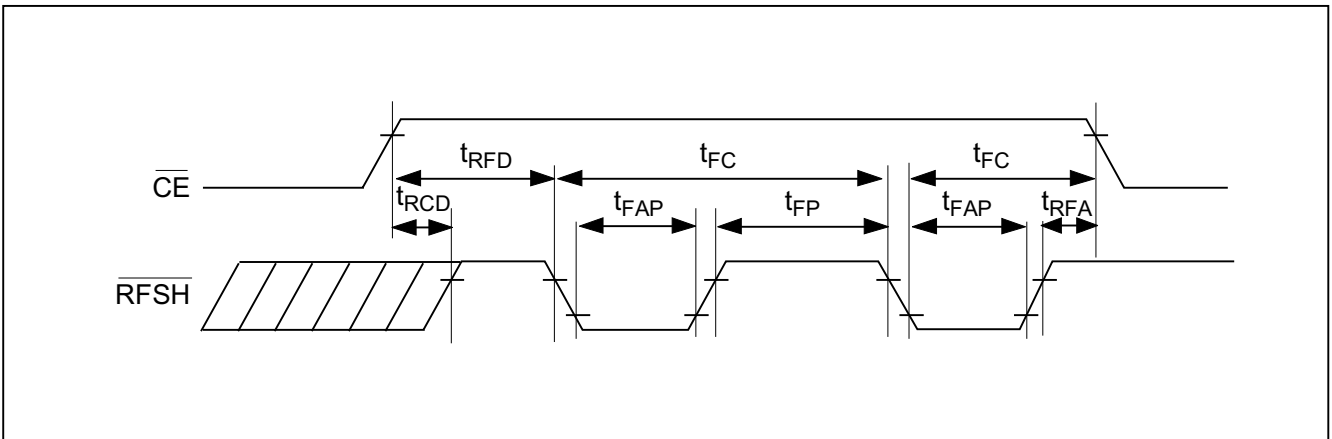
Write Cycle 2 ( $\overline{OE}$  Low Fix)



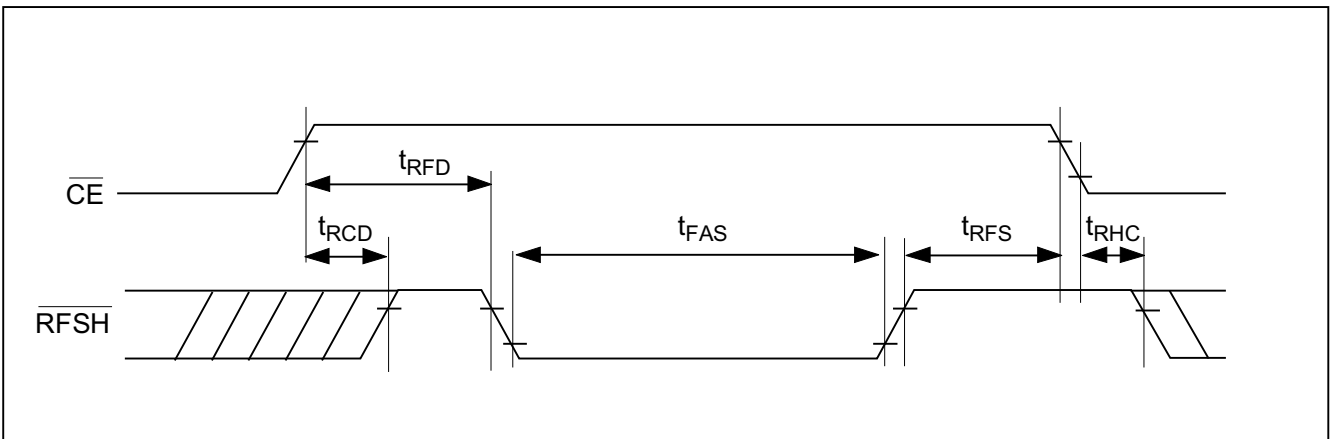
## Read-Modify-Write Cycle



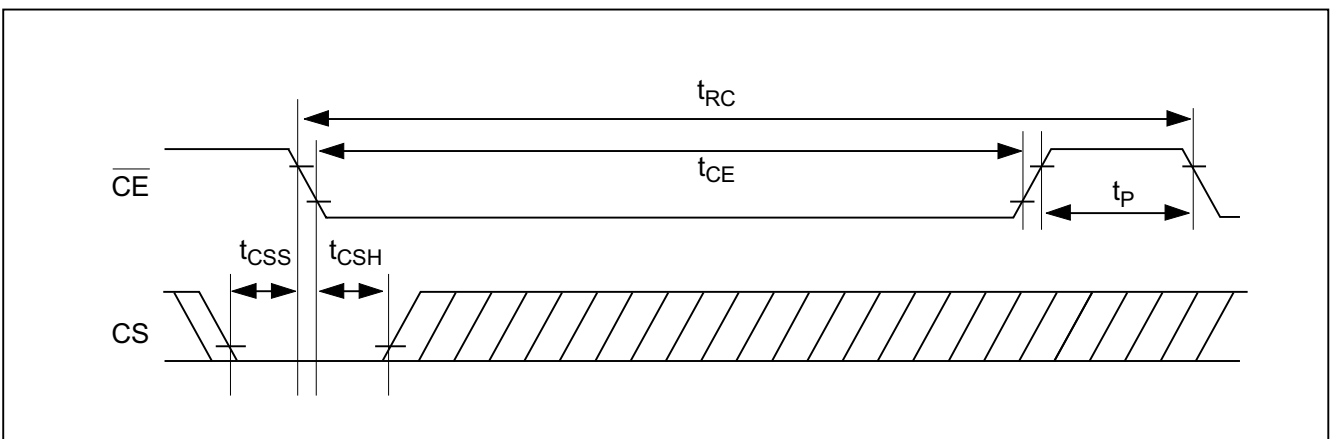
Auto Refresh Cycle



Self Refresh Cycle



CS Standby Mode

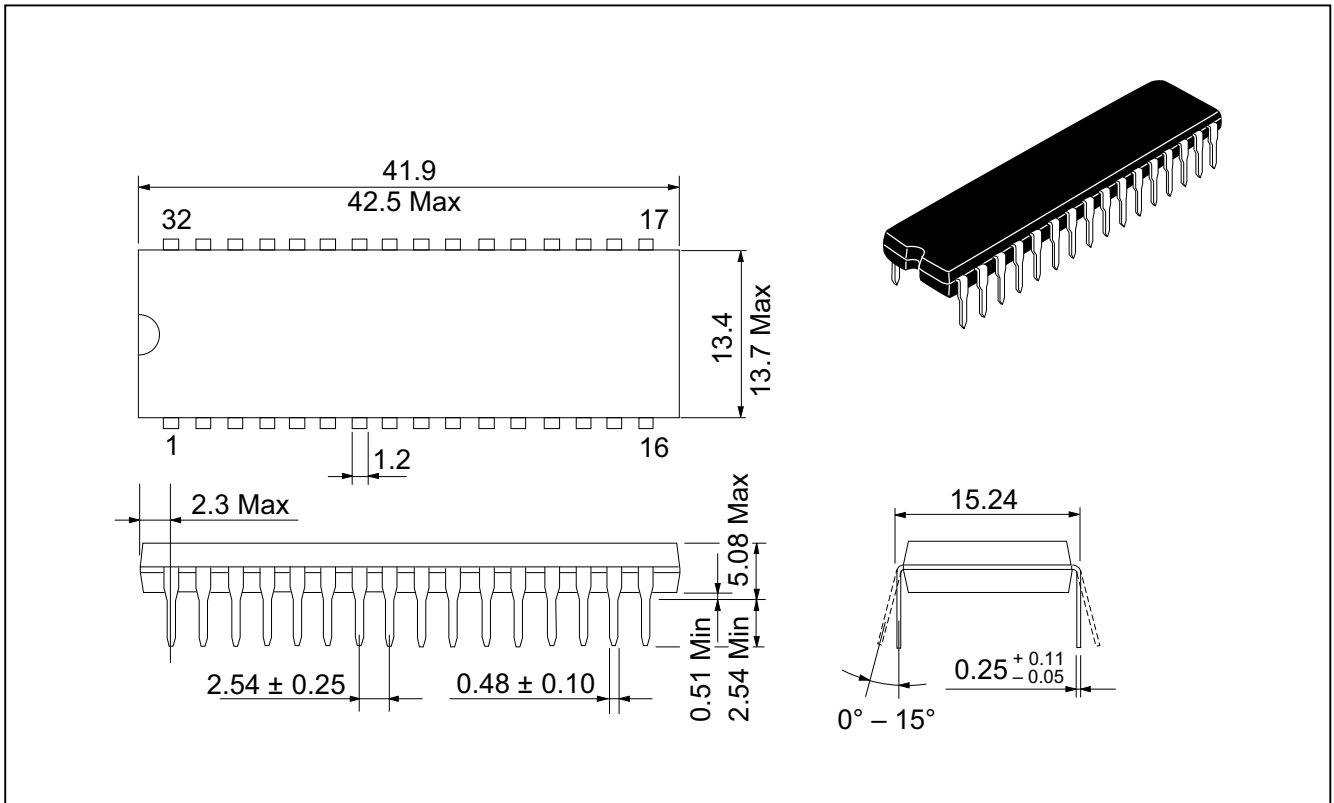


# HM658128A Series

## Package Dimensions

HM658128ALP Series (DP-32)

Unit: mm



HM658128ALFP Series (FP-32D)

Unit: mm

