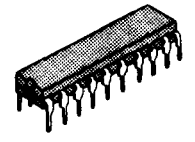
HM6167H-45, HM6167H-55, HM6167HP-45, HM6167HP-55

16384-word x 1-bit High Speed Static CMOS RAM

■ FEATURES

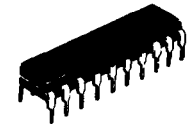
- Fast Access Time. . . . . .HM6167H/P-45 45ns (max)
  HM6167H/P-55 55ns (max)
- Low Power Standby and Low Power Operation
  Standby 100μW (typ), Operating 200mW (typ)
- Single +5V Supply and High Density 20 Pin Package
- Completely Static Memory . . . .No Clock nor Refresh Required
- Fully TTL Compatible . . . . . .All Inputs and Output
- Separate Data Input and Output. . . . . .Three State Output

HM6167H-45, HM6167H-55



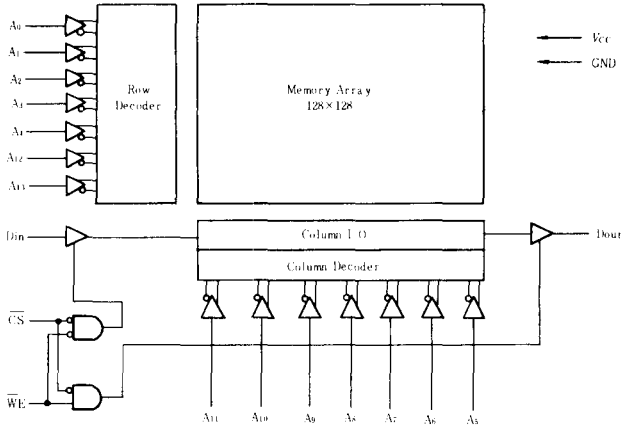
(DG-20)

HM6167HP-45, HM6167HP-55

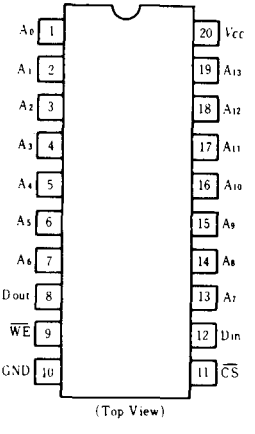


(DP-20)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (under bias)	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC: −0.5V

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−3.0*	–	0.8	V

* Pulse Width: 20ns, DC: V_{IL} (min) = −0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $Ta=0℃$ to $+70℃$)

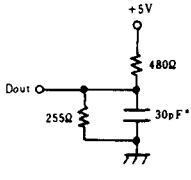
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI}\rvert$	$V_{CC}=5.5V$, $V_{IN}=0V\sim V_{CC}$	—	—	2	μA
Output Leakage Current	$\lvert I_{LO}\rvert$	$\overline{CS}=V_{IH}$, $V_{OUT}=0V\sim V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	40	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	10	20	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$ $V_{IN}\leqq 0.2V$ or $V_{IN}\geqq V_{CC}-0.2V$	—	0.02	2	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Note) Typical limits are at $V_{CC}=5.0V$, $Ta=25℃$ and specified loading.

■AC TEST CONDITIONS

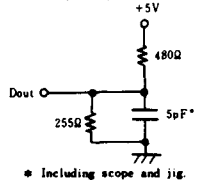
Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■CAPACITANCE ($Ta=25℃$, $f=1.0MHz$)

Item	Symbol	typ	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	$V_{IN}=0V$
Output Capacitance	C_{OUT}	5	7	pF	$V_{OUT}=0V$

Note) This parameter is sampled and not 100% tested.

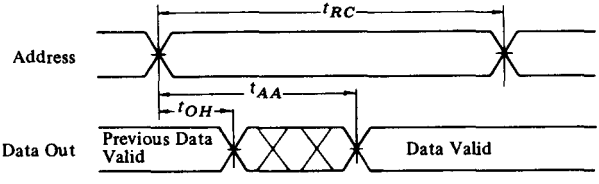
■AC CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0°C to 70°C, unless otherwise noted.)

●READ CYCLE

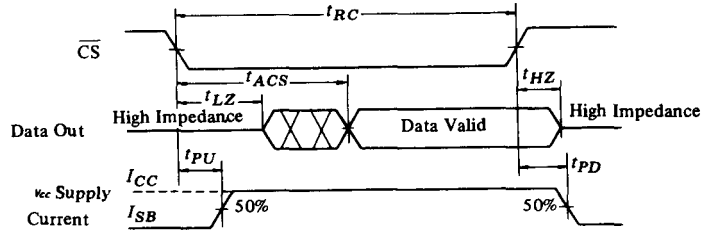
Item	Symbol	HM6167H/P-45		HM6167HP-55		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	ns	(1)
Address Access Time	t_{AA}	–	45	–	55	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	(2) (3) (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	(2) (3) (7)
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	ns	

NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

●TIMING WAVEFORM OF READ CYCLE NO.1 [4), 5)]



●TIMING WAVEFORM OF READ CYCLE NO.2 [4), 6)]

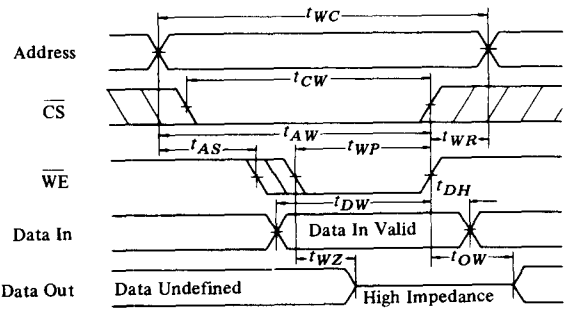


• WRITE CYCLE

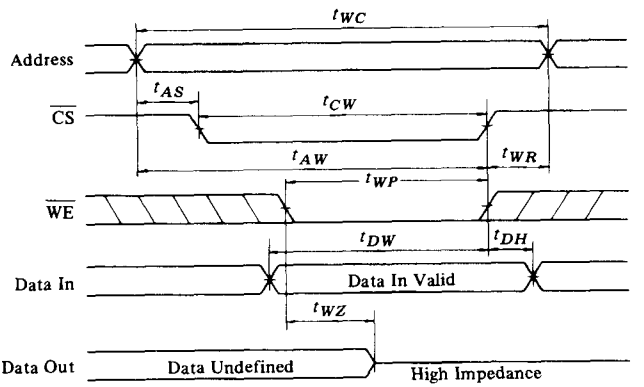
Item	Symbol	HM6167H/P-45		HM6167H/P-55		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	ns	(2)
Chip Selection to End of Write	t_{CW}	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	25	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	–	0	–	ns	(3) (4)

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

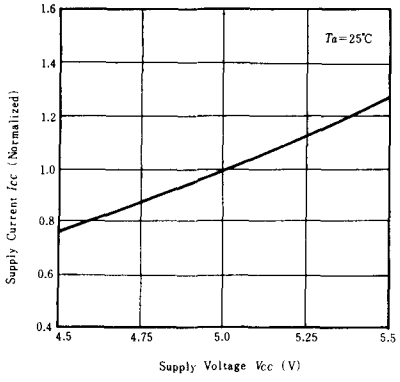
• TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



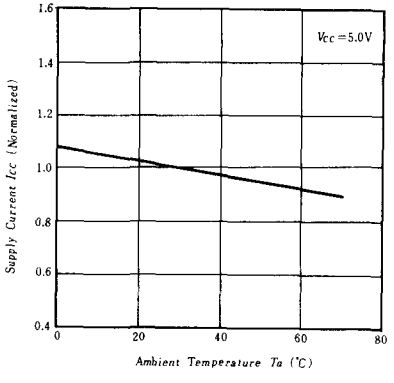
• TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



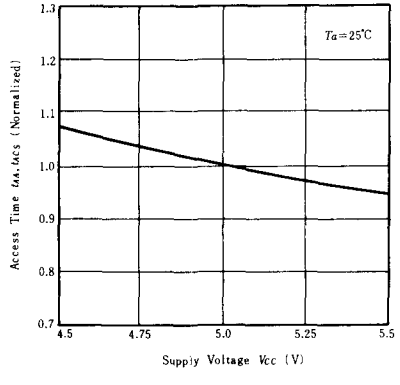
SUPPLY CURRENT vs. SUPPLY VOLTAGE



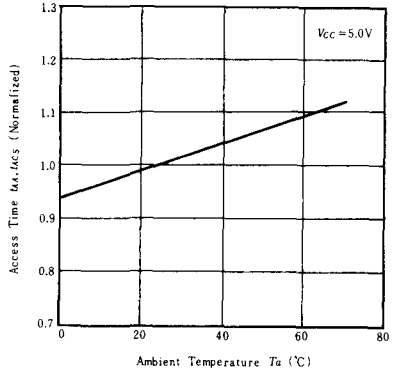
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



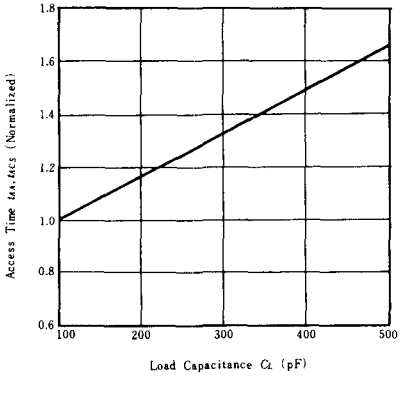
ACCESS TIME vs. SUPPLY VOLTAGE



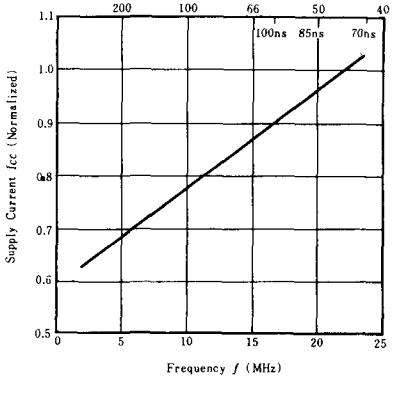
ACCESS TIME vs. AMBIENT TEMPERATURE



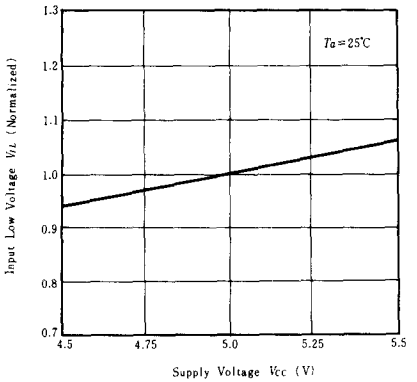
ACCESS TIME vs. LOAD CAPACITANCE



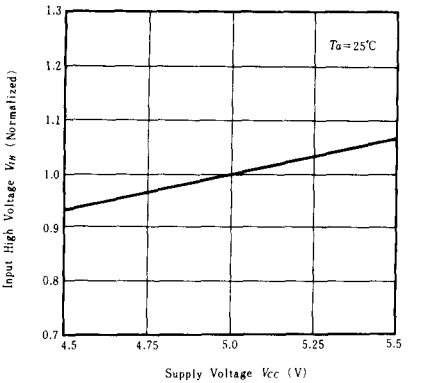
SUPPLY CURRENT vs. FREQUENCY



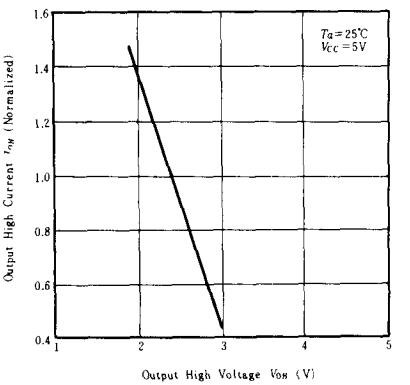
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



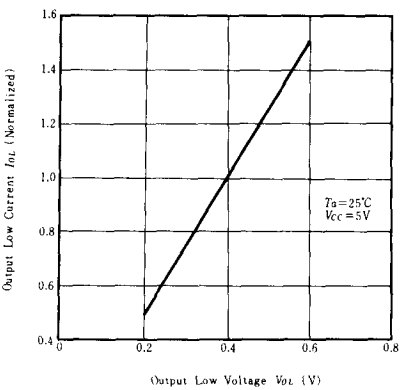
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



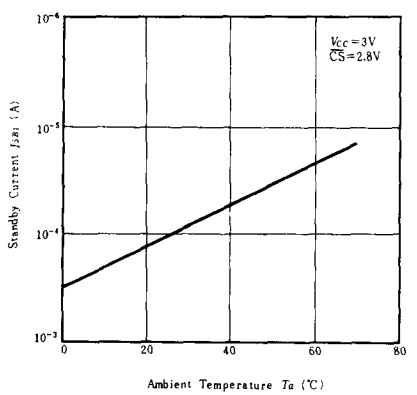
OUTPUT CURRENT vs. OUTPUT VOLTAGE



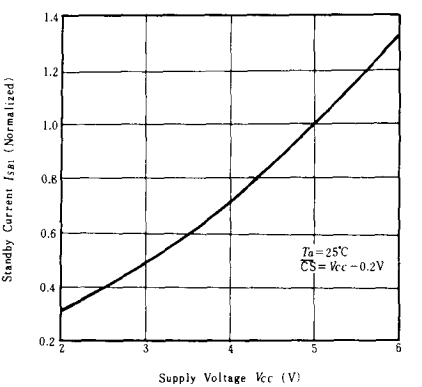
OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE