HEWLETT PACKARD

Wide Supply Voltage, High CMR, Hermetically Sealed Optocoupler

Technical Data

8 Pin Dual In-Line Package
- **HCPL-5200**
- **HCPL-5201 (883B)**
- **5962 8876801PC**
- **HCPL-5230**
- **HCPL-5231 (883B)**
- **5962 8876901PC**

20 Terminal Leadless Chip Carrier
- **HCPL-6230**
- **HCPL-6231 (883B)**

Features

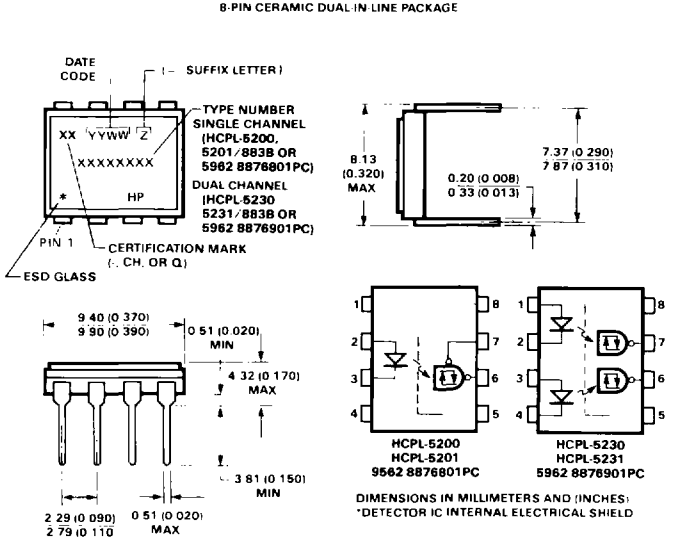
- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed Packages
- Performance Guaranteed over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- Wide V_{CC} Range (4.5 to 20 V)
- 300 ns Maximum Propagation Delay
- Compatible with LSTTL, TTL, and CMOS Logic
- High Common Mode Rejection – 1000 V/μs Guaranteed
- 1500 Vdc Withstand Test Voltage
- Three State Output Available
- HCPL-2200 Function Compatibility

Applications

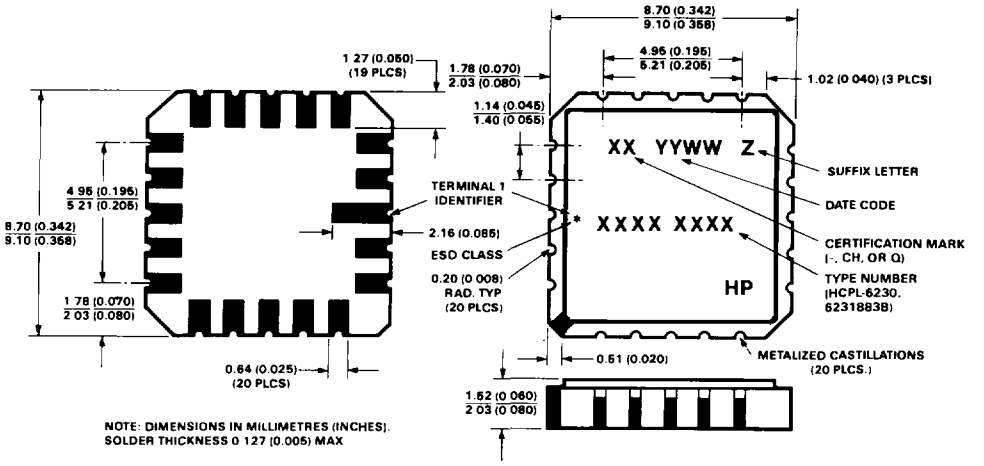
- Military/High Reliability Systems
- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Microprocessor System Interfaces
- Ground Loop Elimination
- Pulse Transformer Replacement
- Isolated Bus Driver (Single Channel)
- High Speed Line Receiver

Outline Drawings

8 PIN CERAMIC DUAL IN-LINE PACKAGE



20 TERMINAL CERAMIC LEADLESS CHIP CARRIER



Description

The HCPL-5200, HCPL-5201, and 5962 8876801PC are single channel, logic gate optocouplers. The HCPL-5230, HCPL-5231 and 5962 8876901PC are dual channel units made from the same chip sets. All six products are in eight pin hermetic dual in-line packages. These units are capable of operation and storage over the full military temperature ranges and can be purchased as either single or dual channel standard product (HCPL-5200 and HCPL-5230 respectively), with full MIL-STD-883 Class Level B testing (HCPL-5201 and HCPL-5231 respectively), or from the DESC Standard Military Drawings (SMDs) 5962-88768 and 5962-88769 as (5962 8876801PC or 5962 8876901PC respectively). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part #, or by adding option #200 to the part number for non-SMD parts.

The HCPL-6230 and HCPL-6231 parts are in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6230. The product with full MIL-STD-883 Class Level B testing is HCPL-6231. These dual channel devices are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold-plated terminals.

Each channel contains an AlGaAs light emitting diode optically coupled to an integrated high gain photon detector. The detector has a threshold with hysteresis. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter. The detector in the single channel units has a three state output stage which allows for direct connection to data buses. The detector IC has an electric shield that provides a guaranteed common mode transient immunity of 1,000 Volts/μsec. Improved power supply rejection eliminates the need for special power supply bypass precautions.

All devices are guaranteed to operate over a V_{CC} range of 4.5 Volts to 20 Volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS. Logic low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 100 nsec when used in the circuit of Figure 11.

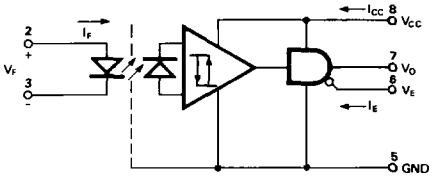
These units are useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

The test programs on the 5962 8876801PC and 5962 8876901PC are in compliance with DESC (SMDs) 5962-88768 and 5962-88769 respectively. The electrical characteristics table shows Group A Subgroup testing requirements from these drawings.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

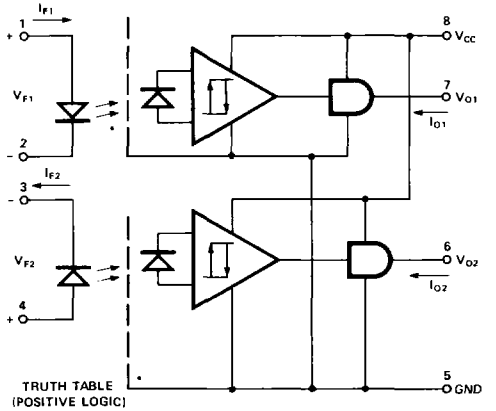
Schematics

8 PIN CERAMIC DIP SINGLE CHANNEL SCHEMATIC



DETECTOR IC INTERNAL ELECTRICAL SHIELD

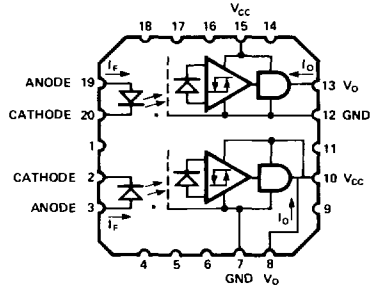
8 PIN CERAMIC DIP DUAL CHANNEL SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
H	H
L	L

20 TERMINAL CERAMIC LEADLESS CHIP CARRIER SCHEMATIC



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	OUTPUT
H	H
L	L

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Current (High)	$I_{F(ON)}$	2	8	mA
Input Voltage (Low)	$V_{F(OFF)}$	0	0.8	Volts
Fan Out	N		4	TTL Loads

Single Channel Product Only

Enable Voltage High	V_{EH}	2.0	20	Volts
Enable Voltage Low	V_{EL}	0	0.8	Volts

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Case Temperature – T_C ..... +170°C
Lead Solder Temperature ..... 260°C for 10 s
Junction Temperature (T_J) ..... +175°C
Average Forward Current – $I_{F\,AVG}$ ..... 8 mA
Peak Input Current – $I_{F\,PK}$ ..... 20 mA[1]
Reverse Input Voltage – V_R ..... 5 V
Supply Voltage – V_{CC} ..... -0.0 V min., 20 V max.
Average Output Current – I_O (per channel) ..... 15 mA
Output Voltage – V_O ..... -0.3 V min., 20 V max.
Total Package Power Dissipation – P_d (per channel) ..... 200 mW

Single Channel Product Only

Three State Enable Voltage – V_E ..... -0.3 V min., 20 V max.

Electrical Characteristics

T_A = -55°C to 125°C, unless otherwise specified. For 4.75 V ≤ V_{CC} ≤ 20 V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V

Parameter		Sym.	Test Conditions		Group A Subgroups[11]	Min.	Typ.*	Max.	Units	Fig.	Notes
Logic Low Output Voltage		V_{OL}	I_{OL} = 6.4 mA (4 TTL Loads)		1, 2, 3			0.5	Volts	1, 3	2
Logic High Output Voltage		V_{OH}	I_{OH} = -2.6 mA (**V_{OH} = V_{CC} - 2.1 V)		1, 2, 3	2.4	**		Volts	2, 3	2
			I_{OH} = -0.32 mA		NA		31		Volts		
Output Leakage Current (V_{OUT} > V_{CC})		I_{OHH}	V_O = 5.5 V	I_F = 8 mA, V_{CC} = 4.5 V	1, 2, 3			100	µA		2
			V_O = 20 V					500	µA		
Logic Low Supply Current	Single Channel (5962-88768)	I_{CCL}	V_{CC} = 5.5 V	V_F = 0 V, V_E = Don't Care	1, 2, 3		4.5	6.0	mA		
			V_{CC} = 20 V				5.3	7.5	mA		
	Dual Channel (5962-88769)		V_{CC} = 5.5 V	V_{F1} = V_{F2} = 0 V	1, 2, 3		9.0	12.0	mA		
			V_{CC} = 20 V				10.6	15	mA		
Logic High Supply Current	Single Channel (5962-88768)	I_{CCH}	V_{CC} = 5.5 V	I_F = 8 mA, V_E = Don't Care	1, 2, 3		2.9	4.5	mA		
			V_{CC} = 20 V				3.3	6.0	mA		
	Dual Channel (5962-88769)		V_{CC} = 5.5 V	I_{F1} = I_{F2} = 8 mA	1, 2, 3		5.8	9.0	mA		
			V_{CC} = 20 V				6.6	12.0	mA		
Logic Low Short Circuit Output Current		I_{OSL}	V_O = V_{CC} = 5.5 V	V_F = 0 V	1, 2, 3	20			mA		2, 3
			V_O = V_{CC} = 20 V			35			mA		
Logic High Short Circuit Output Current		I_{OSH}	V_{CC} = 5.5 V	I_F = 8 mA, V_O = GND	1, 2, 3			-10	mA		2, 3
			V_{CC} = 20 V					-25	mA		
Input Forward Voltage		V_F	I_F = 8 mA		1, 2, 3	1.0	1.3	1.8	Volts	4	2
Input Reverse Breakdown Voltage		V_R	I_R = 10 µA		1, 2, 3	3			Volts		2
Input-Output Insulation		I_{I-O}	45% RH, t = 5 s, V_{I-O} = 1500 Vdc		1			1	µA		4, 5
Propagation Delay Time to Logic Low Output Level		t_{PHL}			9, 10, 11		173	300	ns	5, 6,	2, 6
Propagation Delay Time to Logic High Output Level		t_{PLH}			9, 10, 11		118	300	ns	5, 6,	2, 6
Logic High Common Mode Transient Immunity		$\|CM_H\|$	I_F = 2 mA, V_{CM} = 50 V_{P-P}		9	1000	10,000		V/µs	9	2, 7
Logic Low Common Mode Transient Immunity		$\|CM_L\|$	I_F = 0 mA, V_{CM} = 50 V_{P-P}		9	1000	10,000		V/µs	9	2, 7

Electrical Characteristics Single Channel Product Only

T_A = -55°C to 125°C, unless otherwise specified.
For 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, 4.5 V ≤ V_{CC} ≤ 20 V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 2.0 V ≤ V_{EH} ≤ 20 V, 0 V ≤ V_{EL} ≤ 0.8 V unless otherwise specified.

Parameter	Sym.	Test Conditions		Group A Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
High Impedance State Output Current	I_{OZL}	V_O = 0.4 V	V_{EN} = 2 V, V_F = 0 V	1, 2, 3			-20	µA		
	I_{OZH}	V_O = 2.4 V	V_{EN} = 2 V, I_F = 8 mA	1, 2, 3			20	µA		
		V_O = 5.5 V					100	µA		
		V_O = 20 V					500	µA		
Logic High Enable Voltage	V_{EH}			1, 2, 3	2.0			Volts		
Logic Low Enable Voltage	V_{EL}			1, 2, 3			0.8	Volts		
Logic High Enable Current	I_{EH}	V_{EN} = 2.7 V		1, 2, 3			20	µA		
		V_{EN} = 5.5 V					100	µA		
		V_{EN} = 20 V				0.004	250	µA		
Logic Low Enable Current	I_{EL}	V_{EN} = 0.4 V		1, 2, 3			-0.32	mA		

*All typical values are at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 5 mA unless otherwise specified.

Typical Characteristics

All typical values are at V_{CC} = 5 V, T_A = 25°C), $I_{F(ON)}$ = 5 mA unless otherwise specified.

Parameter	Symbol	Test Conditions	Typ.	Units	Fig.	Notes
Input Current Hysteresis	I_{HYS}	V_{CC} = 5 V	0.07	mA	3	2
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	I_F = 8 mA	-1.25	mV/°C		2
Input-Output Resistance	R_{I-O}	V_{I-O} = 500 Vdc	10^{13}	Ω		2, 8
Input-Output Capacitance	C_{I-O}	f = 1 MHz	2.0	pF		2, 8
Input Capacitance	C_{IN}	f = 1 MHz, V_F = 0 V	20	pF		2, 10
Output Rise Time (10-90%)	t_r		45	ns	5, 7	2
Output Fall Time (90-10%)	t_f		10	ns	5, 7	2

Single Channel Product Only

Output Enable Time to Logic High	t_{PZH}		30	ns	8	
Output Enable Time to Logic Low	t_{PZL}		30	ns	8	
Output Disable Time from Logic High	t_{PHZ}		45	ns	8	
Output Disable Time from Logic Low	t_{PLZ}		55	ns	8	

Dual Channel Product Only

Input-Input Insulation Leakage Current	I_{I-I}	45% Relative Humidity, V_{I-I} = 500 Vdc, T_A = 25°C, t = 5 s	0.5	nA		9
Resistance (Input-Input)	R_{I-I}	V_{I-I} = 500 Vdc	10^{13}	Ω		9
Capacitance (Input-Input)	C_{I-I}	f = 1 MHz	1.5	pF		9

Notes:

1. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
2. Each channel.
3. Duration of output short circuit time not to exceed 10 ms.
4. Device considered a two terminal device: for 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
5. This is a momentary withstand test, not an operating condition.
6. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
8. Measured between each input pair shorted together and all outputs for that channel shorted together.
9. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
10. Zero-bias capacitance measured between the LED anode and cathode.
11. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and −55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

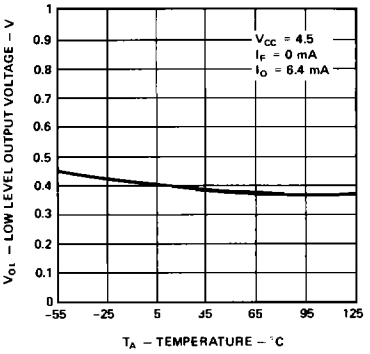


Figure 1. Typical Logic Low Output Voltage vs. Temperature

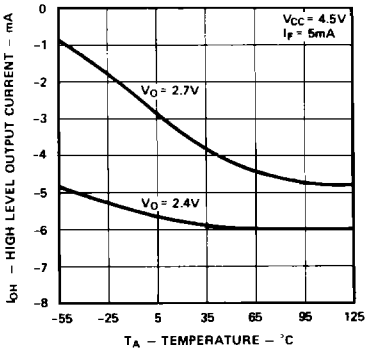


Figure 2. Typical Logic High Output Current vs. Temperature

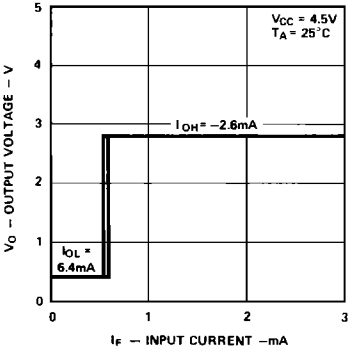


Figure 3. Output Voltage vs. Forward Input Current

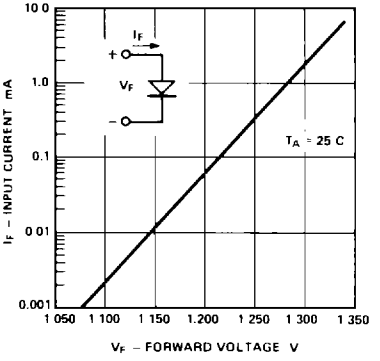


Figure 4. Typical Diode Input Forward Characteristic

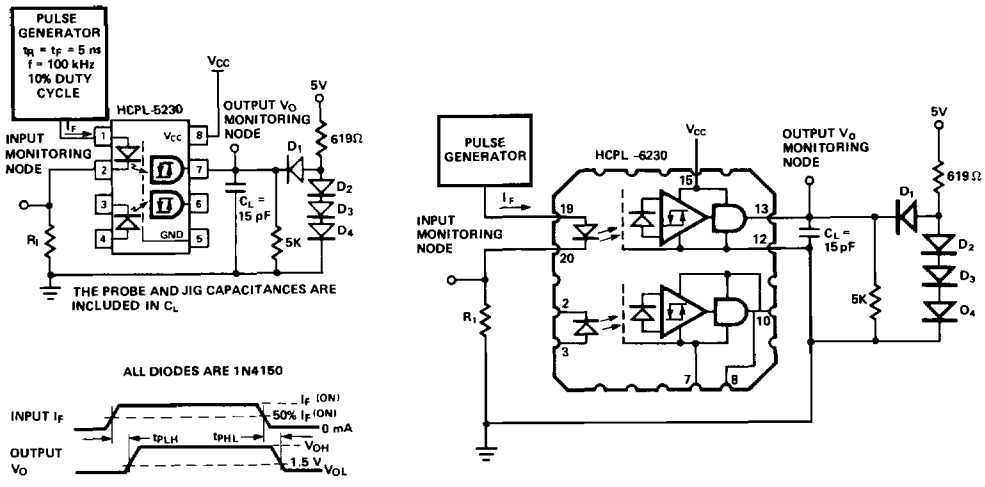


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

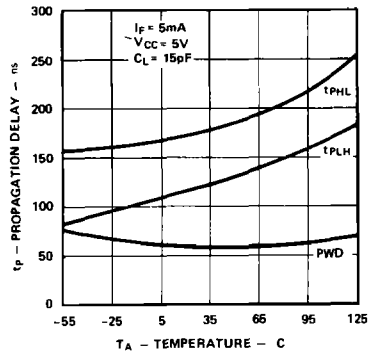


Figure 6. Typical Propagation Delay vs. Temperature

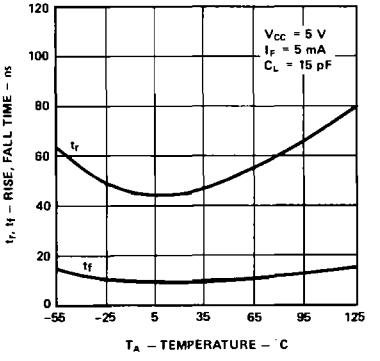


Figure 7. Typical Rise, Fall Time vs. Temperature

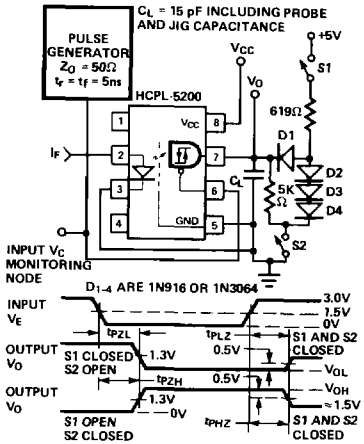


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

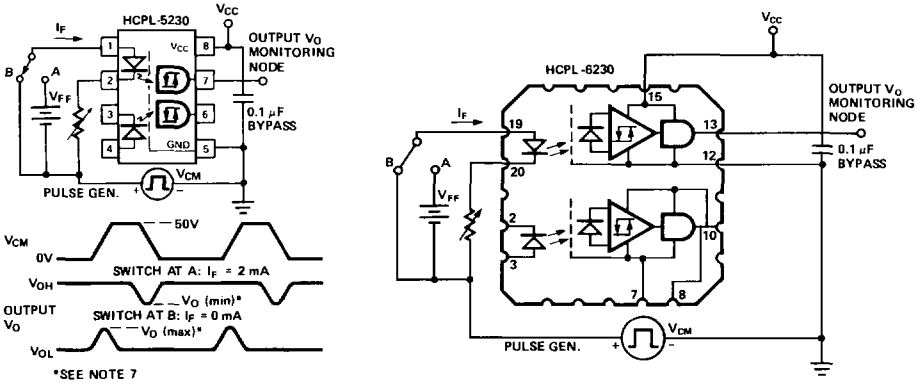


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

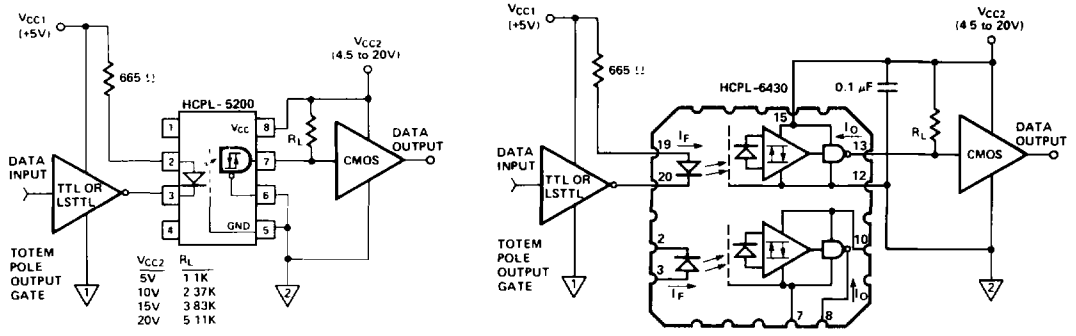


Figure 10. LSTTL to CMOS Interface Circuit.

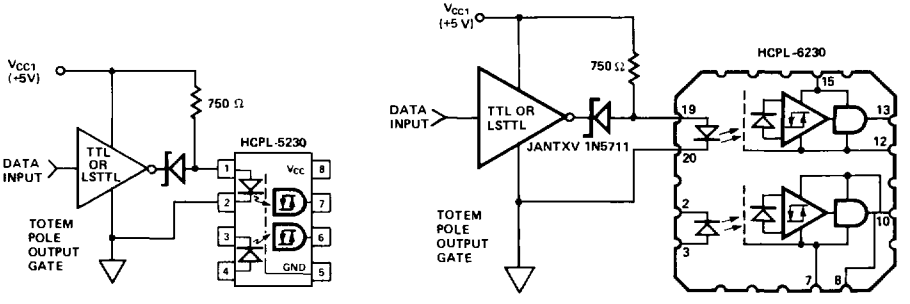


Figure 11. Recommended LED Drive Circuit.

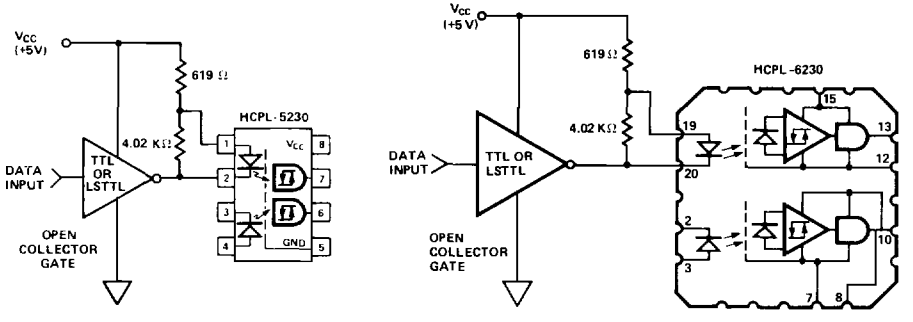


Figure 12. Series LED Drive with Open Collector Gate (4.02 kΩ Resistor Shunts I_{OH} from the LED)

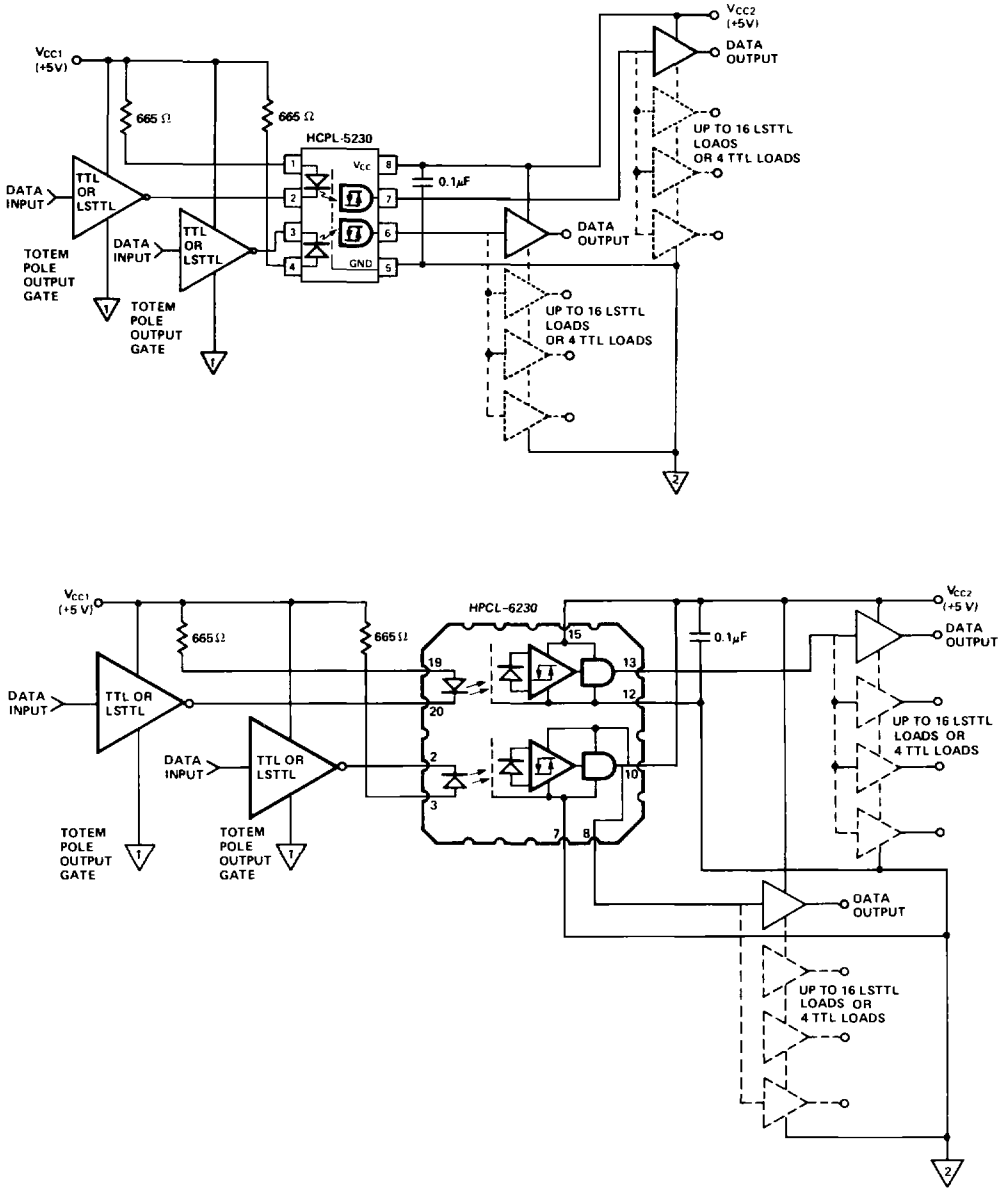


Figure 13. Recommended LSTTL to LSTTL Circuit

Part Numbering System

Commercial Product	Class B Product	SMD Product
HCPL-5200	HCPL-5201	5962 8876801PC
HCPL-5230	HCPL-5231	5962 8876901PC
HCPL-6230	HCPL-6231	By Request

SMD 5962 8876801PC, SMD 5962 8876901PC, and MIL-STD-883 Class B Test Program

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC SMD 5962-88768 for an H.P. Optocoupler from the same generic family using the same manufacturing process, design rules and elements of the same microcircuit group.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.
Group A–See Electrical Characteristics Table.
Group B–No change.
Group C–No change.
Group D–Constant Acceleration – Condition A not E.

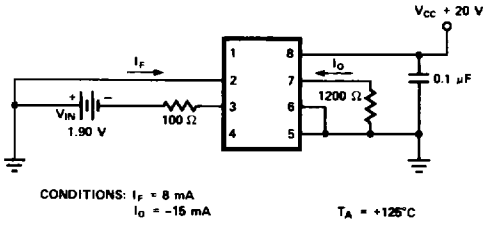


Figure 14. Single Channel Operating Circuit for Burn-in and Steady State Life Tests

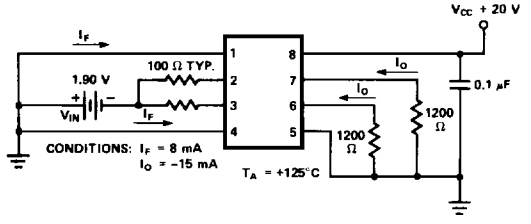


Figure 15. Dual Channel Operating Circuit for Burn-in and Steady State Life Tests

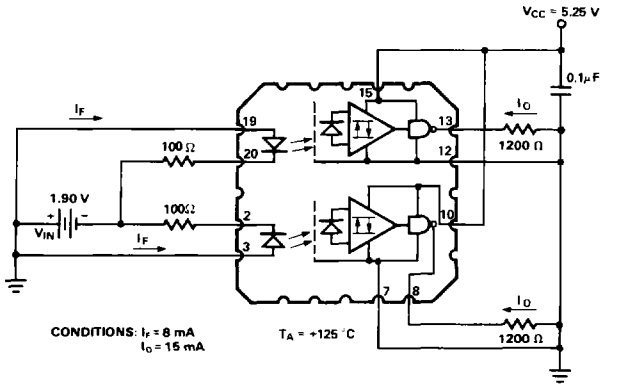


Figure 16. Operating Circuit for Burn-In and Steady State Life Tests