SEPTEMBER 1988

DATA SHEET HC-55421

X21 CONTROLLER

FEATURES

- COMPATIBLE WITH CCITT X21 (1984)
- 8 BIT DATA BUS
- 3 INTERRUPT SOURCES
- TRANSPARENT SERIAL INTERFACE
- PARITY CHECK, INVALID STATE CHECK
- FILTERING OF REPETITIVE CHARACTERS
- RECEIVE FIFO (2 CHARACTERS)
- INTERNAL OR EXTERNAL BYTE CLOCK
- OPERATION UP TO 2MBITS/S
- LOW POWER CMOS (40 mW)

DESCRIPTION

The X21 communication controller is a microprocessor peripheral device. It supports the low level tasks regarding supervision of the X21 interface, protocol handling and data integrity checking being ensured by the microprocessor.

The circuit has an internal 8 bit architecture and allows direct memory access for high speed transfers. Data exchange can also occur through a fully transparent serial interface.

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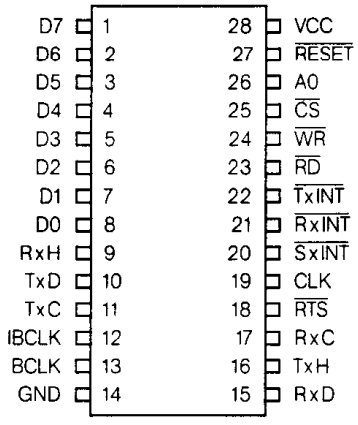
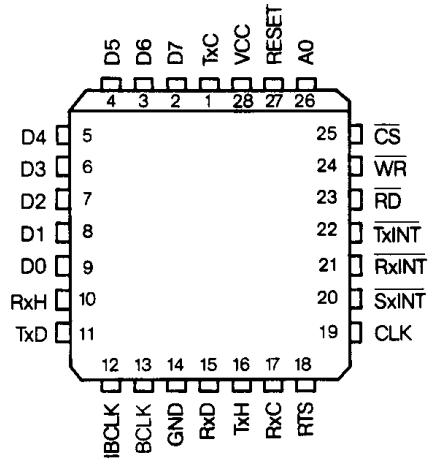
APPLICATIONS

Application field includes video, voice or data transmission on circuit switched data networks and terminal adaptors (TA's) for ISDN (S interface - CCITT X30).

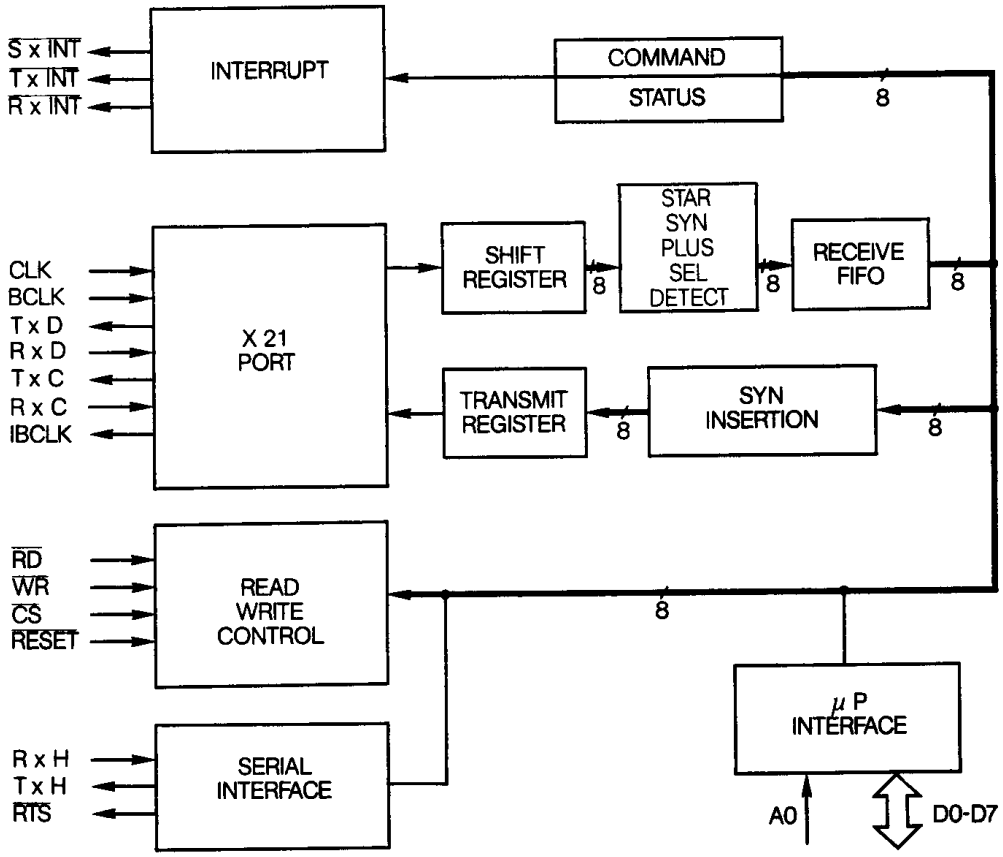
Pin Configurations



PLCC 28 pins (preliminary)



Block Diagram



SYMBOL	PIN N°	TYPE	NAME AND FUNCTION (DIL PACKAGE)
D7-D0	1-8	I/O	Data bus: the data bus lines are bidirectional three-state lines which interface with the system data bus.
A0	26	I	Data/register select (see *table 1*) – A0 = 0 → the command or status register is addressed. – A0 = 1 → the transmit or receive register is addressed.
RD	23	I	Read: Read controls a data or status byte transfer from the controller of the CPU.
WR	24	I	Write: Write controls a data or command byte transfer from the CPU to the controller.
CS	25	I	Chip select: this signal selects the controller and enables reading from or writing into its registers.
Tx D	10	O	Transmitter data (X21 port): Lead "T" seen from the DTE* side. Lead "R" seen from the DCE* side.
Tx C	11	O	Transmitter control (X21 port): Lead "C" seen from the DTE side. Lead "I" seen from the DCE* side.
Rx D	15	I	Receiver data (X21 port): Lead "R" seen from the DTE* side. Lead "T" seen from the DCE* side.
Rx C	17	I	Receiver control (X21 port): Lead "I" seen from the DTE* side. Lead "C" seen from the DCE* side.
CLK	19	I	Clock (X21 port): Lead "S" of the X21 interface.
IBCLK	12	O	Internal byte clock: substitue for BCLK to synchronize the transmit data.
BCLK	13	I	Byte clock (X21 port): this clock is optional (Lead "B").
Tx H	16	O	Transmitter data: this output transmits data on a serial interface.
Rx H	9	I	Receiver data: this input receives data from a serial interface.
$\overline{RTS}$	18	O	Request to send: this output signals that the circuit is ready to transmit data.
$\overline{Rx\ INT}$	21	O (1)	Receiver interrupt: this output indicates that one character is present in the receive register (SR2 = 1).
$\overline{Tx\ INT}$	22	O (1)	Transmitter interrupt: this output indicates that the transmit register is empty (SR7 = 1).
$\overline{Sx\ INT}$	20	O (1)	Status interrupt: this output indicates a change in the status register contents.
$\overline{RESET}$	27	I	Reset: used to reset all internal registers.
VCC	28		Positive supply (+ 5V).
GND	14		Ground: 0V.

*DTE = Data Terminal Equipment.
*DCE = Data Circuit terminating Equipment.

(1) Open drain

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION:

The MHS X21 controller is a microcomputer peripheral device which supports the CCITT X21 communication protocol (1984).

This controller relieves the microprocessor from low level tasks associated with X21 call set-up and data transfers, thus reducing CPU software and component count.

Data can be sent to a 8 bit microprocessor or to synchronous serial data controllers including those conforming to HDLC. Data rate can reach 2Mbits/s. The HC 55421 ensures call set-up and status change detection. Protocol handling and data integrity checking is done by the CPU.

X21 PROTOCOL

The X21 protocol is based on handshaking with acknowledgement: when a terminal issues a status change to a slave station, the slave must respond before the terminal issues another status change. The HC 55421 works equally on the data terminal equipment (DTE) side or on the data circuit terminating equipement (DCE) side.

As shown in *fig. 1*, the X21 physical interface consists of 2 data lines (T and R), 2 control lines (C and I), one data clock (S) and one optional byte clock (B). The byte clock can be generated by the HC 55421.

MICROPROCESSOR INTERFACE

The exchanges between the controller and the microprocessor system interface can be interrupt driven or direct memory access (DMA) driven.

The basic elements involved in these transfers are the following:

- 3 interrupt lines: $\overline{S \times INT}$, $\overline{T \times INT}$ and $\overline{R \times INT}$.
- Command and status registers which can be directly addressed by the CPU.
- Transmit and receive data registers.

The access to the registers is monitored via input $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and A0.

When A0 = 0, the command ($\overline{WR} = 0$) or status ($\overline{RD} = 0$) register is addressed.

A0 = 1 enables the access to the transmit ($\overline{WR} = 0$) or receive ($\overline{RD} = 0$) data register.

A read or write operation to or from any register is enabled by the $\overline{CS}$ pin ($\overline{CS} = 0$).

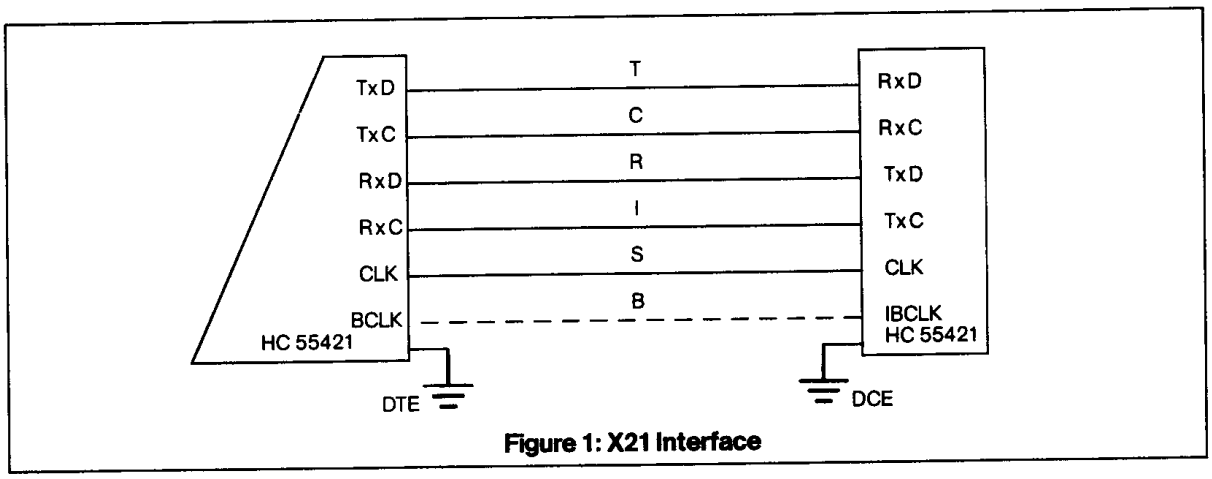


Figure 1: X21 Interface

A0	$\overline{RD}$	$\overline{WR}$	Data	Addressed Register
0	1	0	D0/D7	COMMAND
	0	1		STATUS
1	1	0		TRANS DAT
	0	1		RECV DAT

Table 1: Register Select Decoding

INTERNAL REGISTERS

The circuit works under CPU control by means of 4 registers:

- Command register (CR).
- Status register (SR).
- Transmit data register (TR).
- Receive data register (RR).

	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
0	µP INTERFACE	DISABLE $\overline{R \times INT}$	DISABLE $\overline{T \times INT}$	DISABLE $\overline{S \times INT}$	IBCLK	–	T x C=0	–
1	SERIAL INTERFACE	ENABLE $\overline{R \times INT}$	ENABLE $\overline{T \times INT}$	ENABLE $\overline{S \times INT}$	BCLK	RESET	T x C=1	LOOP MODE

Table 2: Commande Register Set-up

*Command register

The command register is reset to 0 by the external $\overline{RESET}$ signal.

CR0 : Setting this bit to 1 produces a continuous transmission of the transmit register character.

CR1 : This bit directly drives the T x C control line.

CR2 : The circuit is reset when this bit is set to 1. CR2 must be held to 0 to allow the circuit to restart.

CR3 : When CR3=1, the transmit sync. clock out cf pin 12 is BCLK.
When CR3=0, IBCLK is provided instead.

CR4 : Setting this bit to 1 enables a status change interrupt $\overline{S \times INT}$.

CR5 : Setting this bit to 1 enables a transmit interrupt $\overline{T \times INT}$.

CR6 : Setting this bit to 1 enables a receive interrupt $\overline{R \times INT}$.

CR7 : CR7=1 indicates that synchronous serial data transmission is achieved through the serial interface.
CR7 = 0 indicates that data are transferred through the µP interface.

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	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
0	-	-	-	-	-	RR EMPTY	-	R x C=0
1	TR EMPTY	RR OVERLOAD	ERROR R x D	PARITY ERROR R x D	ERROR R x C	ONE CHARACTER RR	STATUS CHANGE	R x C=1

Table 3: Status Register set-up

***Status register**

The status register is cleared the external $\overline{\text{RESET}}$ line.

The bits of the status register are set independently of the state of the command register bits and in particular the interrupt bits (CR4 to CR6).

SR0 : This bit indicates the status of the R x C control line, after a stable state has been detected on this wire.

SR1 : This bit is set to 1 after detection of a status change on R x D or R x C.

SR2 : When the receive FIFO contains at least one character, this bit is set to 1. SR2 is cleared after the received character(s) has (have) been acquired.

SR3 : Set to 1 when an error is detected on the R x C input, namely when a non stable state lasts more than 24 "S" clock cycles.

SR4 : Set to 1 after a parity error detection on R x D, in synchronous mode (error=even parity).

SR5 : Set to 1 after an error detection on R x D input. This means that during more than 24 "S" clock cycles, the R x D wire is not in a stable state (00, FF, AA, 0F or 33) in asynchronous mode.

In synchronous mode, SR5 = 1 when the received characters are not aligned with byte boundaries.

SR6 : This bit indicates an overload of the receive data register (RR) and that one character or more has been lost (SR6 = 1).

SR7 : When the transmit data register (TR) is empty, this bit is set to 1.

The error bits (SR3, SR4, SR5 and SR6), and bit SR1 are cleared whenever the status register is read.

***Transmit and receive data registers**

The transmit register (TR) and receive (RR) can be read or written by the microprocessor or by a DMA. In that mode, interrupts $\overline{\text{T x INT}}$ and $\overline{\text{R x INT}}$ are used as DMA requests.

In microprocessor mode, the µP data transfers are controlled by $\overline{\text{T x INT}}$ and $\overline{\text{R x INT}}$. These interrupts are activated by the status bits SR7 and SR2. *(See paragraph "INTERRUPTIONS").*

X21 INTERFACE

***Receive operation**

All status changes occuring on wires R x D and R x C are detected and processed by the HC 55421.

• Control Line

When the circuit senses a stable state ("0" or "1") during 16 clock periods on wire R x C, a status change interrupt ($\overline{\text{S x INT}}$) is created, and bit SR0 from the status register stores the value of R x C.

If no stable state has been detected during 24 clock cycles, bit SR3 indicates an error and a status interrupt ($\overline{\text{S x INT}}$) is created. Reading the status register clear the error condition.

• Data line

– Asynchronous mode:

When the circuit senses a stable state (00, FF, AA, 0F or 33) during 16 periods on wire R x D, a status change interrupt ($\overline{S \times INT}$) is sent, and the detected value is written into the receive data register.

If no stable state has been detected during 24 clock cycles, bit SR5 shows an error and a $\overline{S \times INT}$ is created. This error is cleared when reading the status register.

– Synchronous mode:

The circuit will switch from asychronous to synchronous mode after detection of two following "SYN" (16) characters. At the same time, a byte sync. clock is generated, and the received characters are compared with characters "PLUS", "BEL", "SYN" and "*".

Going from asynchronous to synchronous mode does not generates an "$\overline{S \times INT}$" interruption.

Characters "SYN" are ignored. They are not loaded into the receive register (RR).

The first character "BEL", "PLUS" or "*" is transferred into register RR and generates a Receive Interrupt $\overline{R \times INT}$.

Following "BEL", "PLUS" or "*" characters are ignored.

In synchronous mode, all characters different from "*", "PLUS", "BEL" and "SYN" are loaded into the receive register and a receive interrupt $\overline{R \times INT}$ is sent.

When the circuit detects a stable state (00, FF, AA, 0F or 33) during 16 bit clock periods, it switches from synchronous to asynchronous mode and sends a status interrupt $\overline{S \times INT}$. The character corresponding to this stable states is loaded into the receive register (RR). The last receive character, corresponding to the first 8 bit clock periods of the stable state has to be ignored.

• Parity check

In synchronous mode, the circuit conforms to X21 specification and checks that the received parity is odd.

Mode	Symbol	Hexadecimal mode
Asynchronous	0	00
	1	FF
	10	AA
		0F
		33
Synchronous	SYN	16
	PLUS	AB
	BEL	07
	*	2A
	OTHER	Code AI5

Table 4: Synchronous/asynchronous modes

Whenever a parity error is detected, bit SR4 (parity error) and SR1 are set in the status register. This will also generate a $\overline{S \times INT}$ (depending on the state of bit CR4). However, the parity error is pointed out after reception of the character following the erroneous character.

Switching from synchronous to asynchronous mode does not generate a parity error.

• Transmit operation

Control line

Bit CR1 from the command register directly controls the status of output T x C.

• Data line

Synchronous data including characters "SYN", "*", "PLUS" and "BEL" are sent out from output T x D. The data are synchronous with BCLK, or with the internal byte clock IBCLK if BCLK is not used. The byte clock is selected through bit CR3.

Bits CR0 and CR7 both control the T x D output according to *table 5*.

CR7 serial mode	CR0 loop mode	Transmit operation
0	0	The circuit sends the character contained in the transmit register. If (TR) is empty, a $\overline{T \times INT}$ is generated, and a "SYN" character is sent.
0	1	The transmit register character is continuously sent to the line. A transmit interruption $\overline{T \times INT}$ is not generated.
1	X	The circuit sends the data received on input R x H from the serial port.

Table 5: Transmit modes

SERIAL MODE

Data can be exchanged through a µP bus, or through a synchronous serial data link in transparent mode. The µP mode is normally used for communication set-up and termination and the transparent mode for the data-transfer (state 5 of X21 spec.).

The serial mode is selected by setting CR7 = 1. This also drives output $\overline{RTS}$ to 0. The internal data paths are from input R x H to output T x D and from input R x D output T x H.

Note also that when CR7 = 0, output T x H = 1.

This mode allows an easy implementation of any communication protocol for data exchange through a synchronous transmitter/receiver (Transcom, Datex-L, Kilostream, DDS...).

The serial synchronous mode can also be implemented on the circuit termination side. In that case, input R x H and output T x H are linked to the data transmission network as shown in *figure 3*.

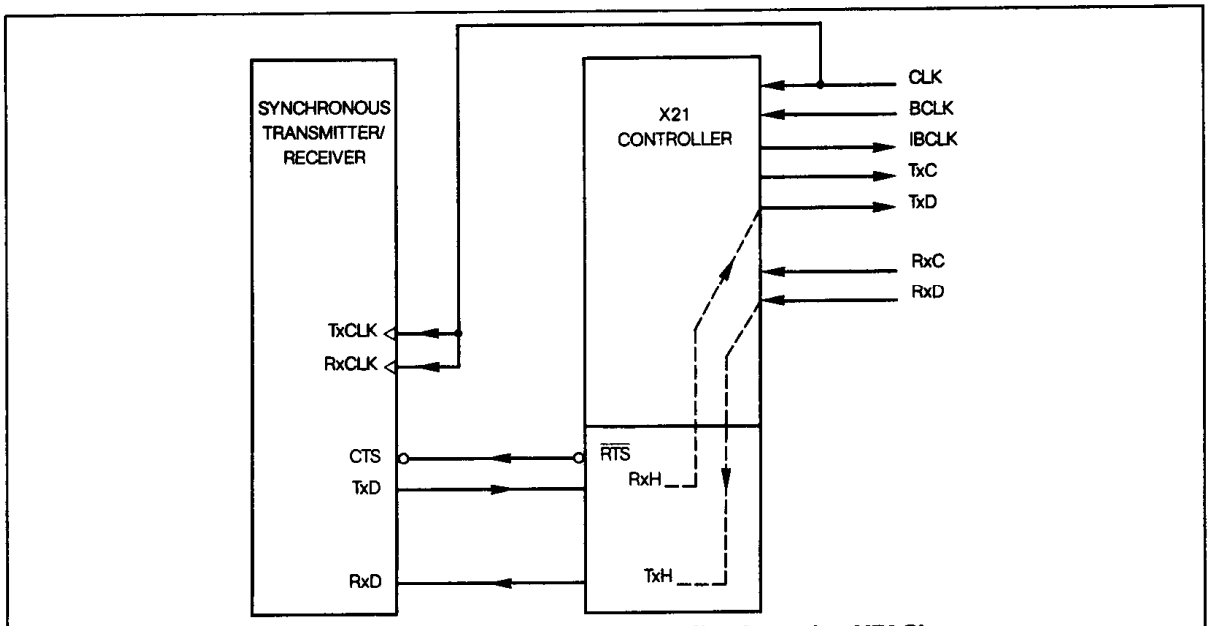


Figure 2: Serial Mode (terminal application using HDLC)

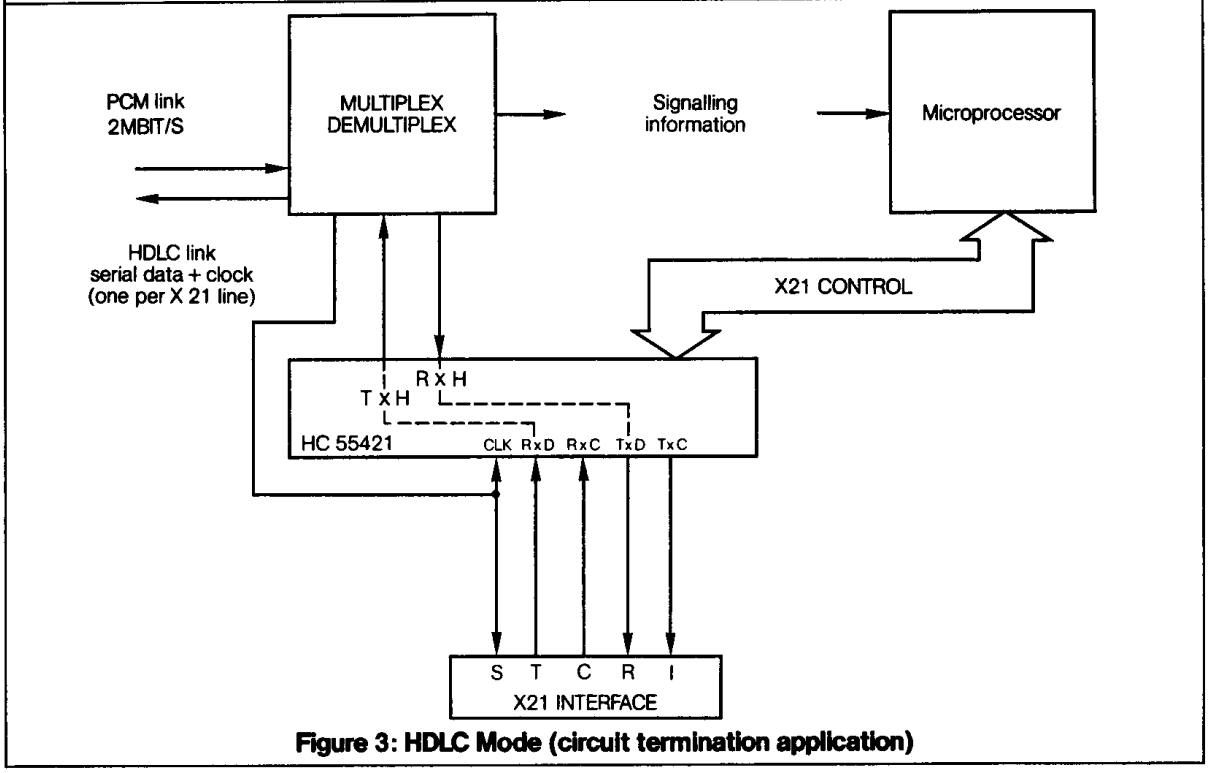
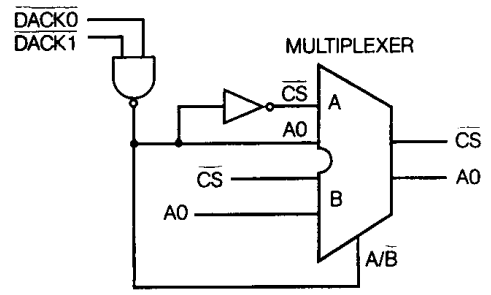


Figure 3: HDLC Mode (circuit termination application)

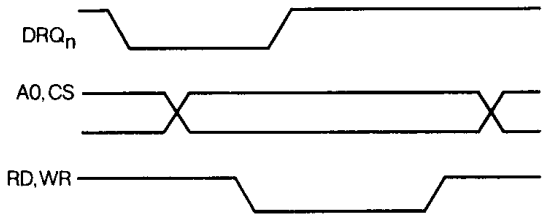
DMA OPERATION

Each HC55421 can be hardware configured to use up to 2 DMA channels: Transmit Channel and Receive Channel; in this case R x INT and T x INT are used as DMA Request lines. Acknowledgment of a DMA cycle is done via normal data read or write cycles. This is accomplished by encoding the DACK signal to generate A0, CS and by multiplexing them with the normal A0, CS signals.

DMA Acknowledge Circuit



DMA Timing



INTERRUPTIONS

• Status interruption S x INT

When enabled (CR4 = 1), this interruption is sent if:

SR1 = 1 → Status change on R x D or R x C.
SR3 = 1 →1 Error detected on R x C.
SR4 = 1 → Parity error.
SR5 = 1 → Error detected on R x D.
SR6 = 1 → Overload in the receive register.

Reading the status register clears this interruption.

• Receive interruption R x INT

When enabled (CR6 = 1), this interruption will occur when a character has been received in register RR, or SR2 = 1.

Reading the receive register clears this interruption.

• Transmit interruption T X INT

When enabled (CR5 = 1), a transmit interruption is set when TR is empty, or SR7 = 1.

This interruption, and also bit SR7, cannot be set in loop mode (CR0 = 0).

Writing into the transmit register clears this interruption. All interruptions are cleared by an external reset (RESET = 0) or an internal reset (CR2 = 1).

Resetting a specific interruption through bits CR4, CR5 or CR6 in the command register will immediately cancel the corresponding interruption.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND : −0.3V to +7V
Input/output voltage : −0.3V to V_{CC} + 0.3V
Storage temperature : −65°C to 150°C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10% operating temperature range 0°C to 70°C.

Parameter	Min.	Max.	Unit	Conditions
Low level input voltage VIL		1.5	V	
High level output/voltage VIH	2		V	
Low level output/voltage VOL		0.4	V	IOL = −4.8 mA
High level output/voltage VOH	2.4		V	IOH = 5 mA
Input leakage current IIL/IIH	−1	+1	µA	$V_{IN} = V_{CC}$ or 0V
3 state output leakage current IOZ	−1	+1	µA	$V_{IN} = V_{CC}$ or 0V
Standby current ICC0		10	µA	V_{CC} = 5V; f_{CLK} = 0 Hz $\overline{CS} = V_{CC}$; *see note 1*
Operating current ICC1		10	mA	V_{CC} = 5V; f_{CLK} = 2 MHz $\overline{CS}$ = GND; *see note 1*

Outputs $\overline{S \times INT}$, $\overline{R \times INT}$ and $\overline{T \times INT}$ are open drain.
Fanout is 2TTL loads max for all outputs including D0-D7.

Note 1: $V_{IN} = V_{CC}$ or GND outputs unloaded.

AC ELECTRICAL CHARACTERISTICS

TA = 0 to 70°C V_{CC} = + 5V ± 10%

Timing requirements.

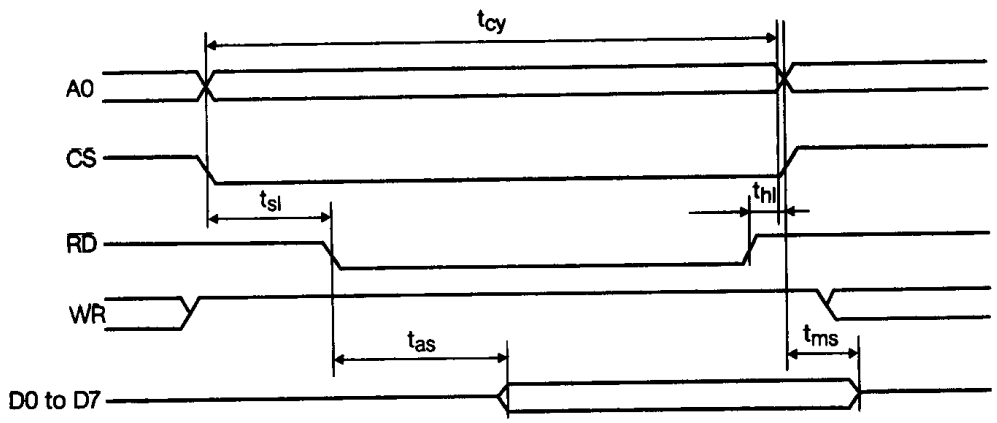
Symbol	Parameter	Min	Max	Unit
tcy	Read/write cycle time	200	–	ns
tsl	Read address set up time	0	–	ns
thl	Read recovery time	20	–	ns
tas	Read access time	–	80	ns
tms	Data hold from chip select high	0	70	ns
tse	Write address set up time	0	–	ns
twe	Write pulse width	50	–	ns
the	Write recovery time	50	–	ns
tsd	Input data valid to write high	50	–	ns
thd	Data hold from write time	20	–	ns
td	Delay IBCLK/CLK	0	50	ns
tclcl	CLK period	480		ns
ttd	CLK to T x D delay		110	ns
tird	CLK to $\overline{R}$ x $\overline{INT}$ delay		tchcl + 110	ns
titd	CLK to $\overline{T}$ x $\overline{INT}$ delay		tclch + 110	ns
tix	$\overline{RD}$ or $\overline{WR}$ to $\overline{T}$ x $\overline{INT}$ or R x $\overline{INT}$		tclch + 110 or tchcl + 110	ns ns
tisd	CLK to $\overline{S}$ x $\overline{INT}$ delay		3/2 x tclcl + 50	ns
tixs	$\overline{RD}$ to $\overline{S}$ x $\overline{INT}$		tclch + 110 or tchcl + 110	ns ns

Test conditions:

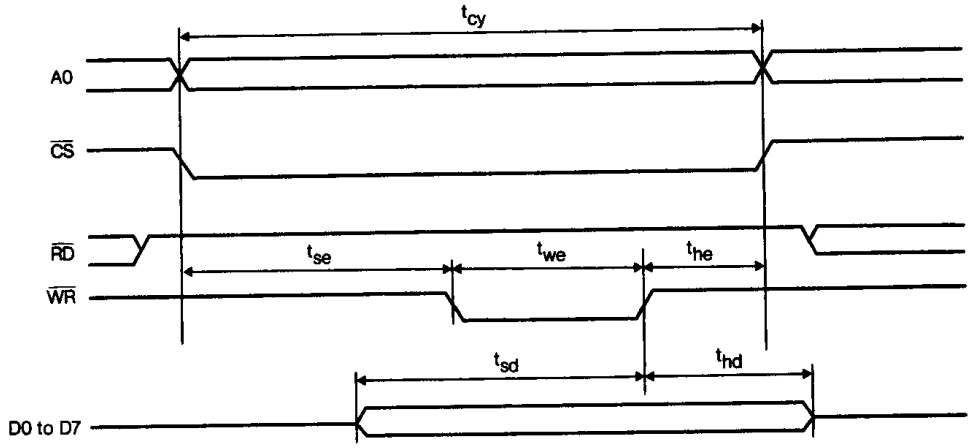
- Cl = 100 pf for all outputs in addition to internal loads.
- All input signals (other than clock) must switch between VIL max – 0.4V and VIH min + 0.4V.
- Clk must switch between 0.4V and V_{CC} – 0.4V, with rise and fall times less or equal 10 ns.

TIMING DIAGRAM

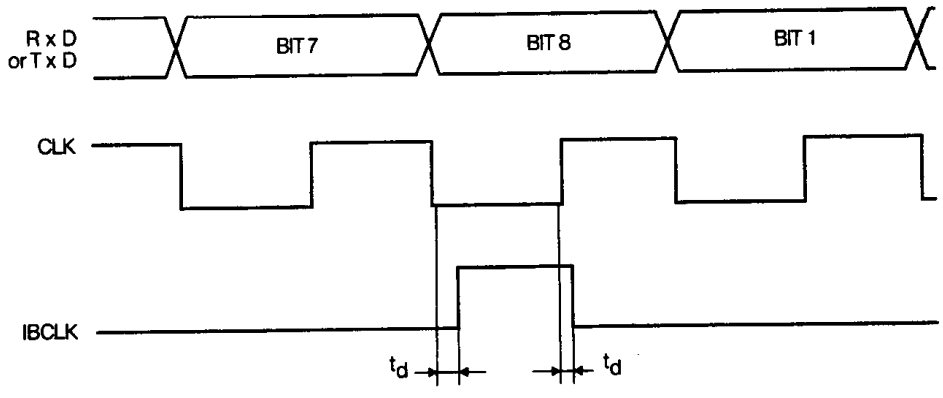
Read cycle: (status register - receive register)



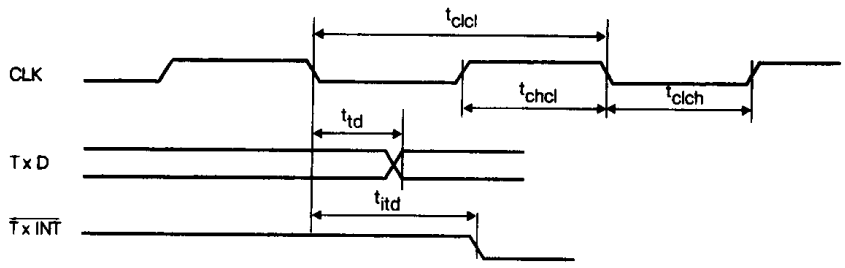
Write cycle: (command register - transmit register)



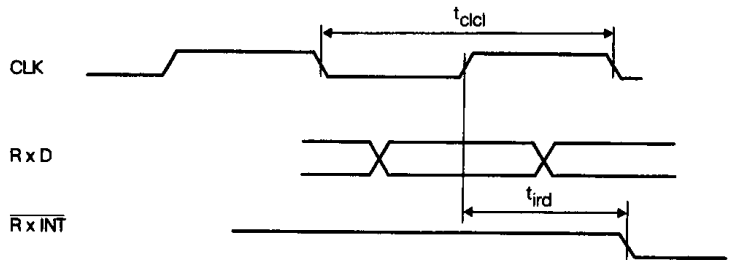
Clock 8 specification (recommandation X24)



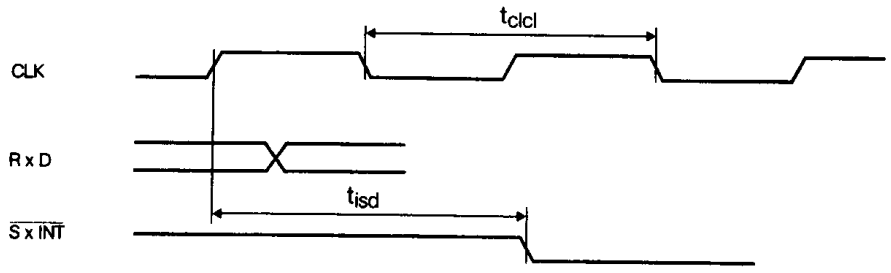
TRANSMIT DATA CYCLE



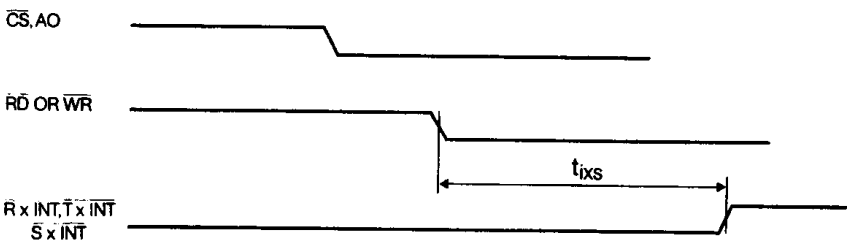
RECEIVE DATA CYCLE



STATUS CHANGE CYCLE



INTERRUPT CYCLE



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