HARRIS SEMICONDUCTOR

HC-5504B

June 1996

SLIC
Subscriber Line Interface Circuit

Features

- **Pin for Pin Replacement for the HC-5504**
- **Capable of 5V or 12V (V_B+) Operation**
- **Monolithic Integrated Device**
- **DI High Voltage Process**
- **Compatible With Worldwide PBX Performance Requirements**
- **Controlled Supply of Battery Feed Current for Short Loops (41mA)**
- **Internal Ring Relay Driver**
- **Allows Interfacing With Negative Superimposed Ringing Systems**
- **Low Power Consumption During Standby**
- **Switch Hook Ground Key and Ring Trip Detection Functions**
- **Selective Denial of Power to Subscriber Loops**

Applications

- **Solid State Line Interface Circuit for Analog and Digital PBX Systems**
- **Direct Inward Dial (DID) Trunks**
- **Voice Messaging PBXs**

Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

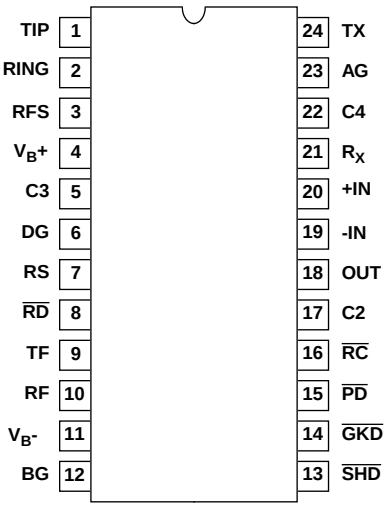
The Harris SLIC is ideally suited for the design of new digital PBX systems by eliminating bulky hybrid transformers.

Ordering Information

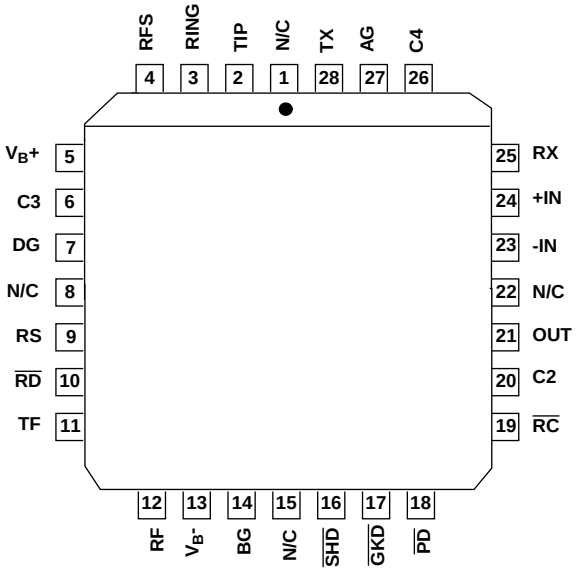
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HC1-5504B-5	0 to 75	24 Ld CERDIP	F24.6
HC1-5504B-9	-40 to 85	24 Ld CERDIP	F24.6
HC3-5504B-5	0 to 75	24 Ld PDIP	E24.6
HC3-5504B-9	-40 to 85	24 Ld PDIP	E24.6
HC4P5504B-5	0 to 75	28 Ld PLCC	N28.45
HC4P5504B-9	-40 to 85	28 Ld PLCC	N28.45
HC9P5504B-5	0 to 75	24 Ld SOIC	M24.3
HC9P5504B-9	-40 to 85	24 Ld SOIC	M24.3

Pinouts

HC-5504B
(PDIP, CERDIP, SOIC)
TOP VIEW



HC-5504B
(PLCC)
TOP VIEW



File Number **2886.2**

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages
- (V_B-) . . . . . -60V to 0.5V
- (V_B+) . . . . . -0.5V to 15V
- (V_B+ - V_B-) 75V

Relay Drive Voltage (V_{RD}) . . . . . -0.5V to 15V

Operating Conditions

Operating Temperature Range
- HC-5504B-5 . . . . . 0°C to 75°C
- HC-5504B-9 . . . . . -40°C to 85°C

Relay Driver Voltage (V_{RD}) . . . . . 5 to 12V
Positive Supply Voltage (V_B+) . . . . . 4.75 to 5.25 or 10.8 to 13.2V
Negative Supply Voltage (V_B-) . . . . . -36 to -58V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) . . . . . 200 to 1200Ω

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	52	15
PDIP Package	65	N/A
PLCC Package	65	N/A
SOIC Package	75	N/A

Maximum Junction Temperature (Hermetic Packages) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC and SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 185
Diode Count 36
Die Dimensions . . . . . 137 x 102
Substrate Potential . . . . . Connected
Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, V_B- = -48V, V_B+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG} = 0 (Note 3), V_B+ = 12V	-	170	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG} = 0 (Note 3), V_B+ = 12V	-	425	550	mW
Off Hook I_B+	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = -40°C	-	-	6.0	mA
Off Hook I_B+	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = 25°C	-	-	5.3	mA
Off Hook I_B-	R_L = 600Ω, I_{LONG} = 0 (Note 3)	-	35	41	mA
Off Hook Loop Current	R_L = 1200Ω, I_{LONG} = 0 (Note 3)	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_B- = -42V, I_{LONG} = 0 (Note 3) T_A = 25°C	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG} = 0 (Note 3)	36	41	48	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	55	-	mA
TIP to RING		-	41	-	mA
TIP and RING to Ground		-	55	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = 12V, $\overline{RC}$ = 1 = HIGH, T_A = 25°C	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	10	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	5	mA
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 3)	-	110	-	kΩ
Transmit Output Impedance	(Note 3)	-	10	20	Ω
2-Wire Return Loss	Referenced to 600Ω + 2.16µF, (Note 3)				
SR_L LO		-	15.5	-	dB
ER_L		-	24	-	dB
SR_L HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz, (Note 3) IEEE Method				
2-Wire Off Hook	$0^oC \le T_A \le 75^oC$	58	65	-	dB
2-Wire On Hook		60	63	-	dB
4-Wire Off Hook		50	58	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method, (Note 3), R_L = 600Ω $0^oC \le T_A \le 75^oC$	-	-	23	dBrnC
		-	-	-67	dBm0p
Insertion Loss 2-Wire to 4-Wire, 4 Wire to 2-Wire	at 1kHz, 0dBm Input Level, Referenced 600Ω	-	±0.05	±0.2	dB
Frequency Response	200Hz - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 3)	-	±0.02	±0.05	dB
Idle Channel Noise 2-Wire to 4-Wire, 4 Wire to 2-Wire	(Note 3)	-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay 2-Wire to 4-Wire, 4 Wire to 2-Wire	(Note 3)	-	-	2	ms
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	36	40	-	dB
Overload Level	V_B+ = +5V	1.5	-	-	V_{PEAK}
2-Wire to 4-Wire, 4 Wire to 2-Wire	V_B+ = 12V	1.75	-	-	V_{PEAK}
Level Linearity 2-Wire to 4-Wire, 4 Wire to 2-Wire	At 1kHz Referenced to 0dBm Level, (Note 3) +3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	(Note 3)				
V_B+ to 2-Wire	30 - 60Hz, R_L = 600Ω	15	-	-	dB
V_B+ to Transmit		15	-	-	dB
V_B- to 2-Wire		15	-	-	dB
V_B- to Transmit		15	-	-	dB
V_B+ to 2-Wire	200 - 16kHz, R_L = 600Ω	30	-	-	dB
V_B+ to Transmit		30	-	-	dB
V_B- to 2-Wire		30	-	-	dB
V_B- to Transmit		30	-	-	dB

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters $T_A = 25^oC$. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA, V_B+ = 12V, 5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_B+ = 12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_B+ = 5V	2.7	-	5.0	V

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 3)	-	1	-	MΩ
Output Voltage Swing	R_L = 10K, V_B+ = 12V	-	±5	-	V_{PEAK}
	R_L = 10K, V_B+ = 5V	-	±3	-	V_{PEAK}
Output Resistance	A_{VCL} = 1 (Note 3)	-	10	-	Ω
Small Signal GBW	(Note 3)	-	1	-	MHz

NOTES:

2. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
4. I_{LONG} = Longitudinal Current

Pin Descriptions

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
5	4	V_B+	Positive Voltage Source - Most positive supply. V_B+ is typically 12V or 5V.
6	5	C_3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B-. Typical value is 0.3µF, 30V.
7	6	DG (Note 5)	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to 5V.
10	8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
13	11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48V with an operational range of -42V to -58V. Frequently referred to as “battery”.
14	12	BG (Note 5)	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
19	16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
20	17	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.
21	18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.

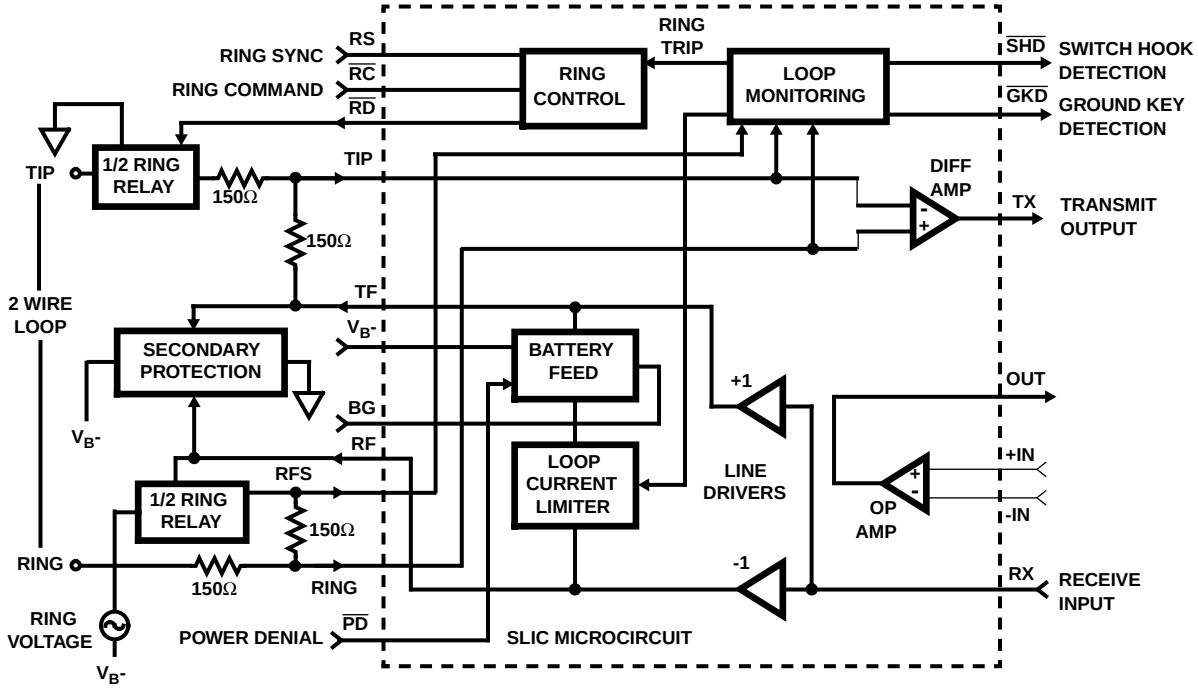
Pin Descriptions (Continued)

28 PIN PLCC	24 PIN DIP/SOIC	SYMBOL	DESCRIPTION
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, 4-Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
26	22	C_4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF, to 1.0µF, 20V. This capacitor should be nonpolarized.
27	23	AG (Note 5)	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1, 8, 15, 22		NC	No internal connection.

NOTES:

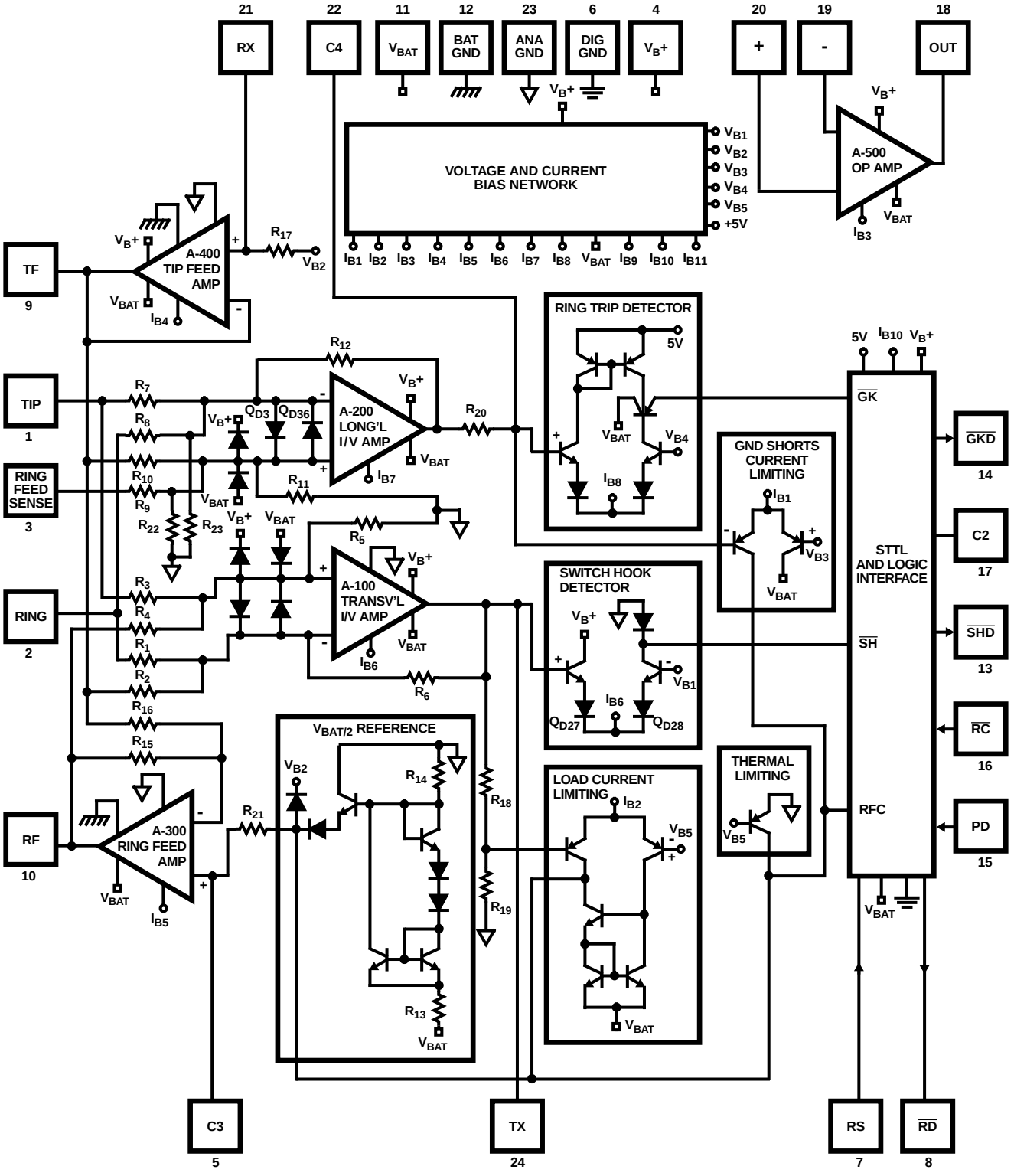
5. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Functional Diagram



Schematic Diagram

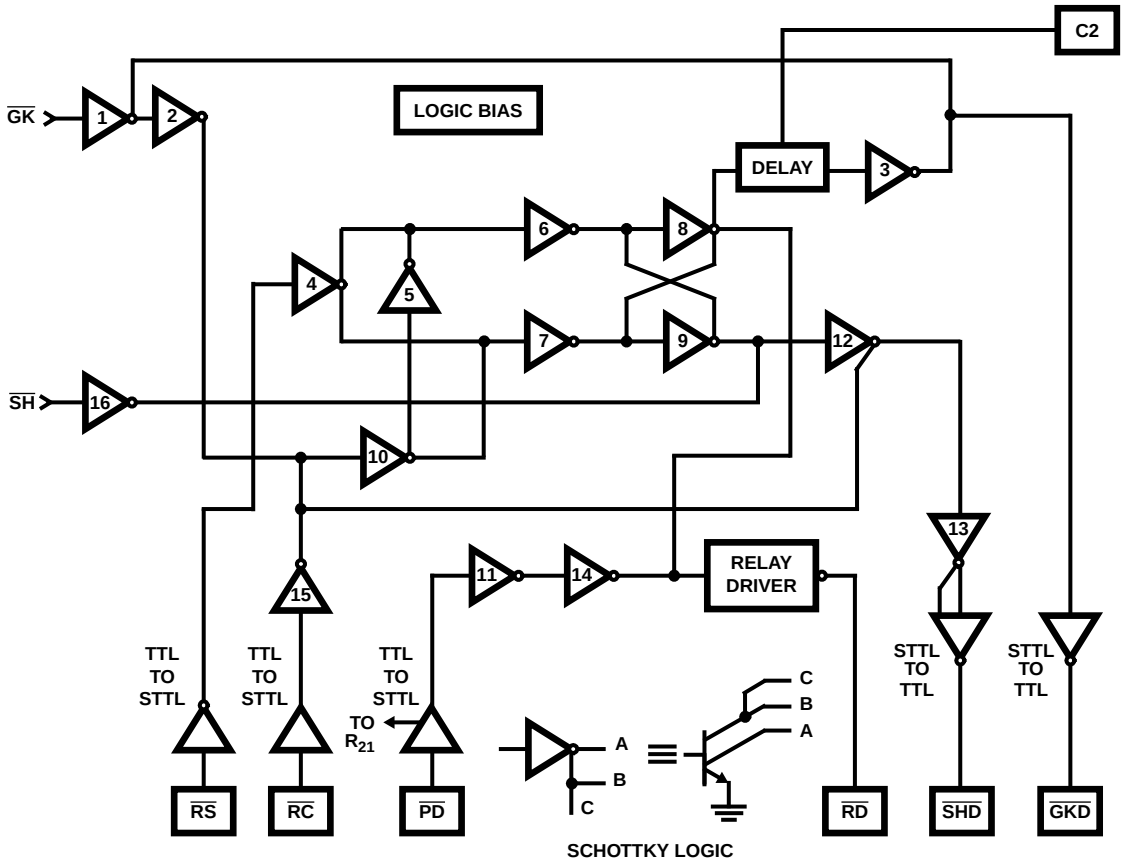
SLIC FUNCTIONAL SCHEMATIC



NOTE: DIP/SOIC Pin Numbers Shown.

Schematic Diagram (Continued)

LOGIC GATE SCHEMATIC



SCHOTTKY LOGIC

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 30mA$_{RMS}$, 15mA$_{RMS}$ per leg, without any performance degradation.

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
50/60Hz Current			
T/GND	11 Cycles	700 (Plastic)	V_{RMS}
R/GND	Limited to 10A$_{RMS}$	350 (Ceramic)	V_{RMS}

Applications Diagram

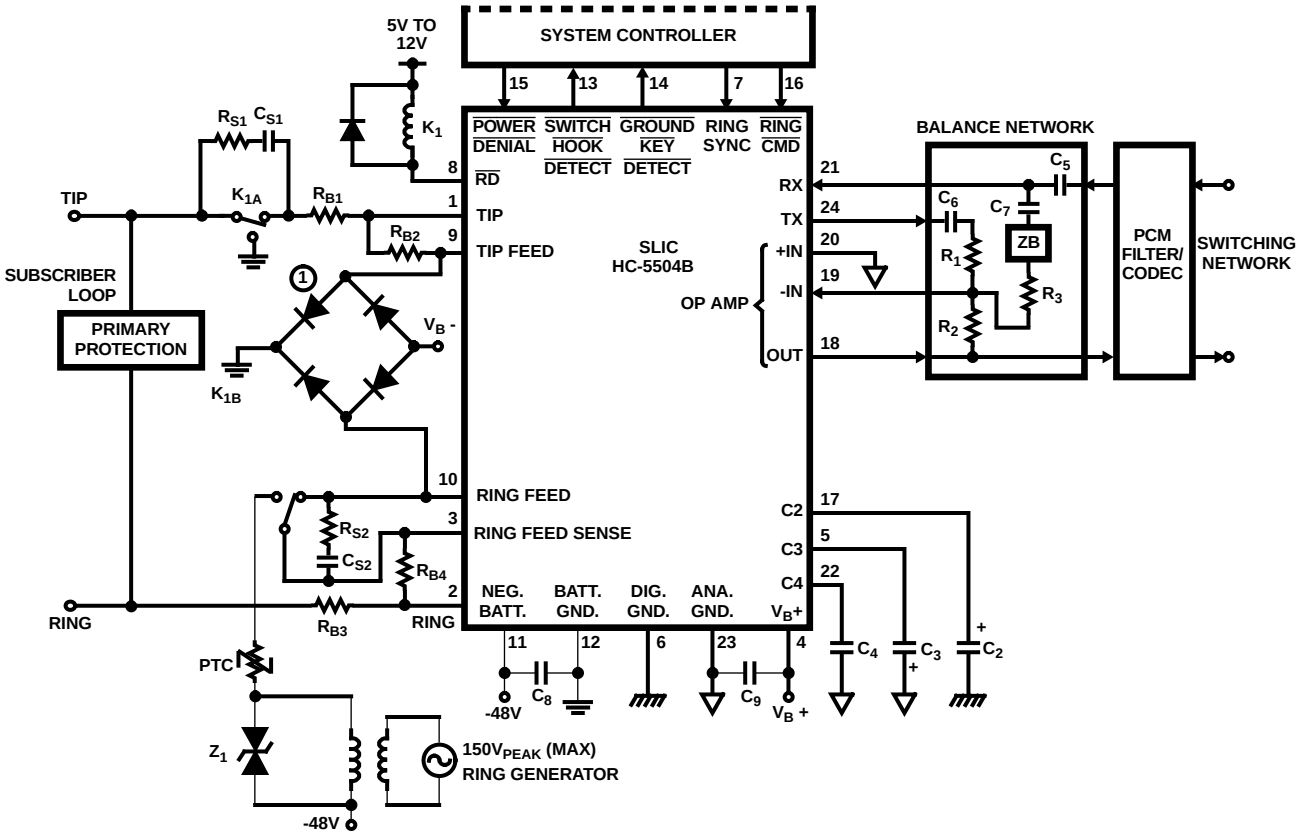


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_2 = 0.15µF, 10V

C_3 = 0.3µF, 30V

C_4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)

C_5 = 0.5µF, 20V

C_6 = C_7 = 0.5µF (10% Match Required) (Note 7)

C_8 = 0.01µF, 100V

C_9 = 0.01µF, 20V, ±20%

R_1 = R_2 = R_3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600Ω Terminations (Note 7).

R_{B1} = R_{B2} = R_{B3} = R_{B4} = 150Ω (0.1% Match Required, 1% absolute value).

R_{S1} = R_{S2} =1kΩ, typically.

C_{S1} = C_{S2} = 0.1µF, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

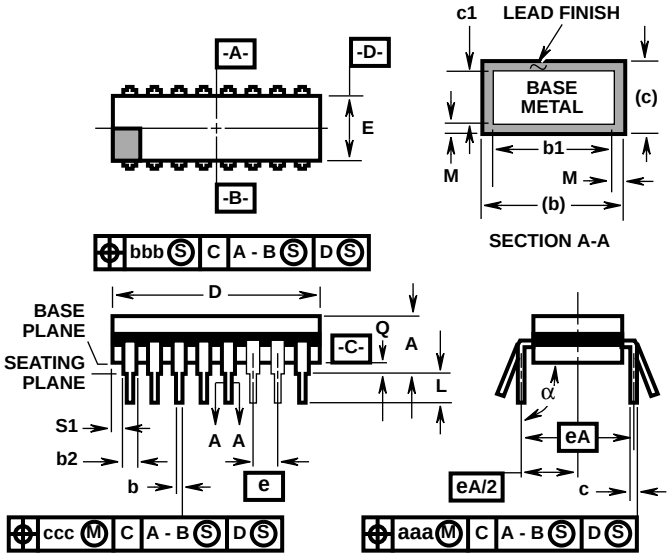
NOTES:

6. Secondary protection diode bridge recommended is a 2A, 200V type.
7. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C_6-R_1 and R_2 and C_7-ZB-R_3, to match in impedance to within 0.3%. Thus, if C_6 and C_7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C_6 sees a -22V step when the loop is closed. Too large a value for C_6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

   A 0.5µF and 100kΩ gives a time constant of 50ms. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.
8. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
9. Application shows Ring Injected Ringing, Balanced or Tip injected configuration may be used.
10. Pin numbers given for DIP/SOIC package.

Additional information is contained in Application Note 549, “The HC-550X Telephone SLICs” By Geoff Phillips

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

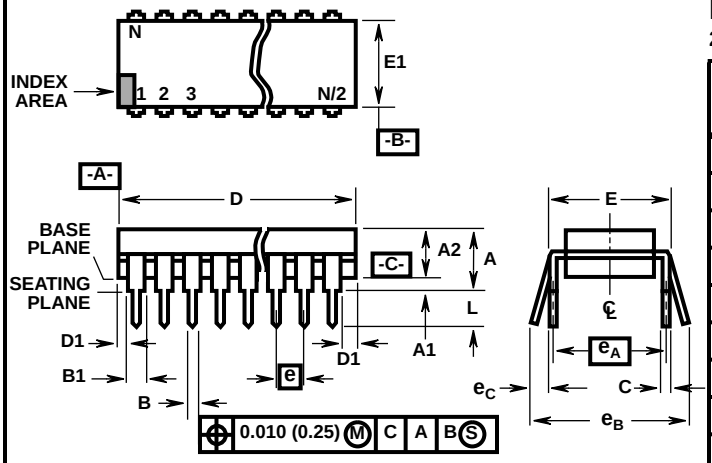
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F24.6 MIL-STD-1835 GDIP1-T24 (D-3, CONFIGURATION A)
24 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	24		24		8

Rev. 0 4/94

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

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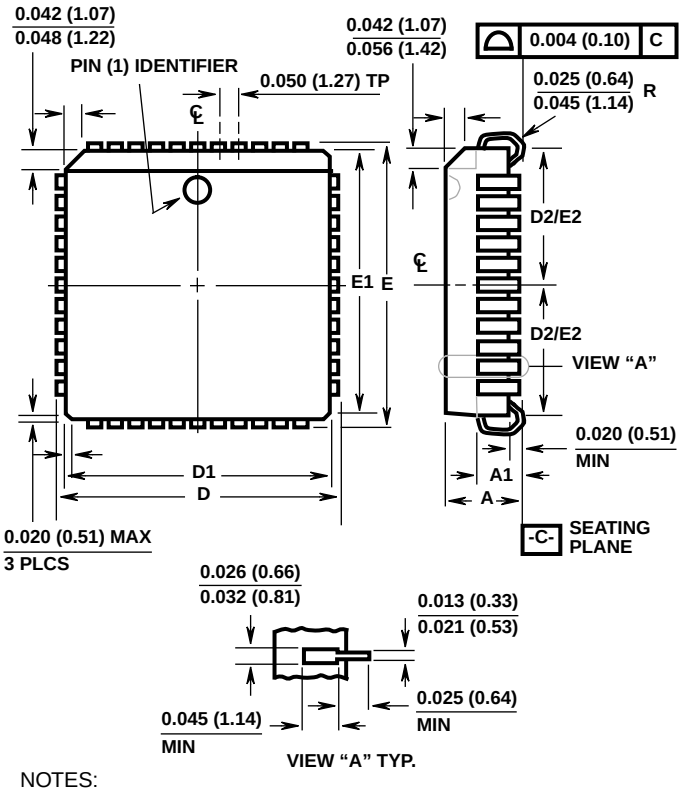
Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

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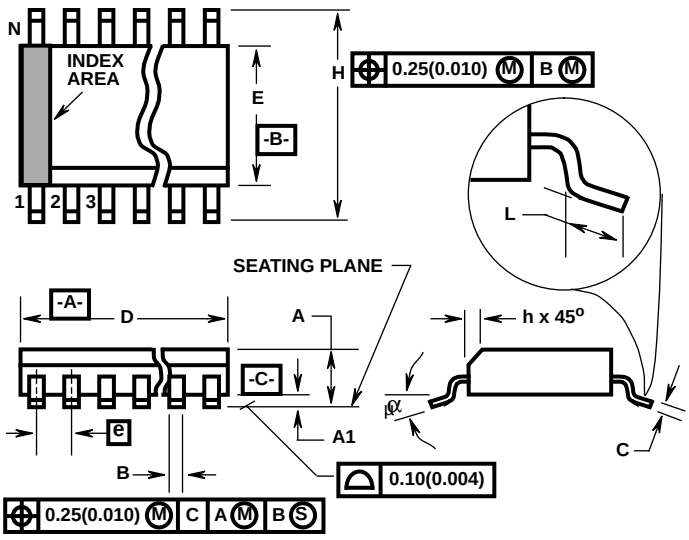
NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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