GENERAL SEMICONDUCTOR®

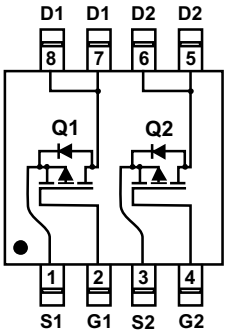
GF4953

Dual P-Channel Enhancement-Mode MOSFET

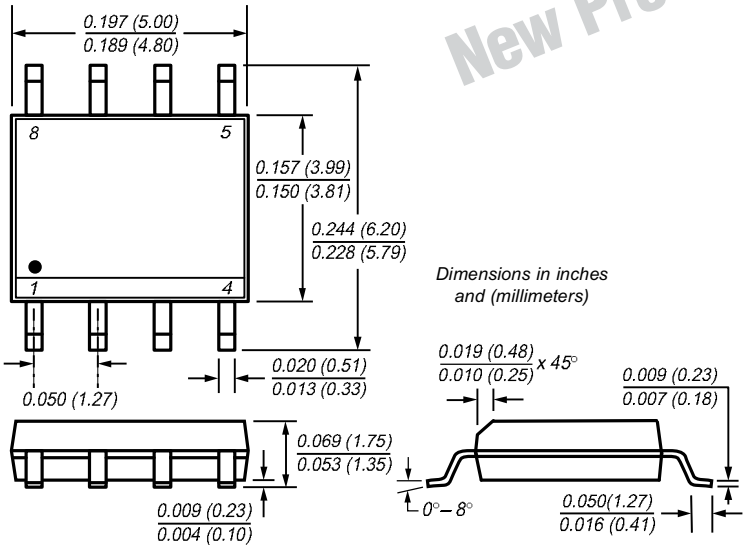
V_{DS} –30V **$R_{DS(ON)}$** 53mΩ **I_D** –4.9A

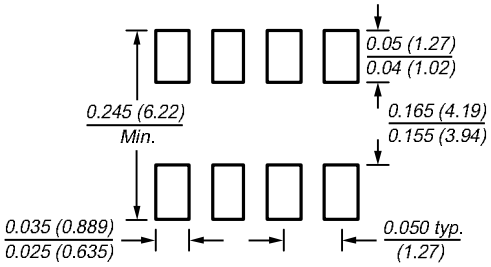
TRENCH GENFET™

New Product



SO-8





Mounting Pad Layout

Mechanical Data

Case: SO-8 molded plastic body

Terminals: Leads solderable per MIL-STD-750,Method 2026

High temperature soldering guaranteed: 250°C/10 seconds at terminals

Mounting Position: Any

Weight: 0.5g

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Specially Designed for Low Voltage DC/DC Converters
- Fast Switching for High Efficiency

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C T_A = 70°C	I_D	–4.9 –3.9	A
Pulsed Drain Current		I_{DM}	–30	
Maximum Power Dissipation(1)	T_A = 25°C T_A = 70°C	P_D	2.0 1.3	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Maximum Junction-to-Ambient Thermal Resistance(1)		$R_{\theta JA}$	62.5	°C/W

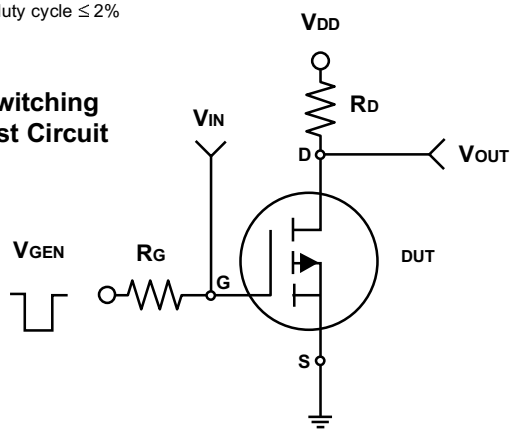
Note: (1) Surface Mounted on FR4 Board, t ≤ 10 sec.

Electrical Characteristics (T_J = 25°C unless otherwise noted)

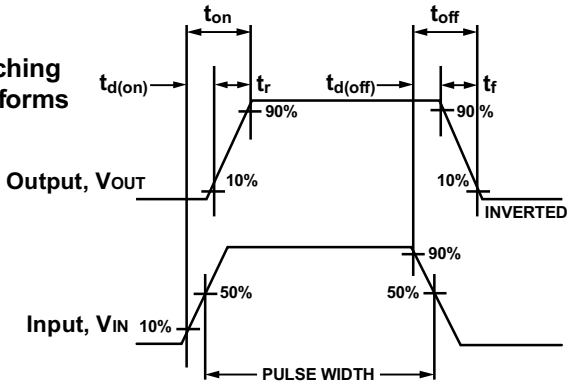
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = –250μA	–30	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250μA	–1.0	–	–3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	–	–	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30V, V_{GS} = 0V	–	–	–1.0	μA
		V_{DS} = –30V, V_{GS} = 0V, T_J = 55°C	–	–	–25	
On-State Drain Current(1)	$I_{D(on)}$	V_{DS} ≥ –5V, V_{GS} = –10V	–20	–	–	A
Drain-Source On-State Resistance(1)	$R_{DS(on)}$	V_{GS} = –10V, I_D = –4.9A	–	43	53	mΩ
		V_{GS} = –4.5V, I_D = –3.6A	–	65	95	
Forward Transconductance(1)	g_{fs}	V_{DS} = –15V, I_D = –4.9A	–	10	–	S
Dynamic						
Total Gate Charge	Q_g	V_{DS}= –15V, I_D= –4.9A, V_{GS}= –5V	–	10	14	nC
		V_{DS} = –15V, V_{GS} = –10V, I_D = –4.9A	–	18	25	
Gate-Source Charge	Q_{gs}		–	3.0	–	
Gate-Drain Charge	Q_{gd}		–	4.0	–	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –15V, R_L = 15Ω, I_D ≈ –1A, V_{GEN} = –10V, R_G = 6Ω	–	9.0	15	ns
Rise Time	t_r		–	5.0	20	
Turn-Off Delay Time	$t_{d(off)}$		–	55	75	
Fall Time	t_f		–	18	25	
Input Capacitance	C_{iss}	V_{DS} = –15V, V_{GS} = 0V, f = 1.0MHz	–	860	–	pF
Output Capacitance	C_{oss}		–	180	–	
Reverse Transfer Capacitance	C_{rss}		–	120	–	
Source-Drain Diode						
Maximum Diode Forward Current	I_S	—	–	–	–1.7	A
Diode Forward Voltage	V_{SD}	I_S = –1.7A, V_{GS} = 0V	–	0.8	–1.2	V

Note: (1) Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%

Switching Test Circuit



Switching Waveforms



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Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

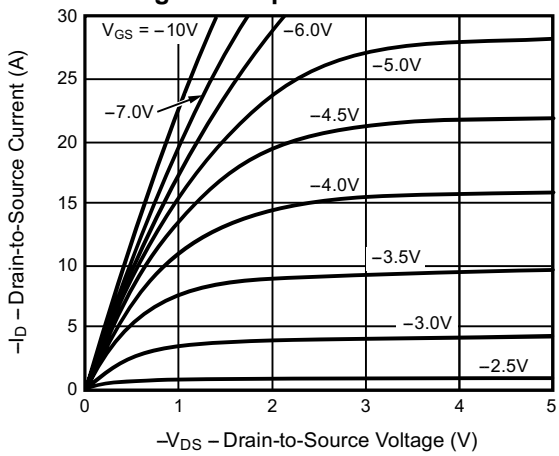


Fig. 2 – Transfer Characteristics

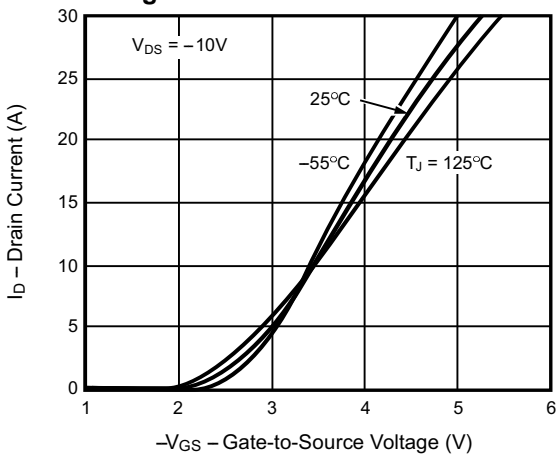


Fig. 3 – Threshold Voltage vs. Temperature

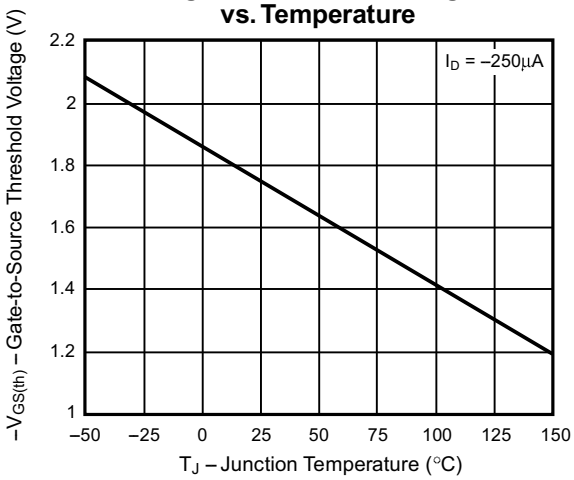


Fig. 4 – On-Resistance vs. Drain Current

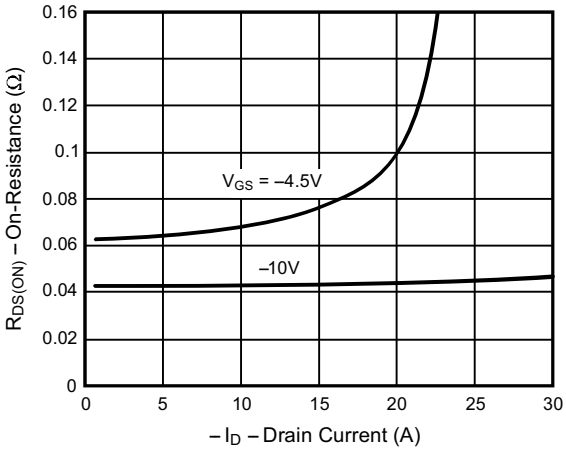
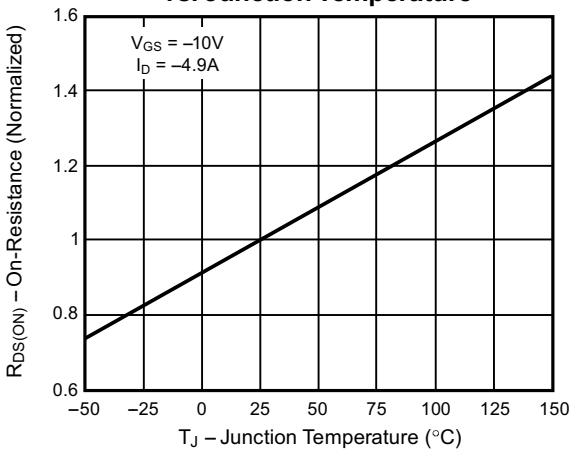


Fig. 5 – On-Resistance vs. Junction Temperature



Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

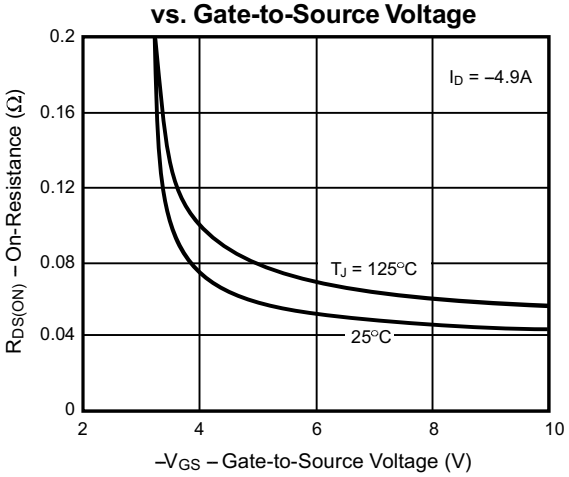


Fig. 7 – Gate Charge

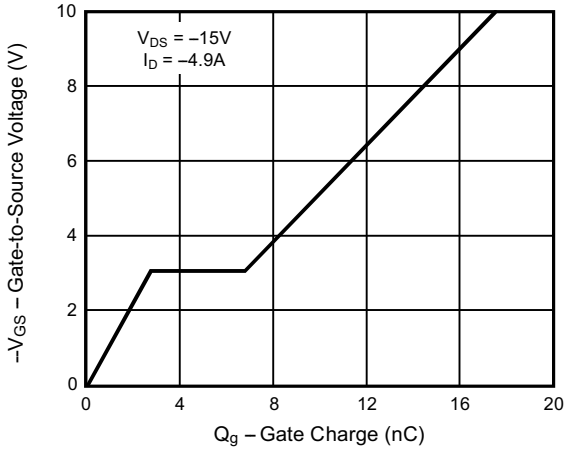


Fig. 8 – Capacitance

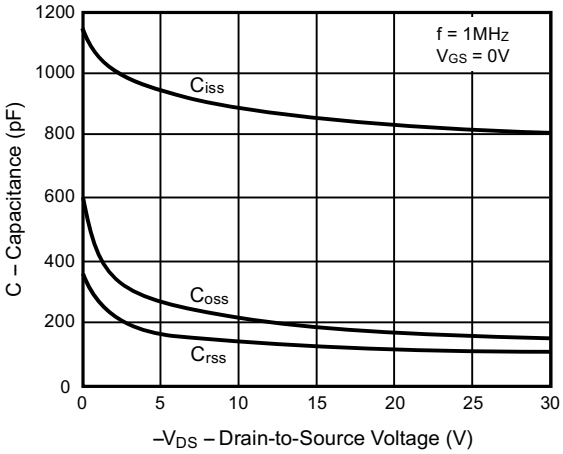
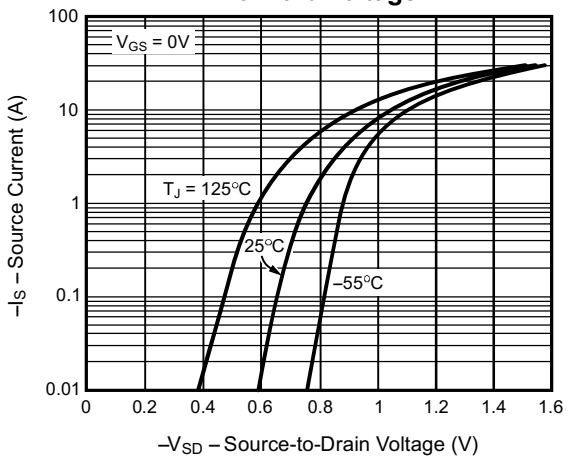


Fig. 9 – Source-Drain Diode Forward Voltage



Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 10 – Breakdown Voltage vs. Junction Temperature

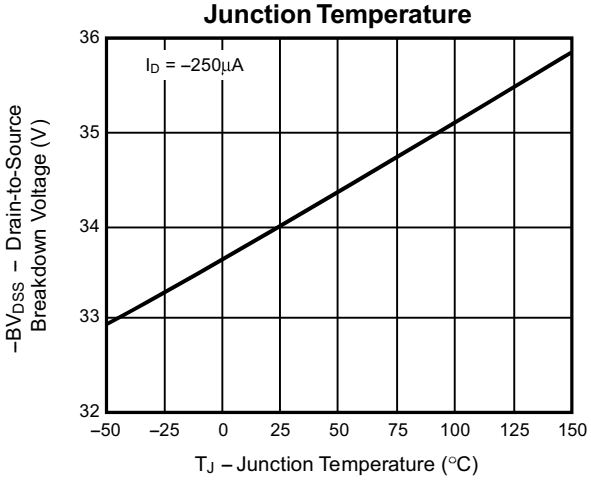


Fig. 11 – Thermal Impedance

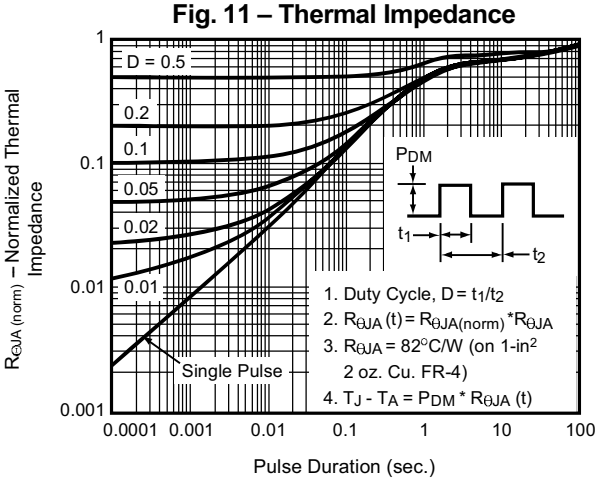


Fig. 12 – Power vs. Pulse Duration

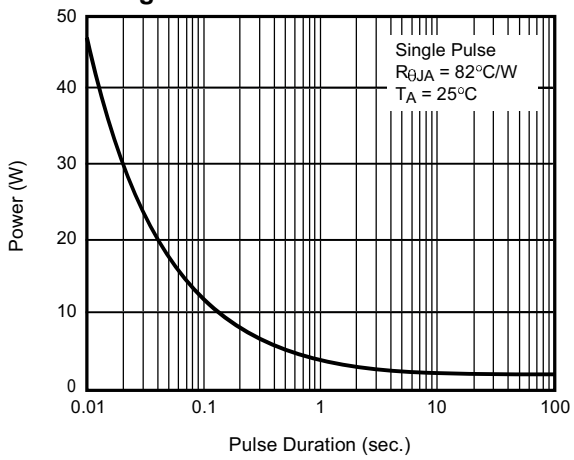


Fig. 13 – Maximum Safe Operating Area