SOT23 NPN SILICON PLANAR HIGH SPEED SWITCHING TRANSISTORS

FMMT2369 FMMT2369A

ISSUE 3 – AUGUST 1995

APPLICATIONS

These devices are suitable for use in high speed, low current switching applications

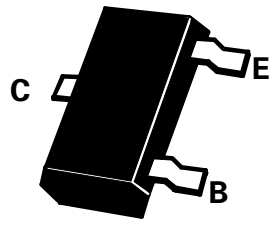
PARTMARKING DETAILS

FMMT2369 - 1J

FMMT2369R - 9R

FMMTA2369A - P5

FMMTA2369AR - 9A



SOT23

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	V_{CBO}	40	V
Collector-Emitter Voltage	V_{CES}	40	V
Collector-Emitter Voltage	V_{CEO}	15	V
Emitter-Base Voltage	V_{EBO}	4.5	V
Continuous Collector Current	I_C	200	mA
Power Dissipation at T_{amb}=25°C	P_{tot}	330	mW
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

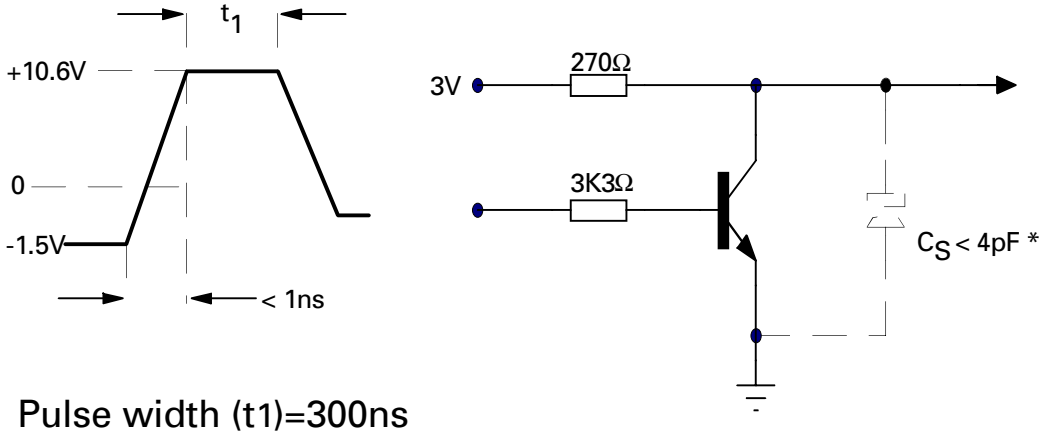
PARAMETER	SYMBOL	FMMT2369		FMMT2369A		UNIT	CONDITIONS.
		MIN.	MAX.	MIN.	MAX.		
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	40		40		V	I_C=10μA, I_E=0
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	15		15		V	I_C=10mA, I_B=0*
	$V_{(BR)CES}$	40		40		V	I_C=10μA, V_{BE}=0
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	4.5		4.5		V	I_E=10μA, I_C=0
Collector Cut-Off Current	I_{CBO}		400		25	nA	V_{CB}=20V, I_E=0
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$		0.25		0.20	V	I_C=10mA, I_B=1mA*
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	0.7	0.85	0.7	0.85	V	I_C=10mA, I_B=1mA*
Static Forward Current Transfer Ratio	h_{FE}	40 20 20	120	40 20	120		I_C=10mA, V_{CE}=1V* I_C=10mA, V_{CE}=1V, T_{amb}=-55°C* I_C=100mA, V_{CE}=1V* I_C=100mA, V_{CE}=2V*
Output Capacitance	C_{obo}		4		4	pF	V_{CB}=5V, I_E=0, f=140KHz
Turn-on Time	t_{on}		12		12	ns	V_{CC}=3V, $V_{BE(off)}$=1.5V I_C=10mA, I_{B1}=3mA (See t_{ON} circuit)
Turn-off Time	t_{off}		18		18	ns	V_{CC}=3V, I_C=10mA, I_{B1}=3mA I_{B2}=1.5mA(See t_{OFF} circuit)
Storage Time	t_s		13		13	ns	I_C=I_{B1}= I_{B2}=10mA (See Storage test circuit)

*Measured under pulsed conditions. Pulse width=300μs. Duty cycle ≤ 2%

Spice parameter data is available upon request for this device

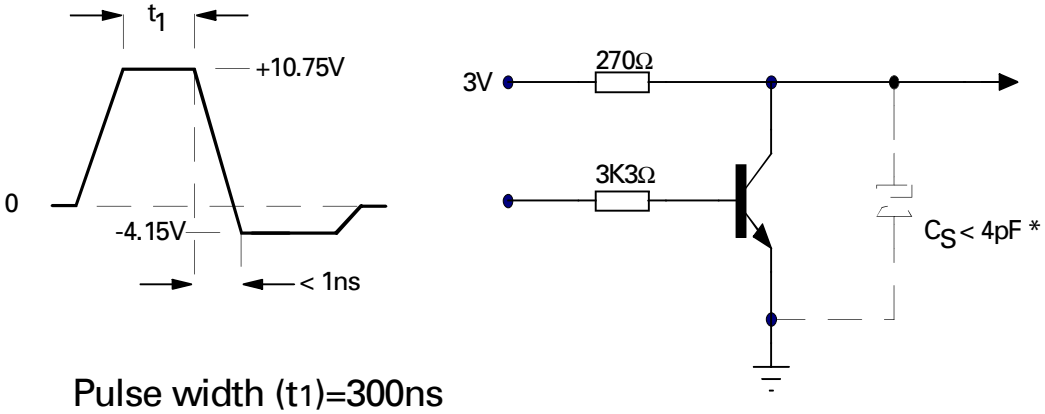
FMMT2369
FMMT2369A

t_{ON} CIRCUIT



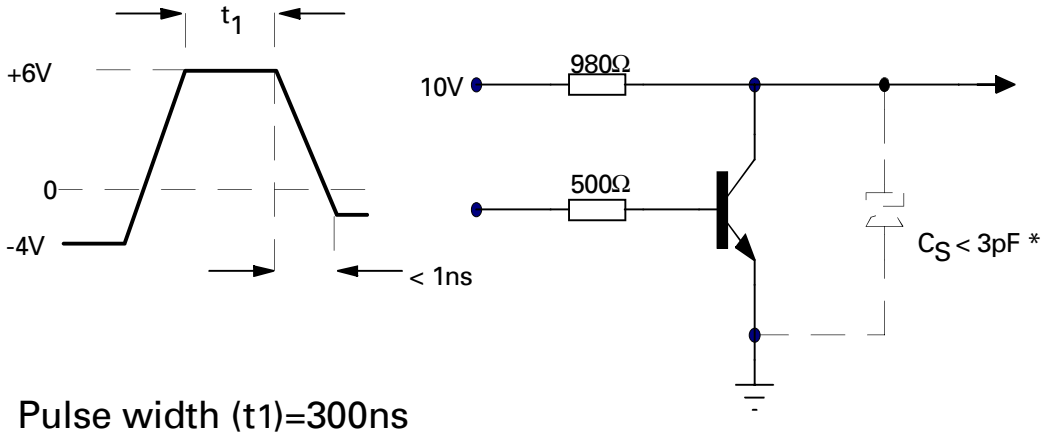
Pulse width (t1)=300ns
Duty cycle = 2%

t_{OFF} CIRCUIT



Pulse width (t1)=300ns
Duty cycle = 2%

STORAGE TEST CIRCUIT



Pulse width (t1)=300ns
Duty cycle = 2%

*** Total shunt capacitance of test jig and connectors**