54110/74110 AND-Gated J-K Master-Slave Flip-Flop with Data Lockout

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T.I.																SN54110	J (1)			W (1)					
																SN74110	J (1)	N (1)							
FAIRCHILD																									
MOTOROLA																									
N.S.C.																									
PHILIPS																									
SIGNETICS																									
																N74110		A (1)							
SIEMENS																FLJ341		(1)							
FUJITSU																									
HITACHI																									
MITSUBISHI																									
NEC																									
TOSHIBA																									

Electrical Characteristics SN54110/SN74110

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54	−55°C to 125°C
Input voltage	5.5V		SN74	0°C to 70°C
		Storage temperature range		−65°C to 150°C

recommended operating conditions

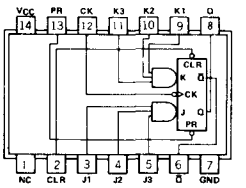
		SN54110			SN74110			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Pulse width, t_w	Clock high	25			25			ns
	Clock low	25			25			
	Preset or clear low	25			25			
Input setup time, t_{setup}		20↑§			20↑§			ns
Input hold time, t_{hold}		5↑§			5↑§			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER*			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage		V_{CC}=MIN, I_I=−12mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=MAX	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OL}=16mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=5.5V			1	mA
I_{IH}	High-level input current	D,J,K, or $\overline{K}$	V_{CC}=MAX, V_I=2.4V			40	μA
		Clear				160	
		Preset				160	
		Clock				40	
I_{IL}	Low-level input current	D,J,K, or $\overline{K}$	V_{CC}=MAX, V_I=0.4V			−1.6	mA
		Clear				−3.2	
		Preset				−3.2	
		Clock				−1.6	
I_{OS}	Short-circuit output current◆	Series 54	V_{CC}=MAX	−20		−57	mA
		Series 74		−18		−57	
I_{CC}	Supply current (Average per flip-flop)		V_{CC}=MAX, See Note 1		23	34	mA
f_{max}	maximum clock frequency		V_{CC}=5V, T_A=25°C, C_L=15pF, R_L=400Ω	20	25		MHz
t_{PLH}	from Preset to output Q (as applicable)				12	20	ns
t_{PHL}	from Preset to output $\overline{Q}$ (as applicable)				18	25	
t_{PLH}	from Clear to output $\overline{Q}$ (as applicable)				12	20	ns
t_{PHL}	from Clear to output Q (as applicable)				18	25	
t_{PLH}	from Clock				20	30	ns
t_{PHL}	to output Q or $\overline{Q}$				13	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC}=5V, T_A=25°C.
◆Not more than one output should be shorted at a time.
*t_{PLH}=propagation delay time, low-to-high-level output.
t_{PHL}=propagation delay time, high-to-low-level output.
§↑The arrow indicates that the rising edge of the clock pulse is used for refence.

Pin Assignment (Top View)



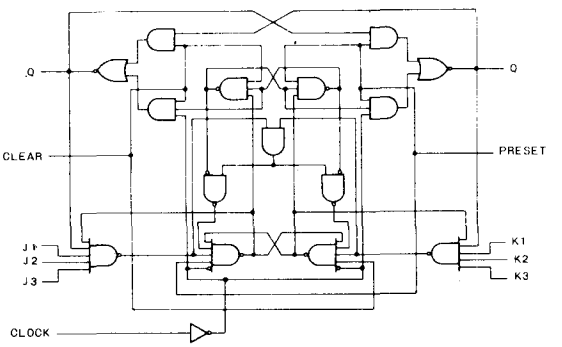
NC-No internal connection

Function Table

'110 (See Note 2)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

positive logic: J = J1·J2·J3
K = K1·K2·K3



'110-GATED J-K WITH CLEAR AND PRESET

NOTES:
1. With all outputs open, ICC is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5V.
2. H=high-level (steady state), L=low level (steady state), X=irrelevant
⎍=high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q_0=the level of Q before the indicated input condition were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.