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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD
SEMICONDUCTOR®

Aug 2011

FDD26AN06A0_F085

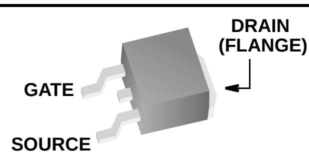
N-Channel PowerTrench® MOSFET
60V, 36A, 26mΩ

Features

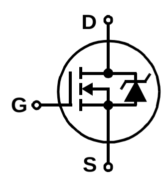
- $r_{DS(ON)}$ = 20mΩ (Typ.), V_{GS} = 10V, I_D = 36A
- Q_g(tot) = 13nC (Typ.), V_{GS} = 10V
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

Applications

- Motor / Body Load Control
- ABS Systems
- Powertrain Management
- Injection Systems
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 12V and 24V systems



TO-252AA
FDD SERIES



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25^{o}C, V_{GS} = 10V)	36	A
	Continuous (T_C = 100^{o}C, V_{GS} = 10V)	25	A
	Continuous (T_{amb} = 25^{o}C, V_{GS} = 10V, $R_{\theta JA}$ = 52^{o}C/W)	7	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	35	mJ
P_D	Power dissipation	75	W
	Derate above 25^{o}C	0.5	W/^{o}C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	^{o}C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252	2.0	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in^2 copper pad area	52	^{o}C/W

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD26AN06A0	FDD26AN06A0_F085	TO-252AA	330mm	16mm	2500 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50V		-	-	1	μA
		V_{GS} = 0V	T_C = 150°C	-	-	250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250μA		2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 36A, V_{GS} = 10V		-	0.020	0.026	Ω
		I_D = 36A, V_{GS} = 10V, T_J = 175°C		-	0.045	0.058	Ω
Dynamic Characteristics							
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	800	-	pF
C_{OSS}	Output Capacitance			-	155	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	55	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V	V_{DD} = 30V, I_D = 36A, I_g = 1.0mA	-	13	17	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 2V		-	1.7	2.2	nC
Q_{gs}	Gate to Source Gate Charge			-	4.3	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	2.6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	4.6	-	nC
Switching Characteristics (V_{GS} = 10V)							
t_{ON}	Turn-On Time	V_{DD} = 30V, I_D = 36A, V_{GS} = 10V, R_{GS} = 25Ω		-	-	123	ns
$t_{d(ON)}$	Turn-On Delay Time			-	9	-	ns
t_r	Rise Time			-	72	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	23	-	ns
t_f	Fall Time			-	35	-	ns
t_{OFF}	Turn-Off Time			-	-	88	ns
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 36A		-	-	1.25	V
		I_{SD} = 18A		-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 36A, dI_{SD}/dt = 100A/μs		-	-	43	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 36A, dI_{SD}/dt = 100A/μs		-	-	50	nC

Notes:
1: Starting T_J = 25°C, L = 83μH, I_{AS} = 29A, V_{DD} = 54V, V_{GS} = 10V.

Typical Characteristics T_C = 25°C unless otherwise noted

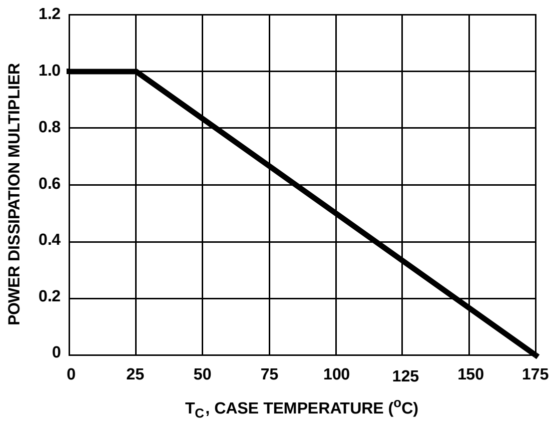


Figure 1. Normalized Power Dissipation vs Case Temperature

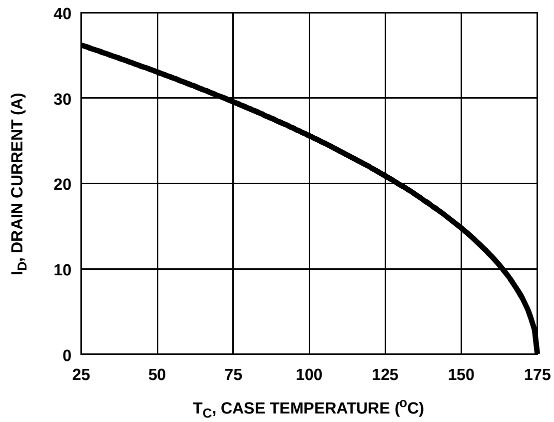


Figure 2. Maximum Continuous Drain Current vs Case Temperature

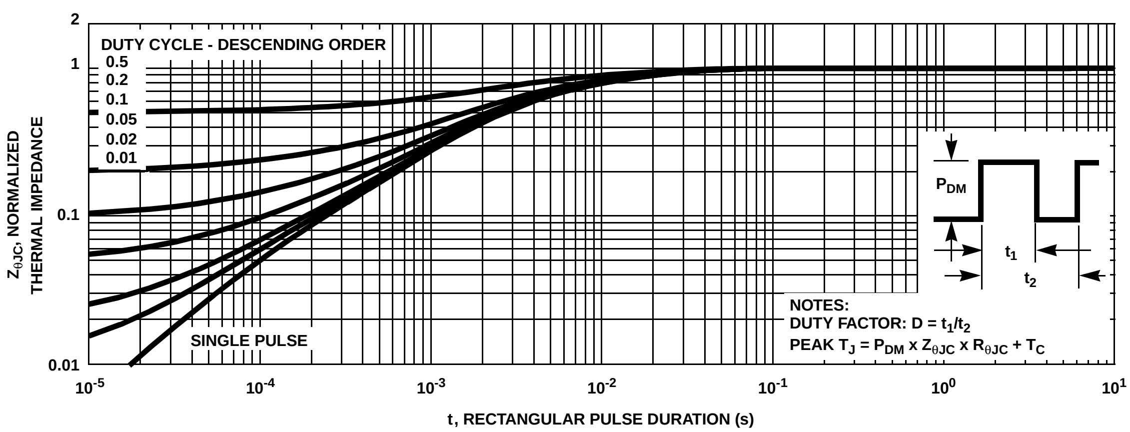


Figure 3. Normalized Maximum Transient Thermal Impedance

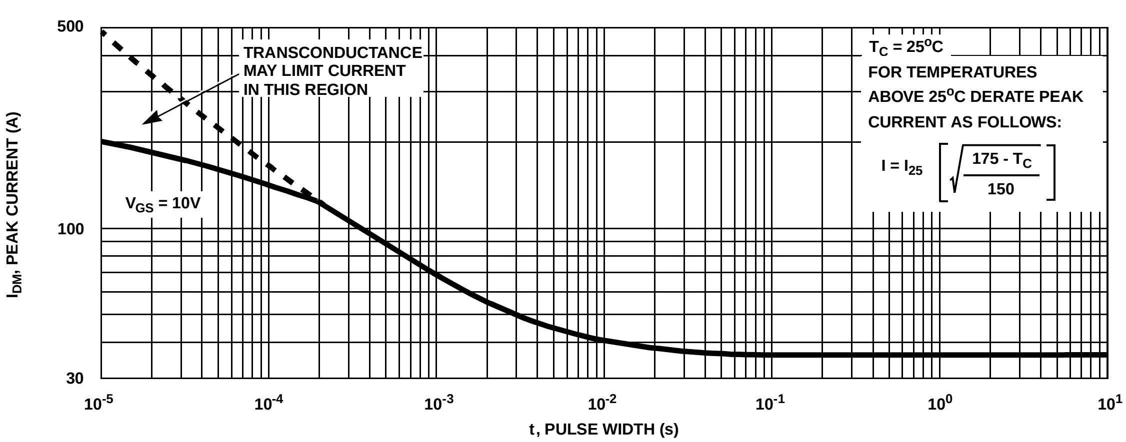


Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted

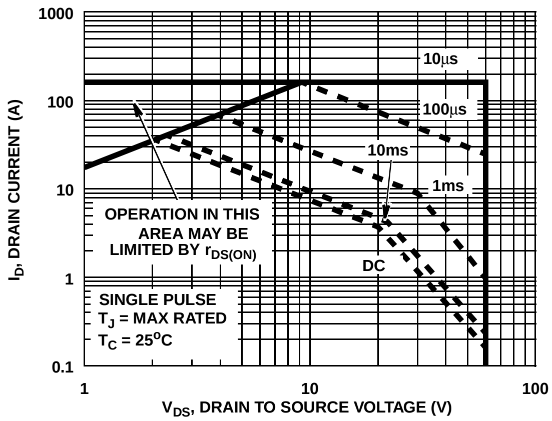
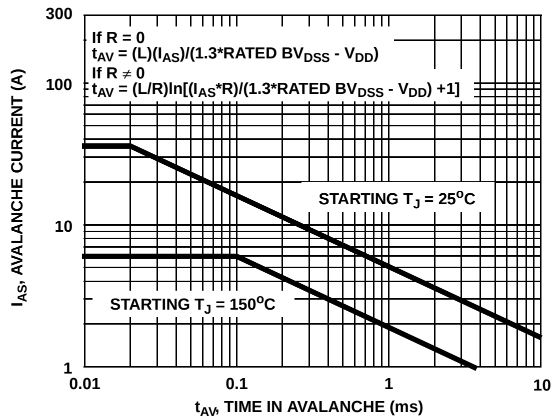


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

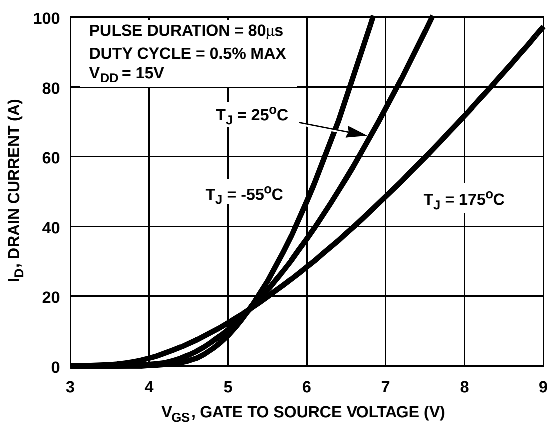


Figure 7. Transfer Characteristics

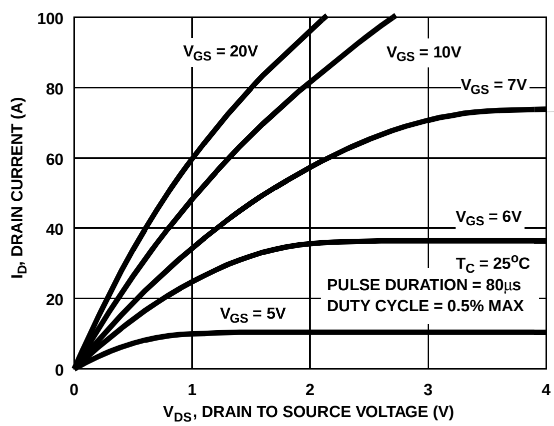


Figure 8. Saturation Characteristics

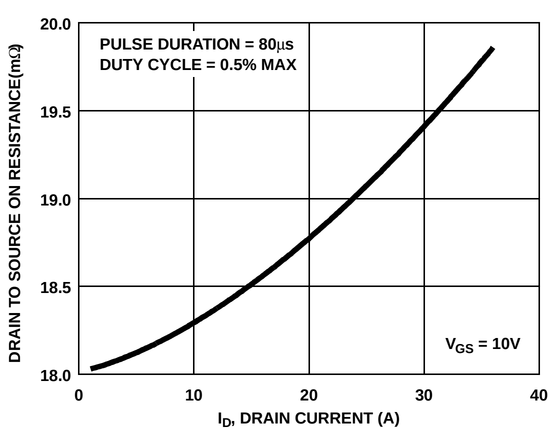


Figure 9. Drain to Source On Resistance vs Drain Current

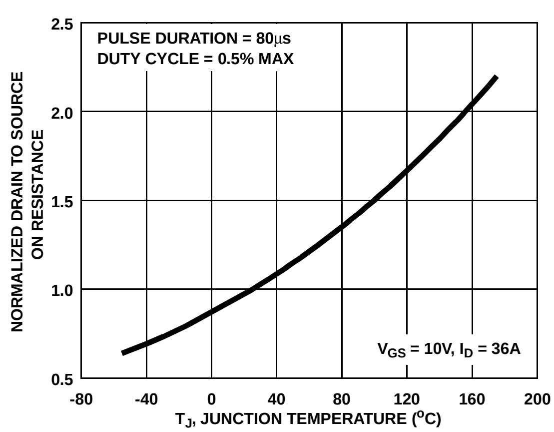


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted

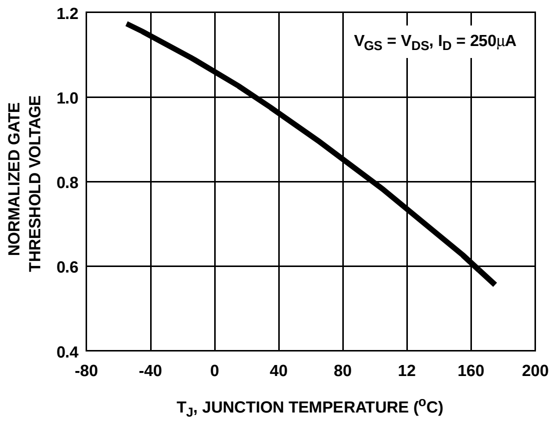


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

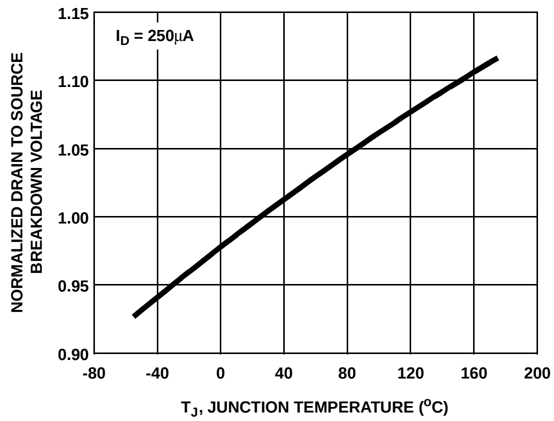


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

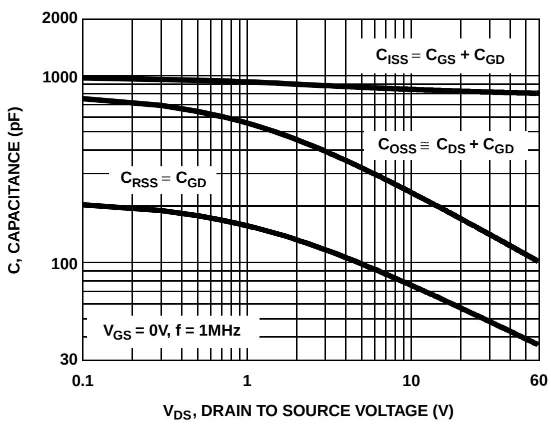


Figure 13. Capacitance vs Drain to Source Voltage

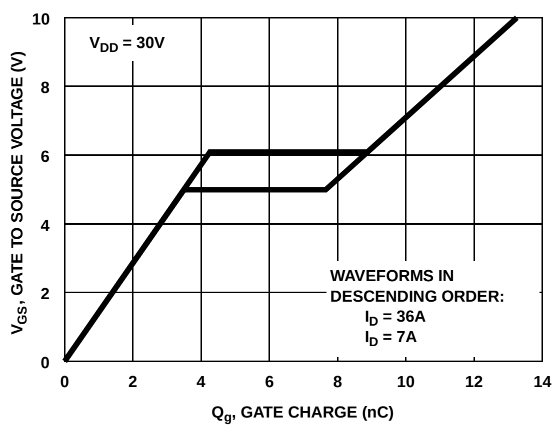


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

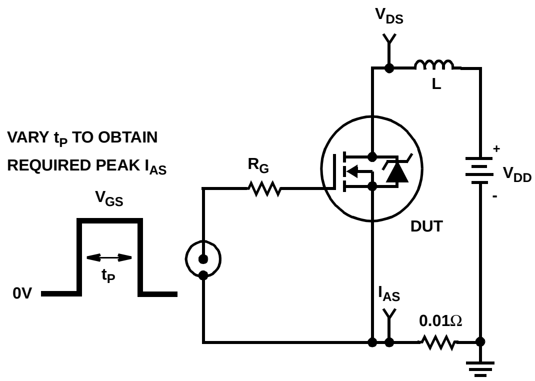


Figure 15. Unclamped Energy Test Circuit

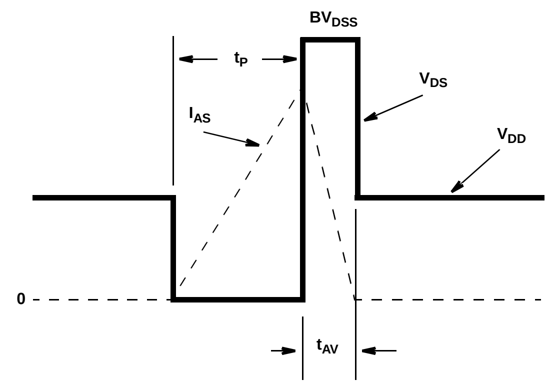


Figure 16. Unclamped Energy Waveforms

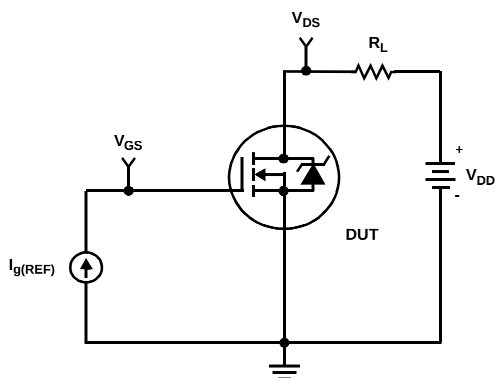


Figure 17. Gate Charge Test Circuit

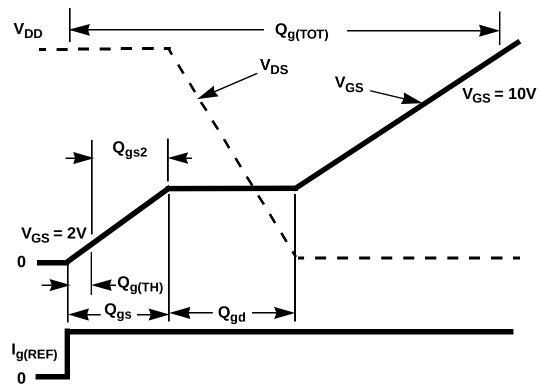


Figure 18. Gate Charge Waveforms

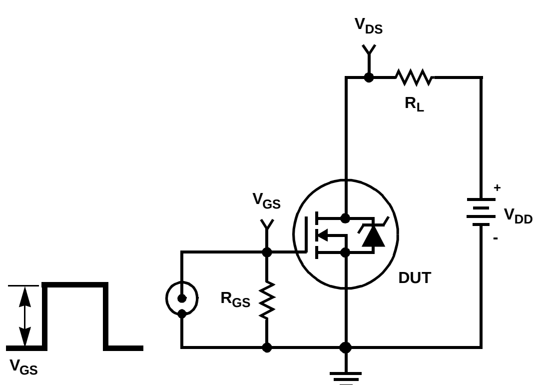


Figure 19. Switching Time Test Circuit

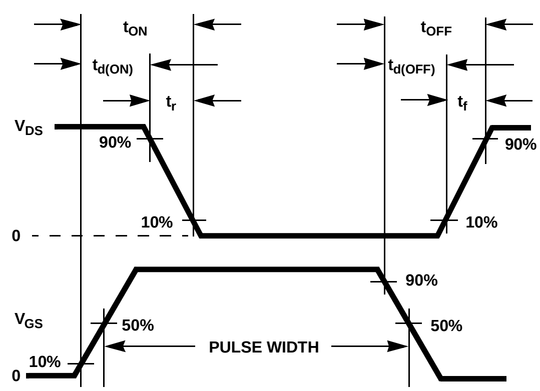


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \qquad \text{(EQ. 2)}$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \qquad \text{(EQ. 3)}$$

Area in Centimeters Squared

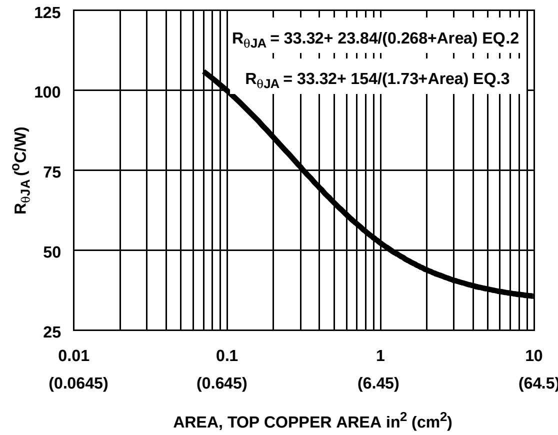


Figure 21. Thermal Resistance vs Mounting Pad Area

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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