ETC5051 • ETC5056

MONOLITHIC PARALLEL INTERFACE CODEC/FILTER

The ETC5051/ETC5056 family consists of A-law and μ-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in Figure 1, parallel I/O data bus interface. The devices are fabricated using double-poly CMOS process.

The encode portion for each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also-included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ-law PCM format.

The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads.

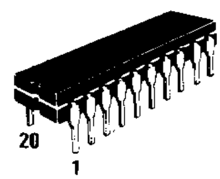
The ETC5051, ETC5056 are especially designed to be used with a line interface controller providing local time and space switching in a distributed control switching system.

- Complete CODEC and filtering system including :
  - Transmit high pass and low pass filtering.
  - Receive low pass filter with sin x/x correction.
  - Receive power amplifier.
  - Active RC noise filters.
  - μ-255 law COder and DECoder - ETC5051
  - A-law COder and DECoder - ETC5056
  - Internal precision voltage reference.
  - Internal auto-zero circuitry.
- Meets or exceeds all D3/D4 and CCITT specifications.
- ±5 V operation.
- Low operating power - typically 60 mW.
- Power-down standby mode - typically 3 mW.
- High speed TRI-STATE® data bus.
- 2 loopback test modes.
- Second source of TP3051, TP3056.

CMOS

MONOLITHIC PARALLEL DATA INTERFACE CODEC/FILTER

CASE J20A



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PIN ASSIGNMENT

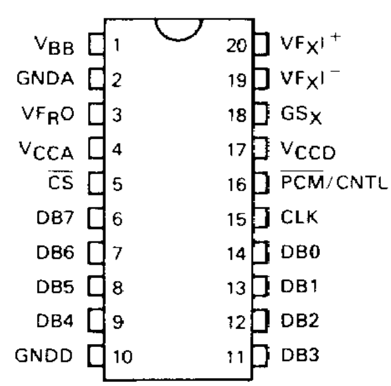

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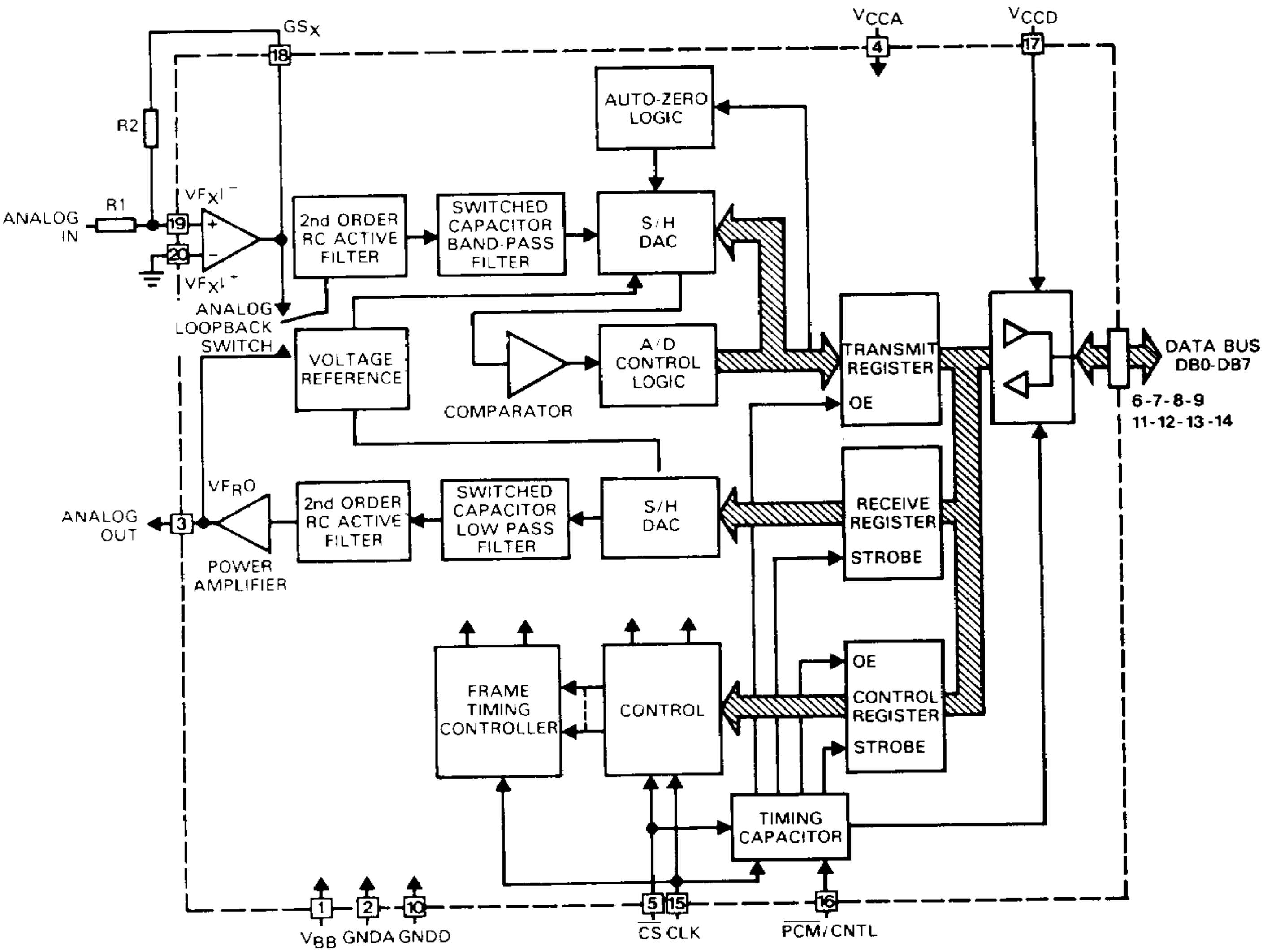
FIGURE 1 - BLOCK DIAGRAM



Parallel CODEC/FILTER

PIN DESCRIPTION

NAME	PIN TYPE *	N°	DESCRIPTION
V_{BB}	S	1	Negative power supply pin. $V_{BB} = -5$ V $\pm 5\%$
GNDA	GND	2	Analog ground. All analog signals are referenced to this pin.
VF_RO	O	3	Analog output of the receive power amplifier. This output can drive a 600 Ω load to ± 2.5 V.
V_{CCA}	S	4	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5$ V $\pm 5\%$. Must be connected to V_{CCD}
$\overline{CS}$	I	5	Device chip select input which controls READ, WRITE and TRI-STATE® operations on the data bus. $\overline{CS}$ does not control the state of any analog functions.
DB7	I/O	6	Bit 7 I/O on the data bus. The PCM LSB.
DB6	I/O	7	Bit 6 I/O on the data bus.
DB5	I/O	8	Bit 5 I/O on the data bus.
DB4	I/O	9	Bit 4 I/O on the data bus.
GNDD	GND	10	Digital ground. All digital signals are referenced to this pin.
DB3	I/O	11	Bit 3 I/O on the data bus.
DB2	I/O	12	Bit 2 I/O on the data bus.
DB1	I/O	13	Bit 1 I/O on the data bus.
DB0	I/O	14	Bit 0 I/O on the data bus. This is the PCM sign bit.
CLK	I	15	The clock input for the switched-capacitor filter and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.
$\overline{PCM}$/CNTL	I	16	This control input determines whether the information on the data bus is PCM data or control data.
V_{CCD}	S	17	Positive power supply pin for the bus drivers. $V_{CCD} = 5$ V $\pm 5\%$. Must be connected to V_{CCA}
GS_X	O	18	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	I	19	Inverting input of the transmit input amplifier.
VF_XI^+	I	20	Non-inverting input of the transmit input amplifier.

* I : Input, O : Output, S : Power supply.
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FUNCTIONAL DESCRIPTION

CLOCK AND DATA BUS CONTROL

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table 1 and must be correctly selected by control bits C0 and C1.

CLK also functions as a READ/$\overline{\text{WRITE}}$ control signal, with the device reading the data bus on a positive half-clock cycle and writing the bus on a negative half-clock cycle, as shown in Figure 4.

POWER-UP

When power is first applied, power-on reset circuitry initializes the CODEC/filter and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0-DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The ETC5051, ETC5056 is powered-up via a command to the control register (see Control Register Functions). This sets the device in the standby mode with all circuitry activated, but encoding and decoding do not begin untill PCM READ and PCM WRITE chip selects occur.

TABLE I. Control Bit Functions

Control Bits	Function		
C0, C1	Select Clock Frequency		
	C0	**C1**	**Frequency**
	0	X	1.024 MHz
	1	0	0.768 MHz or 0.772 MHz
	1	1	1.28 MHz
C2, C3	Digital and Analog Loopback		
	C2	**C3**	**Mode**
	1	X	digital loopback
	0	1	analog loopback
	0	0	normal
C4	Power Down/Power-Up 1 = power-down 0 = power-up		
C5	ETC5051 : Don't care ETC5056 0 : A-law without even bit inversion 1 : A law with even bit inversion		
C6, C7	Don't care		

DATA BUS ASSIGNEMENT

The parallel I/O data bus is defined as follows :

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

READING THE BUS

If CLK is low when $\overline{\text{CS}}$ goes low, bus data is gated in during the next positive half-clock cycle of CLK and latched or the negative-going transition. If PCM/CNTL is low during the falling $\overline{\text{CS}}$ transition, then the bus data is defined as PCM voice data, which is latched into the receive register. This also functions as an internal receive frame synchronization pulse to start a decode cycle and must occur once per receive frame ; i.e., at an 8 kHz rate.

If $\overline{\text{PCM}}$/CNTL is high during the falling $\overline{\text{CS}}$ transition, the bus data is latched into the control register. This does not effect frame synchronization.

WRITING THE BUS

If CLK is high when $\overline{\text{CS}}$ goes low, at the next falling transition of CLK, the bus drivers are enabled and either the PCM transmit data or the contents of the control register are gated onto the bus, depending on the level of PCM/CNTL at the $\overline{\text{CS}}$ transition. If PCM/CNTL is low during the $\overline{\text{CS}}$ falling transition, the transmit register data is written to the bus. An internal transmit frame synchronization pulse is also generated to start an encode cycle, and this must occur once per transmit frame ; i.e., at an 8 kHz rate.

If $\overline{\text{PCM}}$/CNTL is high during the $\overline{\text{CS}}$ falling transition, the control register data is written to the bus. This does not affect frame synchronization.

The receive register contents may also be written back to the bus, as described in the Digital Loopback section.

Except during a WRITE cycle, the bus drivers are in TRI-STATE mode.

CONTROL REGISTER FUNCTIONS

Writing to the control register allows the user to set the various operating states of the ETC5051 and ETC5056. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select.
   Since one of three distinct clock frequencies may be used, the actual frequency must be known by the device for proper operation of the switched-capacitor filters. This is achieved by writting control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Loopback
In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in the ETC5051, ETC5056 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back onto the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.

3. Analog Loopback
In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is enterred by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.

4. Power-Down/Power-Up
The ETC5051, ETC5056 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, setting bit C4 to 0 power-up the device.

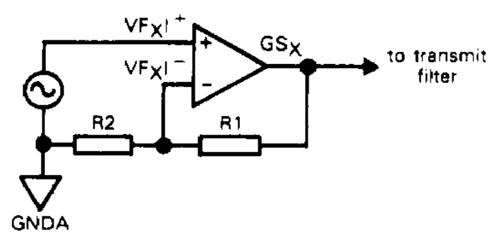
TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 2. The low noise and wide bandwidth allow gains in excess of 20dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2nd order RC active pre-filter, followed by an 8th order switched-capacitor bandpass filter clocked at 256 kHz.
The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-255 law (ETC5051) or A-law (ETC5056) coding schemes. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{max}) of nominally 2.5 V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a PCM WRITE chip select will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs.

DECODER AND RECEIVE FILTER SECTION

The receive section consists of an expanding DAC which drives a 5th order switched-capacitor low pass filter clocked at 256 kHz. The decoder is of A-law (ETC5056) or μ-law (ETC5051) coding law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter. The power amplifier output stage is capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section has unity-gain. Following a PCM READ chip select, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is - 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.



Non-inverting transmit gain = $20 \log_{10} \left(\frac{R1 + R2}{R2} \right)$

Out gain to provide peak overload level - t_{max} at GS_X (see Transmission Characteristics)

FIGURE 2 - Transmit Gain Adjustment

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
GNDD to GNDA		±0.3	V
V_{CCA} or V_{CCD} to GNDD or GNDA	V_{CC}	+7.0	V
Voltage at any analog input or output	V_{IN}, V_{OUT}	V_{CC} + 0.3 to V_{BB} − 0.3	V
Voltage at any digital input or output		V_{CC} + 0.3 to GNDD − 0.3	V
Operating temperature range	T_{oper}	− 25 to + 125	°C
Storage temperature range	T_{stg}	− 60 to + 150	°C
Lead temperature (soldering, 10 seconds)		300	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 V ±5%, V_{BB} = − 5 V ±5%, GNDA = 0 V, T_A = 0°C to 70°C (Unless otherwise noted) ; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = − 5.0 V, T_A = 25°C, all signals are referenced to GNDA.

DIGITAL INTERFACE

Characteristic	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.6	V
Input high voltage	V_{IH}	2.2	–	–	V
Output low voltage IL = 2.5 mA, DB0 - DB7	V_{OL}	–	–	0.4	V
Output high voltage IH = − 2.5 mA, DB0 - DB7	V_{OH}	2.4	–	–	V
Input low current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs)	I_{IL}	−10	–	10	μA
Input high current (V_{IH} ≤ V_{IN} ≤ V_{CC})	I_{IH}	−10	–	10	μA
Output current in high impedance state (TRI-STATE) (GNDD ≤ V_O ≤ V_{CC}), DB0 - DB7	I_{OZ}	−10	–	10	μA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)

Characteristic	Symbol	Min	Typ	Max	Unit
Input leakage current (−2.5V ≤ V ≤ +2.5V) VF_XI^+ or VF_XI^-	I_IXA	−200	–	200	nA
Input resistance (−2.5V ≤ V ≤ +2.5V) VF_XI^+ or VF_XI^-	R_IXA	10	–	–	MΩ
Output resistance (closed loop, unity gain)	R_OXA	–	1	3	Ω
Load resistance GS_X	R_LXA	10	–	–	kΩ
Load capacitance GS_X	C_LXA	–	–	50	pF
Output dynamic range (R_L ≥ 10kΩ) GS_X	V_OXA	±2.8	–	–	V
Voltage gain (VF_XI^+ to GS_X)	A_VXA	5000	–	–	V/V
Unity gain bandwidth	F_UXA	1	2	–	MHz
Offset voltage	$V_{OS}XA$	−20	–	20	mV
Common mode voltage	$V_{CM}XA$	−2.5	–	2.5	V
Common-mode rejection ratio	CMRRXA	60	–	–	dB
Power supply rejection ratio	PSRRXA	60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)

Characteristic	Symbol	Min	Typ	Max	Unit
Output resistance VF_RO	R_ORF	–	1	3	Ω
Load resistance (VF_RO = ± 2.5V)	R_LRF	600	–	–	Ω
Load capacitance	C_LRF	–	–	500	pF
Output DC offset voltage	VOS_RO	−200	–	200	mV

POWER DISSIPATION (ALL DEVICES)

Characteristic	Symbol	Min	Typ	Max	Unit
Power-down current	$I_{CC}0$	–	0.5	1.5	mA
Power-down current	$I_{BB}0$	–	0.05	0.3	mA
Active current	$I_{CC}1$	–	6.0	9.0	mA
Active current	$I_{BB}1$	–	6.0	9.0	mA

TIMING SPECIFICATIONS

Characteristic	Symbol	Value			Unit
		Min	Typ	Max	
Period of clock	t_{PC}	760	–	–	ns
Width of clock high	t_{WCH}	330	–	–	ns
Width of clock low	t_{WCL}	330	–	–	ns
Rise time of clock	t_{RC}	–	–	50	ns
Fall time of clock	t_{FC}	–	–	50	ns
Set-Up time of CLK high or low	t_{SCS}	100	–	–	ns
Hold time from $\overline{CS}$ low to CLK	t_{HCS}	100	–	–	ns
Width of chip select	t_{WCS}	100	–	–	ns
Set-Up time of $\overline{PCM}$/CNTL	t_{SPCM}	0	–	–	ns
Hold time of $\overline{PCM}$/CNTL	t_{HPCM}	100	–	–	ns
Set-Up time of data in	t_{SDI}	50	–	–	ns
Hold time of data in	t_{HDI}	20	–	–	ns
Delay time of data in ($C_L = 0$ pF to 200 pF)	t_{DDO}	90	–	260	ns
Delay time to data output disabled ($C_L = 0$ pF to 200 pF)	t_{DDZ}	20	–	80	ns

Switching Time Waveforms

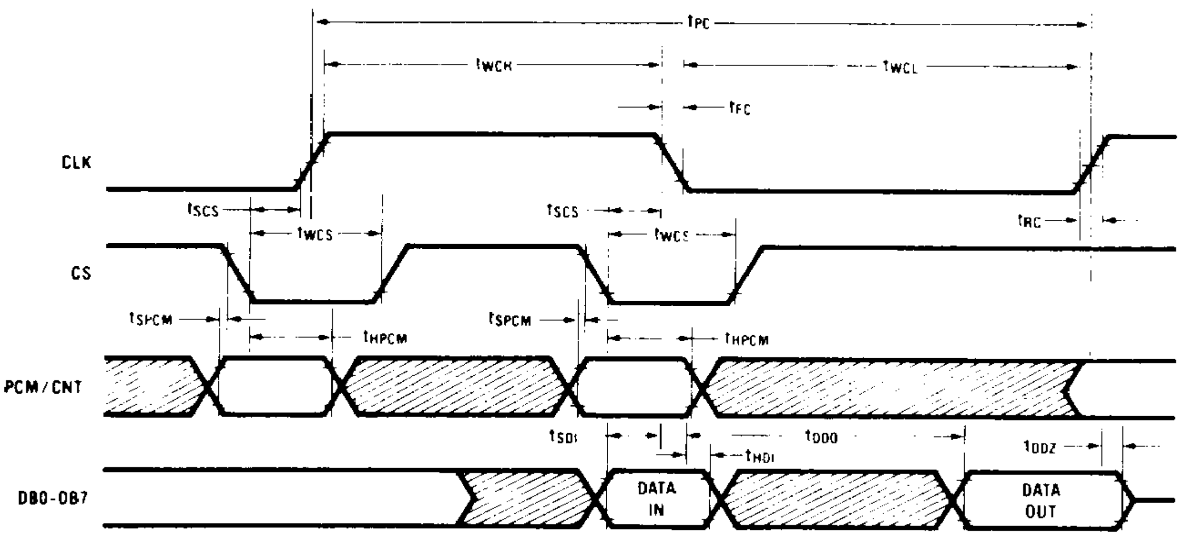


FIGURE 4. Timing Waveforms for ETC 5051, ETC 5056

TRANSMISSION CHARACTERISTICS

(All devices) T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ±5%, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

AMPLITUDE RESPONSE

Characteristic	Symbol	Min	Typ	Max	Unit
Absolute levels - Nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0 ETC5051, ETC5056		–	1.2276	–	Vrms
Max overload level 3.14 dBm0 ETC5051 3.17 dBm0 ETC5056	t_{MAX}	 – –	 2.492 2.501	 – –	V_{PK}
Transmit gain, absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V) Input at GS_X = 0 dBm0 at 1020 Hz	G_{XA}	−0.15	–	0.15	dB
Transmit gain, relative to G_{XA} f = 16Hz f = 50Hz f = 60Hz f = 180Hz f = 200Hz f = 300Hz-3000 Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up,measure reponse from 0Hz to 4000Hz	G_{XR}	 – – – −2.8 −1.8 −0.15 −0.35 −0.7 – –	 – – – – – – – – – –	 −40 −30 −26 −0.2 −0.1 0.15 0.05 0 −14 −32	dB
Absolute transmit gain variation with temperature (T_A = 0°C to +80°C)	G_{XAT}	–	–	± 0.1	dB
Absolute transmit gain variation with supply voltage (V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%)	G_{XAV}	–	–	± 0.05	dB
Transmit gain variations with level Sinusoidal test method reference level = −10dBm0 VF_XI^+ = −40dBm0 to +3dBm0 VF_XI^+ = −50dBm0 to −40dBm0 VF_XI^+ = −55dBm0 to −50dBm0	G_{XRL}	 −0.2 −0.4 −1.2	 – – –	 0.2 0.4 1.2	dB
Receive gain, absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V) Input = digital code sequence for 0dBm0 signal at 1020Hz	G_{RA}	−0.15	–	0.15	dB
Receive gain, relative to G_{RA} f = 0Hz to 3000 Hz f = 3300Hz f = 3400Hz f = 4000Hz	G_{RR}	 −0.15 −0.35 −0.7 –	 – – – –	 0.15 0.05 0 −14	dB
Absolute receive gain variation with temperature (T_A = 0°C to + 70°C)	G_{RAT}	–	–	± 0.1	dB
Absolute receive gain variation with supply voltage (V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%)	G_{RAV}	–	–	± 0.05	dB
Receive gain variations with level Sinusoidal test method;reference input PCM code corresponds to an ideally encoded −10dBm0 signal PCM level = −40dBm0 to +3dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	G_{RRL}	 −0.2 −0.4 −1.2	 – – –	 0.2 0.4 1.2	dB
Receive output drive level (R_L = 600 Ω)	V_{RO}	−2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS

(All devices) T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Characteristic	Symbol	Min	Typ	Max	Unit
Transmit delay, absolute (f = 1600Hz)	D_{XA}	–	290	315	µs
Transmit delay, relative to D_{XA}	D_{XR}				µs
f = 500Hz-600Hz		–	195	220	
f = 600Hz-800Hz		–	120	145	
f = 800Hz-1000 Hz		–	50	75	
f = 1000Hz-1600Hz		–	20	40	
f = 1600Hz-2600Hz		–	55	75	
f = 2600Hz-2800Hz		–	80	105	
f = 2800Hz-3000Hz		–	130	155	
Receive delay, absolute (f = 1600Hz)	D_{RA}	–	180	200	µs
Receive delay, relative to D_{RA}	D_{RR}				µs
f = 500Hz-1000Hz		−40	−25	–	
f = 1000Hz-1600Hz		−30	−20	–	
f = 1600Hz-2600Hz		–	70	90	
f = 2600Hz-2800Hz		–	100	125	
f = 2800Hz-3000Hz		–	145	175	

NOISE

Characteristic	Symbol	Min	Typ	Max	Unit
Transmit noise, P message weighted (ETC5056, VF_XI^+ = 0V)	N_{XP}	–	−74	−69 (Note 1)	dBm0p
Receive noise, P message weighted (ETC5056 PCM code equals positive zero)	N_{RP}	–	−82	−79	dBm0p
Transmit noise, C message weighted (ETC5051, VF_XI^+ = 0V)	N_{XC}	–	12	15	dBrnC0
Receive noise, C message weighted ETC 5054, PCM code equals alternating positive and negative zero	N_{RC}	–	8	11	dBrnC0
Noise, single frequency f = 0kHz to 100kHz, loop around measurement, VF_XI^+ = 0Vrms	N_{RS}	–	–	−53	dBm0
Positive power supply rejection, transmit VF_XI^+ = 0Vrms, V_{CC} = 5.0V_{DC}+100mVrms, f = 0kHz-50kHz	$PPSR_X$	40	–	–	dBp
Negative power supply rejection, transmit VF_XI^+ = 0Vrms, V_{BB} = −5.0V_{DC}+100mVrms f = 0kHz-50kHz	$NPSR_X$	40	–	–	dBp
Positive power supply rejection, receive (PCM code equals positive zero, V_{CC} = 5.0V_{DC}+100mVrms)	$PPSR_R$				
f = 0Hz-4000Hz		40	–	–	dBp
f = 4kHz-25kHz		40	–	–	dB
f = 25kHz-50kHz		36	–	–	dB
Negative power supply rejection, receive (PCM code equals positive zero, V_{BB} = −5.0V_{DC}+100mVrms)	$NPSR_R$				
f = 0Hz-4000Hz		40	–	–	dBp
f = 4kHz-25kHz		40	–	–	dB
f = 25kHz-50kHz		36	–	–	dB

TRANSMISSION CHARACTERISTICS (Continued)

(All devices) $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Spurious out-of-band signals at the channel output Loop around measurement, 0 dBm0, 300Hz-3400Hz input applied to VF_XI^+, measure individual image signals at VF_RO	SOS	–	–	−30	dB
4600Hz-7600Hz		–	–	−32	
7600Hz-8400Hz		–	–	−40	
8400Hz-100,000Hz		–	–	−30	
DISTORTION					
Signal to total distortion (sinusoidal test method) Transmit or receive half-channel	STD_X or STD_R				dBp
Level = 3.0dBm0		33	–	–	
= 0dBm0 to −30dBm0		36	–	–	
= −40dBm0 XMT		29	–	–	
RCV		30	–	–	
= −55dBm0 XMT		14	–	–	
RCV		15	–	–	
Single frequency distortion, transmit	SFD_X	–	–	−46	dB
Single frequency distortion, receive	SFD_R	–	–	−46	dB
Intermodulation distortion Loop around measurement, VF_XI^+ = −4dBm0 to −21dBm0, two frequencies in the range 300Hz-3400Hz	IMD	–	–	−41	dB
CROSSTALK					
Transmit to receive crosstalk, 0dBm0 transmit level f = 300Hz-3400Hz, D_R = steady PCM code	$CT_{X\text{-}R}$	–	−90	−75	dB
Receive to transmit crosstalk, 0dBm0 receive level f = 300Hz-3400Hz, VF_XI = 0V	$CT_{R\text{-}X}$	–	−90	−70 (Note 2)	dB

Note 1. Measured by extrapolation of the S/N ratio result in the first segment of the encoder.

Note 2 $CT_{R\text{-}X}$ is measured with a −40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT DATA BUS OUTPUT

	ETC5051 μ-Law (MSB … LSB)	ETC5056 True A-Law, C5 = 0 (includes Even Bit inversion) (MSB … LSB)
V_{IN} = + Full-Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} = 0 V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} = − Full-Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0
	NOT APPLICABLE (C_5 IS DON'T CARE)	SIGN + MAGNITUDE A-LAW, C_5 = 1 (Before Even bit inversion)
V_{IN} = + Full-Scale		1 1 1 1 1 1 1 1
V_{IN} = 0 V		1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
V_{IN} = − Full-Scale		0 1 1 1 1 1 1 1

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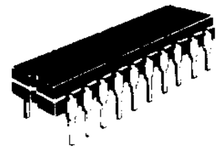

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