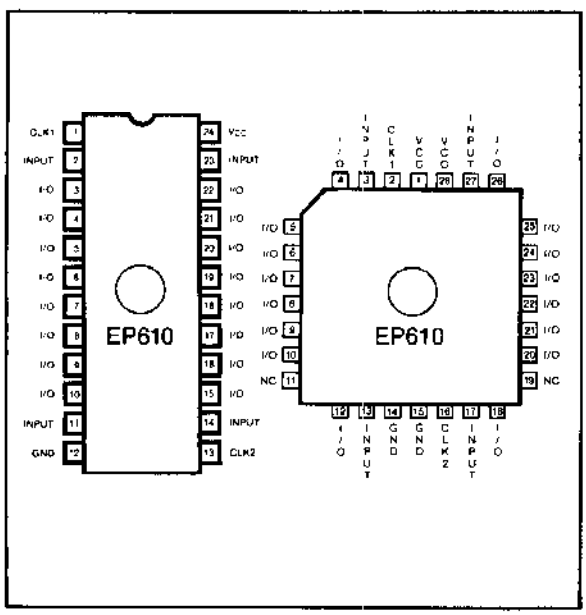
HIGH PERFORMANCE 16 MACROCELL EPLD

EP610

FEATURES

- High density (over 600 gates) replacement for TTL and 74HC.
- Advanced CMOS EPROM technology, allows erase and reprogram.
- High speed, t_{pd} = 25 ns.
- "Zero Power" (typically 10μA standby).
- Asynchronous clocking of all registers or banked register operation from 2 synchronous clocks.
- Sixteen Macrocells with configurable I/O architecture allowing 20 inputs and 16 outputs.
- Programmable registers providing D, T, SR or JK flipflops with individual Clear control.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support featuring Schematic Capture, Interactive Netlist, Boolean Equation and State Machine design entry.
- Space saving 24 pin, 300 mil, dual in-line package and 28 pin J-leaded chip carrier.

CONNECTION DIAGRAM



GENERAL DESCRIPTION

The Altera EP610 Programmable Logic Device is capable of implementing over 600 equivalent gates of SSI and MSI logic functions all in a space saving 24 pin, DIP, 300 mil package or a 28 pin J-leaded chip carrier.

The EP610 uses familiar sum-of-products logic providing a programmable AND with fixed OR structure. The device accommodates both combinatorial and sequential logic functions with up to 20 inputs and 16 outputs. The EP610 includes an Altera proprietary programmable I/O architecture providing individual selection of either combinatorial or registered output and feedback signals, active high or low.

A unique feature of the EP610 is the ability to program D, T, SR, or JK flipflop operation individually for each output without sacrificing product terms. In addition, each register can be individually clocked from any of the input or feedback paths available in the AND array. These features allow a variety of logic functions to be simultaneously implemented.

The CMOS EPROM technology reduces the power consumption to less than 20% of equivalent bipolar devices without sacrificing speed performance. Other advantages include: 100% generic testing (all devices are 100% tested at the factory). The device can be erased with ultraviolet light. Design changes are no longer costly, nor is there a need for post programming testing.

Programming the EP610 is accomplished with the use of Altera's A+PLUS development software which supports four different design entry methods. Once the circuit has been entered, the A+PLUS software performs automatic translation into logical equations, boolean minimization, and design fitting directly into an EP610.

REV. 4.0

FUNCTIONAL DESCRIPTION

The EP610 is an Erasable Programmable Logic Device (EPLD) which uses a CMOS EPROM technology to configure connections in a programmable AND logic array. The device also contains a revolutionary programmable I/O architecture which provides advanced functional capability for user programmable logic.

Externally, the EP610 provides 4 dedicated data inputs, 2 synchronous clock inputs, and 16 I/O pins which may be configured for input, output, or bi-directional operation.

Figure 1 and 2 shows the EP610 basic Macrocell and the complete block diagram. The internal architecture is organized with familiar sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from true and complement signals of the four dedicated data inputs and sixteen I/O architecture control blocks. The 40 input AND array encompasses 160 product terms which are distributed among 16 available Macrocells. Each EP610 product term represents a 40 input AND gate.

Each Macrocell contains ten product terms. Eight product terms are dedicated for logic implementation. One product term is used for Clear control of the Macrocell internal register. The remaining product term is used for Output Enable/Asynchronous Clock implementation.

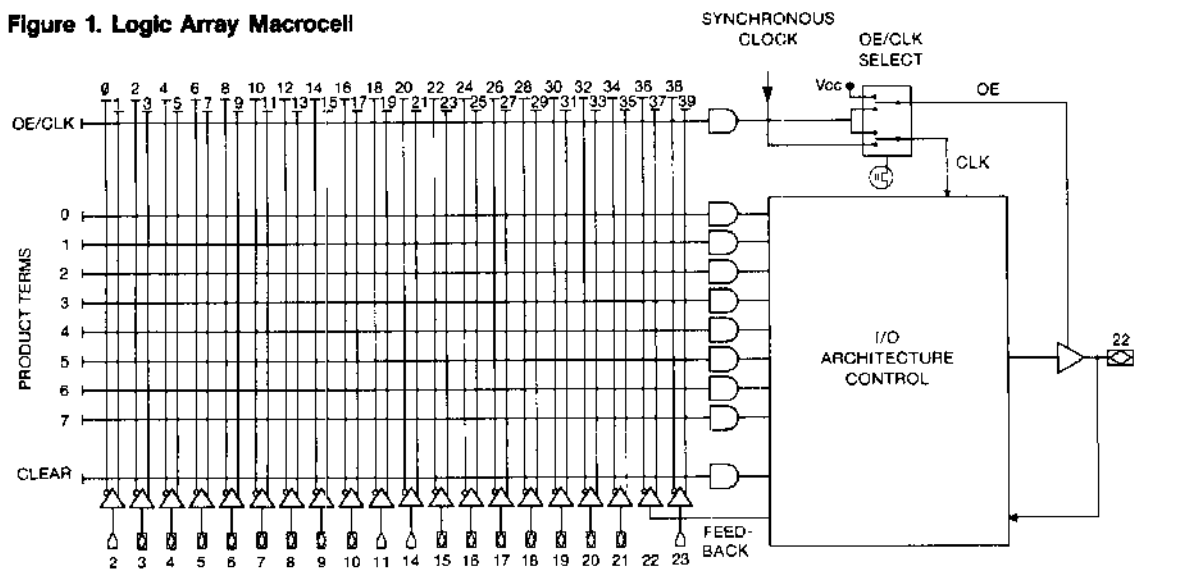
At the intersection point of an input signal and a product term there exists an EPROM connection. In the erased state, all connections are made. This means both the true and complement of all inputs are connected to each product term. Connections are opened during the programming process. Therefore, any product term may be connected to the true or complement of any array input signal. When both the true and complement of any signal is left intact, a logical false results on the output of the AND gate. If both the true and complement connections are open, then a logical "don't care" results for that input. If all inputs for the product term are programmed open, then a logical true results on the output of the AND gate.

Two dedicated clock inputs provide synchronous clock signals to the EP610 internal registers. Each of the clock signals controls a bank of eight registers. CLK1 controls registers associated with Macrocells 9-16. CLK2 controls registers associated with Macrocells 1-8. The EP610 advanced I/O architecture allows the number of synchronous registers to be user defined, from one to sixteen. Both dedicated clock inputs are positive edge triggered.

I/O ARCHITECTURE

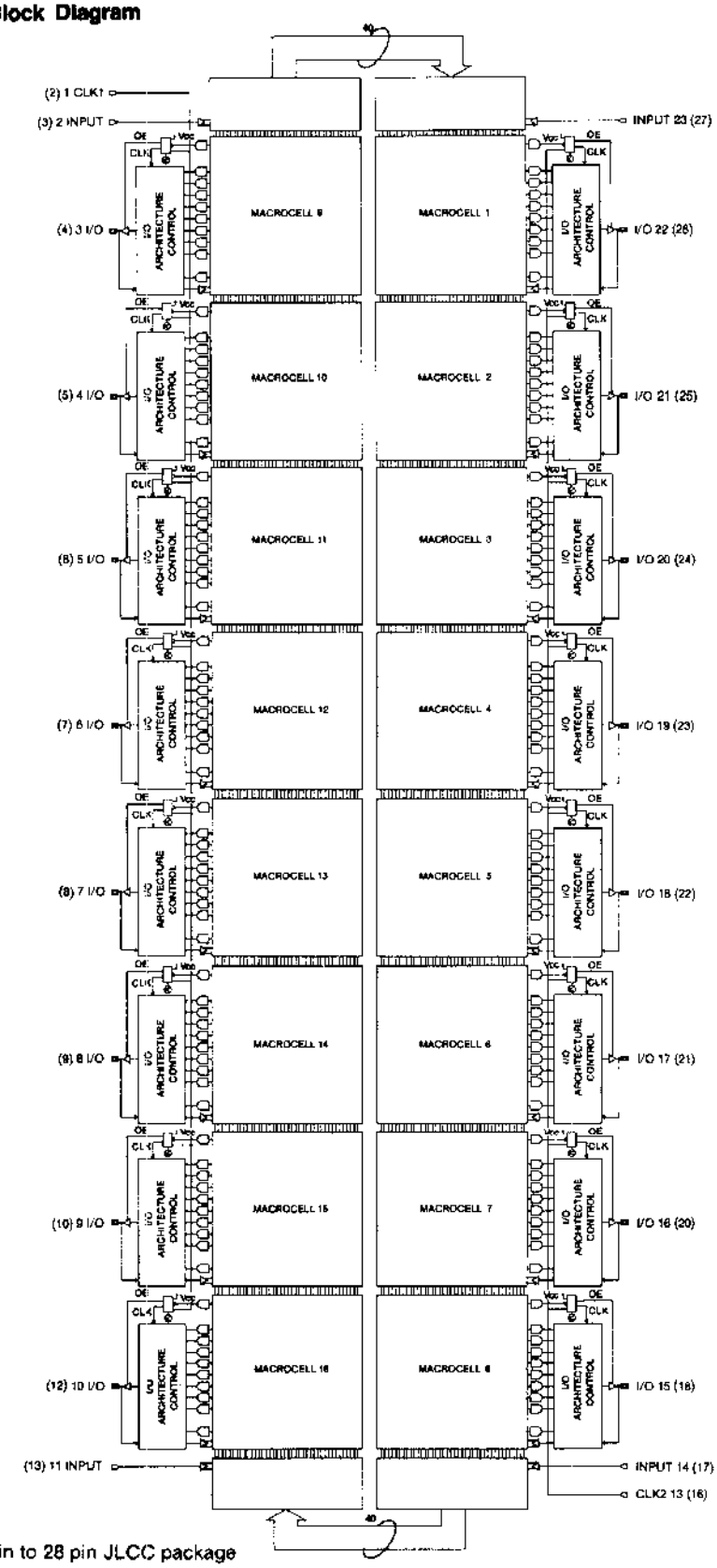
The EP610 Input/Output Architecture provides each Macrocell with over 50 possible I/O configurations. Each I/O can be configured for combinatorial or registered output, with programmable output polarity. Four different types of registers (D, T, JK, SR), can be implemented into every I/O without any additional logic requirements. I/O feedback selection can also be programmed for registered or input (pin) feedback. Another benefit of the EP610 I/O architecture is its ability to individually clock each internal register from asynchronous clock signals.

Figure 1. Logic Array Macrocell



Note: ◊ = I/O pin, in which Logic Array input is from feedback path.

Figure 2. EP610 Block Diagram



Pin #'s in ( ) pertain to 28 pin JLCC package

OE/CLK Selection

Figure 3 shows the two modes of operation which are provided by the OE/CLK Select Multiplexer. The operation of this multiplexer is controlled by a single EPROM bit and may be individually configured for each EP610 I/O pin. In Mode 0, the three-state output buffer is controlled by a single product term. If the output of the AND gate is a logical true then the output buffer is enabled. If a logical false resides on the output of the AND gate then the output buffer is seen as high impedance. In this mode the Macrocell flipflop may be clocked by its respective synchronous clock input. After erasure, OE/CLK Select Mux is configured as Mode 0.

In Mode 1, the Output Enable buffer is always enabled. The Macrocell flipflop now may be triggered from an asynchronous clock signal generated by the OE/CLK multiplexable product term. This mode allows individual clocking of flipflops from any available signal in the AND array. Because both true and complement signals reside in the AND array, the flipflop may be configured for positive or negative edge trigger operation. With the clock now controlled by a product term, gated clock structures are also possible.

OUTPUT/FEEDBACK Selection

Figure 4 shows the EP610 basic output configurations. Along with combinatorial output, four register types are available. Each Macrocell I/O may be independently configured. All registers have individual Asynchronous Clear control from a dedicated product term. When the product term is asserted to a logical one, the Macrocell register will immediately be loaded with a logical zero independently of the clock. On power up, the EP610 performs the Clear function automatically.

When the D or T register is selected, eight product terms are ORed together and made available to the register input. The Invert Select EPROM bit determines output polarity. The Feedback Select Multiplexer enables registered, I/O (pin) or no feedback to the AND array.

If the JK or SR registers are selected, the eight product terms are shared among two OR gates. The allocation of product terms for each register input is optimized by the A+PLUS development software. The Invert Select EPROM bits configures output polarity. The Feedback Select Multiplexer enables registered or no feedback to the AND array.

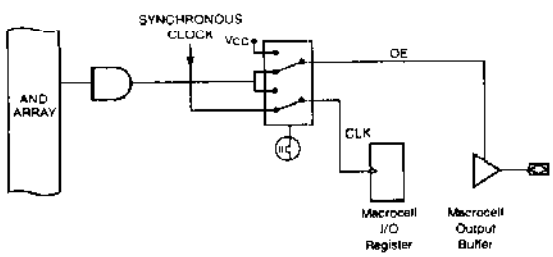
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback. No output is obtained by disabling the Macrocell output buffer.

In the erased state, the I/O is configured for combinatorial active low output with input (pin) feedback.

Figure 3. OE/CLK Select MUX

MODE Ø

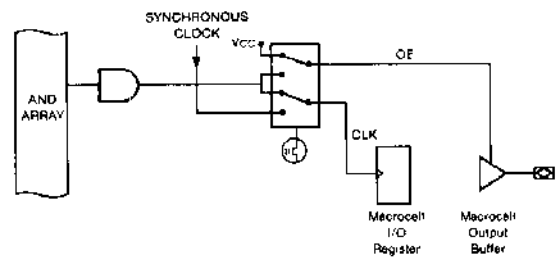
OE = P-Term Controlled
CLK = Synchronous



The register is clocked by the synchronous clock signal which is common to 7 other Macrocells. The output is enabled by the logic from the product term.

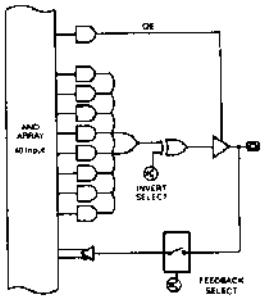
MODE 1

OE = Enabled
CLK = Asynchronous



The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP610.

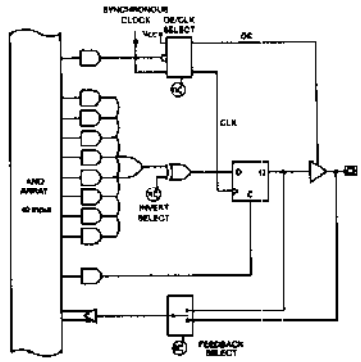
Figure 4. I/O Configurations



COMBINATORIAL

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin



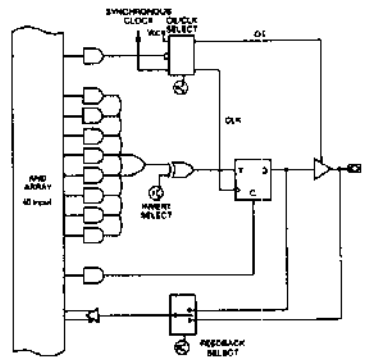
D-TYPE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D-Register/High	D-Register Pin, None
D-Register/Low	D-Register Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



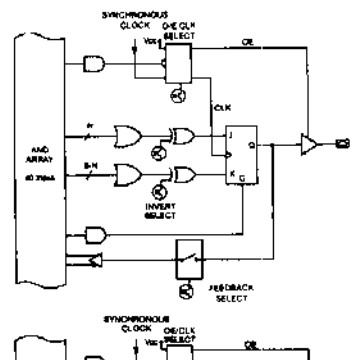
TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register / High	T-Register, Pin, None
T-Register / Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



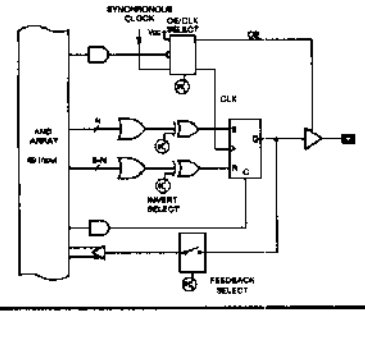
JK FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



SR FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

ABSOLUTE MAXIMUM RATINGS

COMMERCIAL, INDUSTRIAL, MILITARY OPERATING RANGES

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-175	+175	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
t_R	INPUT rise time	note (9)		500 (250)	ns
t_F	INPUT fall time	note (9)		500 (250)	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (8)		20	100 (150)	μA
I_{CC2}	V_{CC} supply current (non-turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		3	10 (15)	mA
I_{CC3}	V_{CC} supply current (turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		32	60 (75)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS

EP610-25, EP610-30,
EP610-35, EP610-40

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial, C)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial, I)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military, M)*
Note (5)

			EP610-25		EP610-30		EP610-35		EP610-40		NON-TURBO ADDER	
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	note (5)	UNIT
t_{PD1}	Input to non-registered output	C_1 = 35pF		25		30		35		40	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37		42	30	ns
t_{PZX}	Input to output enable			25		30		35		40	30	ns
t_{PXZ}	Input to output disable	C_1 = 5pF note (2)		25		30		35		40	30	ns
t_{CLR}	Asynchronous output clear time	C_1 = 35pF		27		32		37		42	30	ns
t_{IO}	I/O input buffer delay			2		2		2		2	0	ns

SYNCHRONOUS CLOCK MODE

			EP610-25		EP610-30		EP610-35		EP610-40		NON-TURBO ADDER	
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	note (5)	UNIT
f_{MAX}	Maximum frequency	note (10)	47.6		41.7		37.0		31.3		0	MHz
t_{SU}	Input setup time		21		24		27		32		30	ns
t_H	Input hold time		0		0		0		0		0	ns
t_{CH}	Clock high time		10		11		12		15		0	ns
t_{CL}	Clock low time		10		11		12		15		0	ns
t_{CO1}	Clock to output delay			15		17		20		22	0	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)			25		30		35		40	0	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	40.0		33.3		28.6		25.0		0	MHz

ASYNCHRONOUS CLOCK MODE

			EP610-25		EP610-30		EP610-35		EP610-40		NON-TURBO ADDER	
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	note (5)	UNIT
f_{MAX}	Maximum frequency	note (10)	47.6		41.7		37.0		31.3		0	MHz
t_{ASU}	Input setup time		8		8		8		10		30	ns
t_{AH}	Input hold time		12		12		12		14		0	ns
t_{ACH}	Clock high time		10		11		12		14		0	ns
t_{ACL}	Clock low time		10		11		12		14		0	ns
t_{ACO1}	Clock to output delay			27		32		37		42	30	ns
t_{ACNT}	Minimum clock period (register output feedback to register input - internal path)			25		30		35		40	0	ns
f_{ACNT}	Internal maximum frequency ($1/t_{ACNT}$)	note (7)	40.0		33.3		28.6		25.0		0	MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 13, (high voltage pin during programming), has capacitance of 50 pF max.
5. See TURBO-BIT™, page 44.
6. Figures in ( ) pertain to military and industrial temperature version.
7. Measured with device programmed as a 16 bit counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100ns after last transition).
9. Clock t_R, t_F = 250 (100) ns.
10. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE		SPEED AVAILABILITY
Commercial (0°C to 70°C)	C	EP610-25 EP610-30 EP610-35
Industrial (-40°C to 85°C)	I	EP610-40
Military (-55°C to 125°C)	M	EP610-40

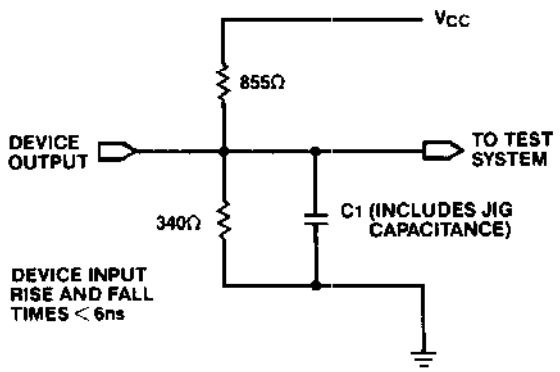
* **The specifications noted above apply to military operating range devices. MIL-STD-883 compliant product specifications are provided in military product drawings available on request from Altera marketing at 408/984-2800, ext. 101. These military product drawings should be used for the preparation of source control drawings.**

FUNCTIONAL TESTING

The EP610 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP610 allows test program patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

Figure 5. AC Test Conditions



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

DESIGN SECURITY

The EP610 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

TURBO-BIT

Some EPLDs contain a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode (Icc1) is disabled. This renders the circuit less sensitive to Vcc noise transients which can be created by the power-up/power-down cycle when operating in the low power mode. The typical Icc vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed.

If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

Figure 6. I_{CC} vs F_{MAX}

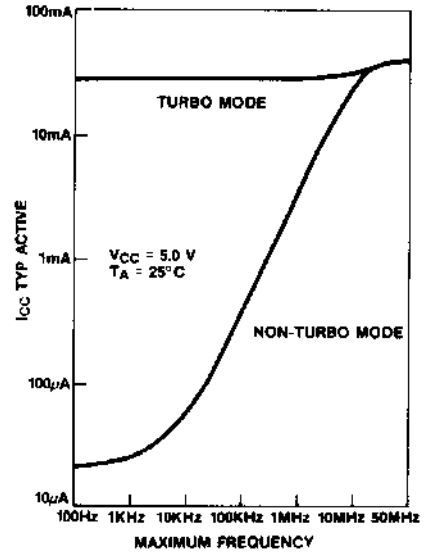


Figure 7. Output Drive Currents

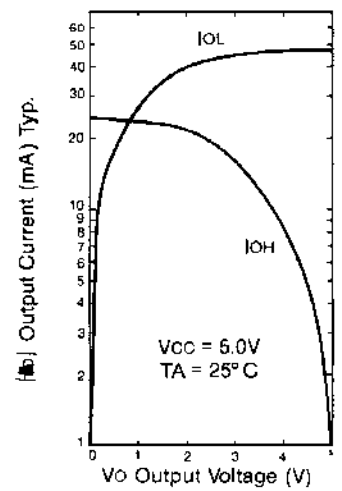
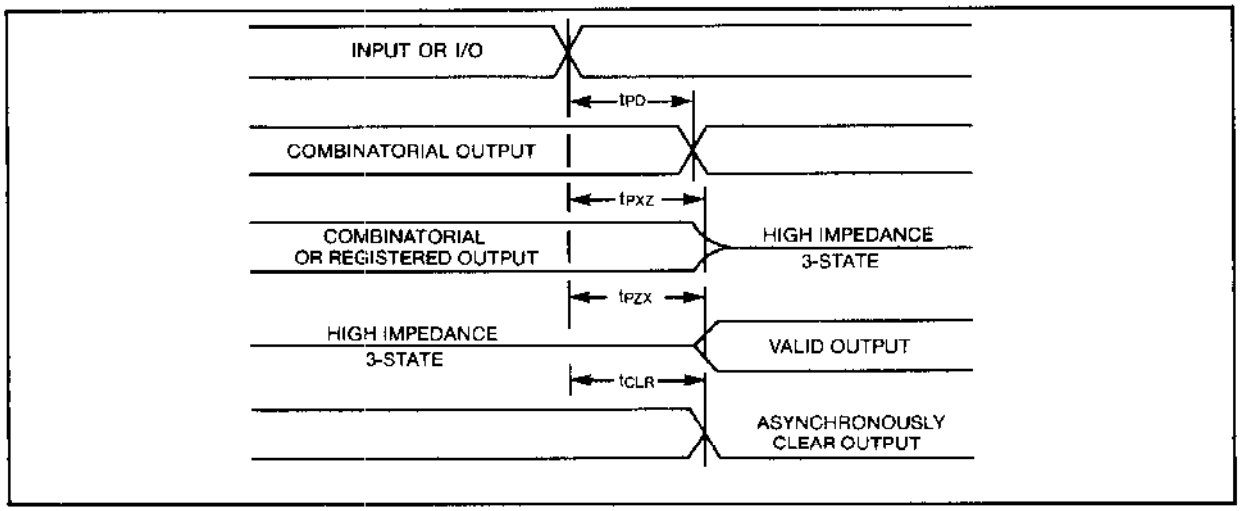
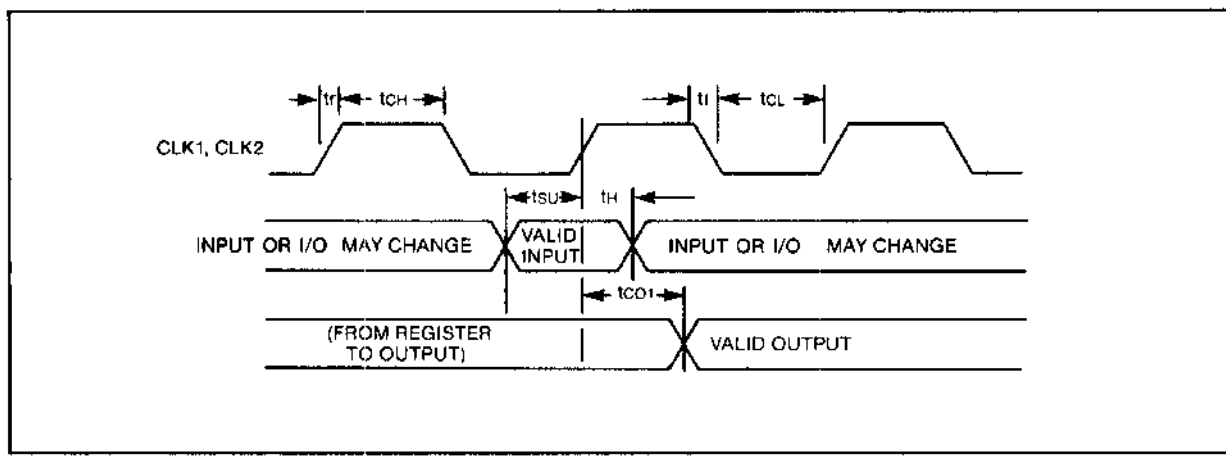


Figure 8. Switching Waveforms

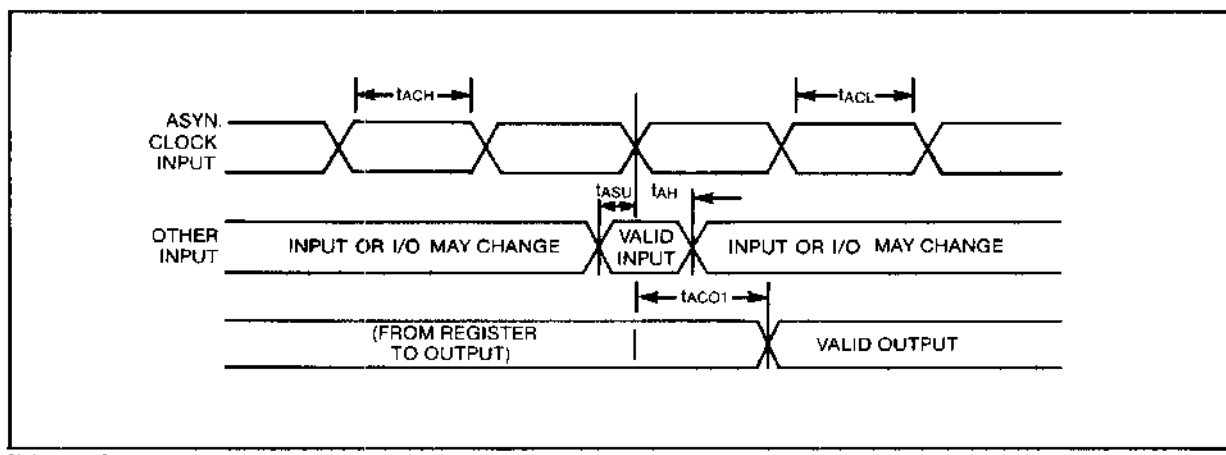
COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



ASYNCHRONOUS CLOCK MODE



Notes: t_r & $t_f < 6ns$
t_{CL} & t_{CH} measured at 0.3V and 2.7V
all other timing at 1.5V
Input voltage levels at ϕV and 3V