Edsun Continuous Edge® Graphics D-to-A Converters (CEG/DAC ™) EL171, EL471, EL478

Features

- ✓ Single-Chip Mixed-Signal Video Display Processor
  - * Triple 8-bit D/A Converters
  - * 256-Word Palette RAM
  - * Anti-Aliasing Logic
  - * Color Spectrum Generation Logic
- ✓ Full VGA Compatibility with Industry Standard:
  - * IMSG171, IMSG176, and ADV476
  - * BT471, BT476 and BT478
- ✓ Complete Implementation of CEG Level 3:
  - * Opcodes in the Bitmap for Color Mixing
  - * 4- and 8-bit Pixel Encoding Methods
  - * More than 740,000 colors with 8-bit Pixels
  - * Full Gamma Correction
- ✓ Anti-Sparkle Circuitry
- ✓ Pixel Replication Compensation
- ✓ Edsun Dynamic Palette™ for Mid-Image Color Reload
- ✓ 35, 50, and 66 MHz speeds
  - * Supports CRT Resolution up to 1024 x 768
- ✓ 5V Monolithic CMOS

Applications

- ✓ High Quality Color Graphics
- ✓ Desktop Publishing
- ✓ CAE/CAD/CAM Applications
- ✓ Image Processing

Product Description

The Edsun Laboratories Continuous Edge Graphics/Digital-to-Analog Converter (CEG/DAC) dramatically improves the images on standard color CRT monitors, while remaining fully compatible with industry-standard chips. A CEG/DAC with CEG Level 3 eliminates the "jaggies", enhances the effective resolution of the monitor, and increases the usable color range to more than 740,000 simultaneous colors (in 8-bits-per-pixel). The CEG/DAC guarantees full compatibility with standard palette DACs by powering-up in Compatibility Mode with the CEG circuitry bypassed.

The EL171, EL471 and EL478 are real-time digital signal processors that interpret pixels in the bitmap as colors and opcodes. Edsun Continuous Edge Graphics technology can blend any two colors in the palette or reassign any color in the palette in mid-image (Edsun Dynamic Palette – EDP).

Using the latest techniques in semiconductor design, the CEG/DAC chip combines three matched video-speed computation channels to simultaneously correct all three video colors (red, green and blue). Combining patented, mathematical and empirical models, the CEG/DAC provides a fully normalized gamma correction, optimized for common screen phosphors in a typical office lighting environment. Figure 1 shows the CEG/DAC block diagram.

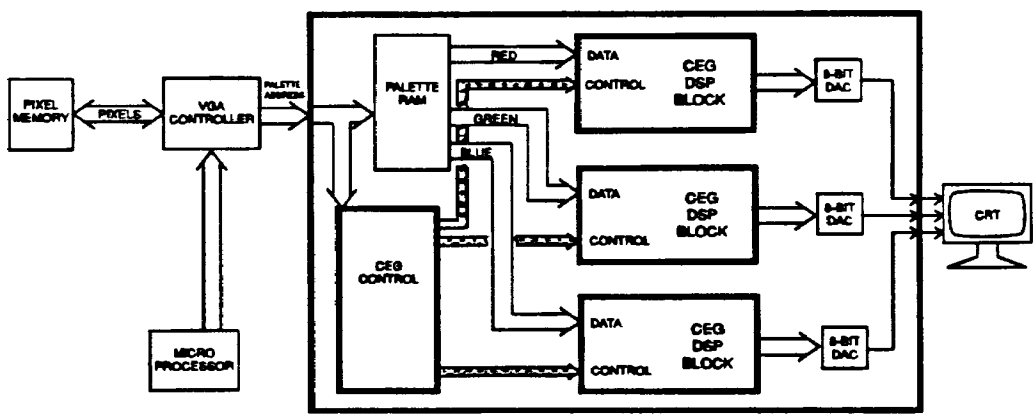

Figure 1. *CEG/DAC Functional Block Diagram*

Advance Information: *Data contained in this document is preliminary and subject to change without notice.*

Edsun Laboratories, Inc. • 564 Main Street • Waltham, MA 02154 • U.S.A.
617-647-9300, FAX: 617-894-6927

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The EL171, EL471 and EL478 provide all the current features of CEG Level 3 plus Edsun Dynamic Palette and Pixel Replication Compensation. CEG Level 3 includes:

* Color mixing
* Basic-8, Advanced-4, and Advanced-8 encoding
* Full gamma correction

The Edsun Laboratories CEG/DAC is available in a 28 pin plastic DIP package or in a 44 pin J lead PLCC package. These can be ordered in 35, 50 and 66 MHz speed grades, as shown in Table 1.

	Speeds		
Packages	35 MHz	50 MHz	66 Mhz
28-pin Plastic DIP	EL171-35		
44-pin J Lead PLCC	EL471-35	EL471-50	EL471-66
44-pin J Lead PLCC	EL478-35	EL478-50	EL478-66

Table 1. *CEG/DAC Part Numbers*

Compatibility

CEG/DACs are available in plug-compatible replacements for the most popular palette DACs, including the Inmos IMSG171 and IMSG176, the Analog Devices ADV476 and the Brooktree BT471/8. All are compatible with standard VGA video controllers.

The CEG/DAC powers-up in Compatibility Mode with the CEG circuitry bypassed, as shown in Figure 2. A software key sequence uses a reserved series of palette accesses to enable CEG. The section *Enabling CEG* describes this key sequence; Appendix A gives a program sample.

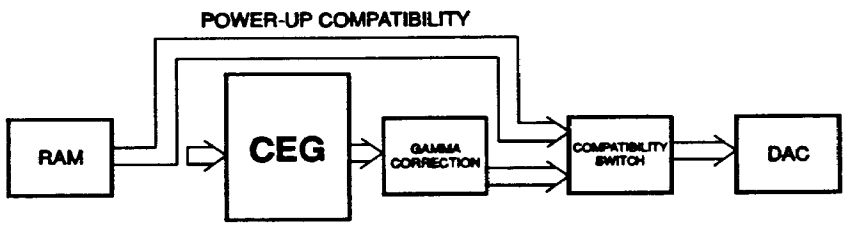


Figure 1. *Power-up Compatibility*

In Compatibility Mode, the EL171 and EL471 always uses six bits for each palette color component (red, green and blue). The EL478 uses either 6-bit or 8-bit colors, depending on the setting of the 8/~6 pin (see Table 2).

	Compatibility Mode		CEG Mode
CEG/DAC	6-bit Colors	8-bit Colors	8-bit Colors
EL171	✓		✓
EL471	✓		✓
EL478	✓	✓	✓

Table 2. *CEG/DAC Bits Per Color Component*

In 6-bit Compatibility Mode, the CEG/DAC shifts color data as it writes to and reads from the palette, as shown in Figure 3. The microprocessor writes right-justified data in D5 - D0 to the palette. In the palette, data is stored left-justified with bits D1 and D0 set to 0. During palette read operations, the six bits of color palette data are returned to the microprocessor in D5 - D0, with D7 and D6 set to 0.

The CEG mode byte, which occupies the "blue" value of palette location 223, is also shifted when it is written, but not when read. Figure 4 shows the shift effect applied to the mode byte. See *Enabling CEG* for more information about the mode byte.

All eight bits of the palette data register are significant when CEG is enabled. Set the CEG mode before writing the 8-bit color palette data to avoid the shifting operations that occur when the chip is in Compatibility Mode.

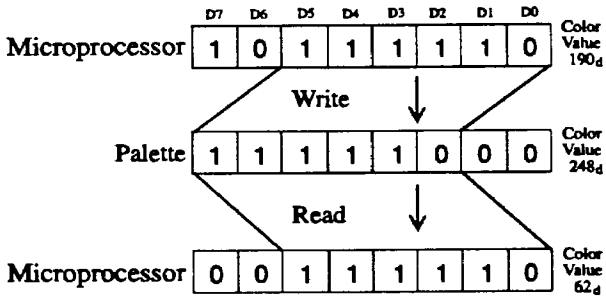


Figure 2. *Shift Operations On Palette Data*

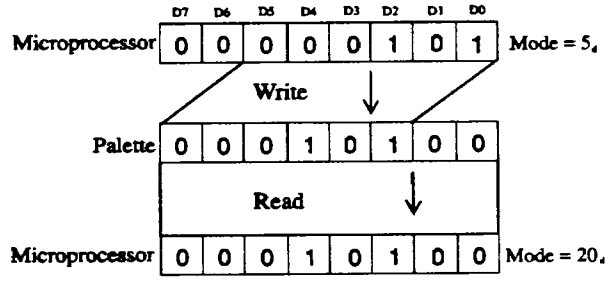


Figure 3. *Shift Operations on the Mode Byte*

Introduction to CEG

In traditional graphics systems, edge pixels are displayed in one of two abutting colors, resulting in the jagged "staircase" effect. This defect is called *aliasing*. Figure 5 shows the handling of such an edge with current computer graphics techniques. CEG solves the aliasing problem by blending the two abutting colors so that the edge (in the pixels outlined in Figure 5) is a percentage of the color to the left and the color to the right.

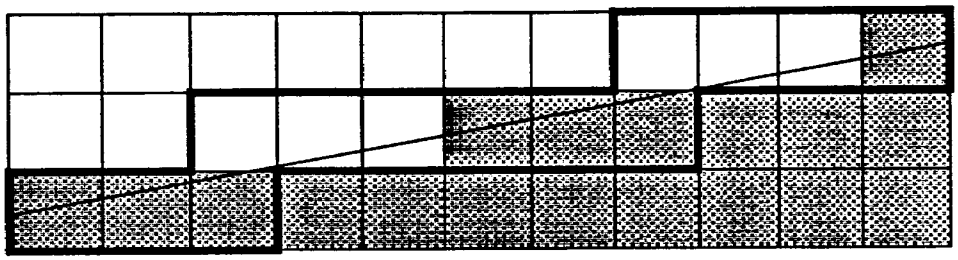


Figure 4. *Aliasing on a Typical Raster Graphics Display*

The CEG/DAC places the two edge colors in two registers, the A register and the B register. The color to the left of the edge goes into the B register, and the color to the right goes into the A register. The CEG/DAC computes a real-time weighted average on each of the colors. Figure 1 shows the functional block diagram of the entire system, and Figure 6 shows the operations performed in each DSP computation block. The adjunct publication *Continuous Edge Graphics Level 3* gives more information on mixing and the registers. The formula for calculating the mix is as follows:

Mixed Color = ((Color B * Mix) + (Color A * (31 - Mix)) + 16)/31

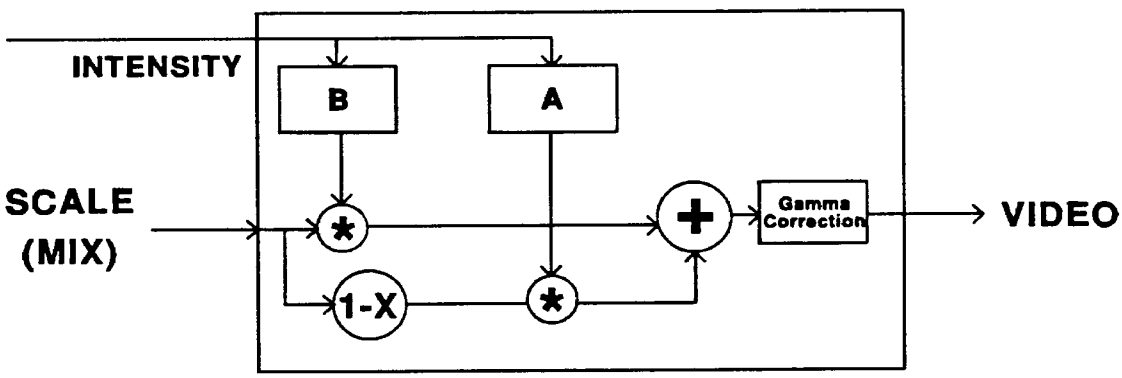


Figure 5. *DSP Block Mix Functionality*

With a CEG/DAC, opcodes for mixing and loading the dynamic palette are stored in the bitmap. If CEG is enabled, the CEG/DAC uses these opcodes to blend custom colors and to modify the palette dynamically. There are two general approaches to encoding the opcodes in the bitmap. In the first approach, the mixing and color information can be encoded together in one pixel (a simple approach, but more limited in the number of colors displayed). In the second approach, the mixing instruction is stored in one pixel and the colors in a different pixel (more complex, but allows many more colors). These two approaches are called, respectively, Basic-8 encoding and Advanced encoding. The Advanced CEG encoding methods can also use the Edsun Dynamic Palette.

By mixing colors from the palette, CEG Level 3 can display many new colors. The CEG/DAC achieves a still wider range of colors with the Edsun Dynamic Palette. When EDP is enabled, a single color number is reserved as the EDP opcode. Storing this opcode and its data into pixels allows a palette location to be changed at that point in an image.

The Edsun Laboratories CEG/DAC also provides pixel replication compensation and gamma correction. Certain VGA controllers repeat each pixel twice in low resolution modes. Because CEG requires sequences of opcodes and data, pixel replication compensation is available in CEG modes to adjust for these controllers. Gamma correction is used whenever CEG is enabled. Like ordinary palette DACs, the CEG/DAC performs no gamma correction in Compatibility Mode.

The Encoding Methods

The *Continuous Edge Graphics Level 3* describes in detail the Basic-8 encoding method, and two Advanced encoding methods. Table 3 lists the characteristics of each CEG encoding method.

Encoding Method	Bits per Pixel	Palette Colors	Mixes	CEG Colors	EDP	Notes
Basic-8	8	16 + 16	8	16*16*8 = 2048		Mixes and colors in the same pixel
Advanced-4	4	8	8	8*8*7/2 = 224	✓	Mixes and colors in different pixels
Advanced-8	8	223	32	223*32*222/2 = 792,096	✓	Mixes and colors in different pixels

Table 3. *CEG Encoding Methods*

Basic-8 encoding provides 16 colors with eight mixes, plus explicit loading of the A or B color registers. The Basic-8 method is appropriate for applications where eight bits are available and a moderate number of colors are required, such as CAD applications.

The two Advanced methods store colors and opcodes in different pixels. The Advanced-4 encoding supports 4-bits-per-pixel graphics, making it the CEG method to use in 4-bit systems such as the standard IBM VGA. Advanced-4 provides eight palette colors and eight mixes. Advanced-8 provides 223 drawing colors with full 32-mix shading. Use the Advanced-8 encoding method when there is a requirement for many colors, such as solid model rendering and computer imaging.

In the Advanced methods, an entry in the palette also can be reserved for the EDP opcode. The dynamic palette further expands the number of colors available.

Basic-8 Encoding

The Basic-8 method encodes the 16 drawing colors and eight mixes into the 8-bit pixel as shown in Figure 7. Table 4 shows the mix ratios that correspond to each pixel value in the mix field.

P7	P6	P5	P4	P3	P2	P1	P0
<------ Mix 0-7 ------>			<------> Register	<---------- Color 0-15 ---------->			

Figure 6. *Pixel Encoding for Basic-8*

The register bit selects whether the color is placed in the A register or the B register. When the register bit is set to 0, the A register is used; when the register bit is set to 1, the B register is used. The register bit also selects which portion of the palette is accessed by the color field, because the A and B registers use different palette ranges.

The color field of the pixel data refers to the first 16 colors in the palette (colors 0 - 15) when the register bit equals 0 (for the A register). When the register bit equals 1 (for the B register), the color field refers to the second 16 colors in the palette (colors 16 - 31). To find the palette location for the B register, add 16 to the color bits in P0 - P3 (for example, with the register bit = 1, color 0 refers to palette location 16). Generally, these two palette banks are loaded with the same sets of colors, but different colors can be used to double the possible number of colors.

Mix Value	Ratio	
	Color A	Color B
0	31/31	0/31
1	27/31	4/31
2	22/31	9/31
3	18/31	13/31
4	13/31	18/31
5	9/31	22/31
6	4/31	27/31
7	0/31	31/31

Table 4. *Basic-8 Mix Values*

Advanced Encoding

In the two Advanced encoding methods, the pixel contains either a color or an opcode. Mix opcodes operate on the colors in the A and B registers. The companion publication, *Continuous Edge Graphics Level 3*, describes how the two colors are stored in the registers and how they are displayed.

The Advanced-4 encoding method combines eight palette colors with eight mixes in the 4-bit pixel, providing 224 CEG colors. The four LSBs of the pixel value refer to either palette locations 0 - 7, or a mix opcode as shown in Table 5.

As shown in Figure 8, when using the Advanced-4 encoding, inputs P3 - P0 contain data, and inputs P7 through P4 are ignored.

P7	P6	P5	P4	P3	P2	P1	P0
<---------- Not considered ---------->				<---------- Color or Opcode --------->			

Figure 7. *Pixel Encoding for Advanced-4*

Mix Value	Ratio		Description
	Color A	Color B	
0	—	—	Palette color 0
1	—	—	Palette color 1
2	—	—	Palette color 2
3	—	—	Palette color 3
4	—	—	Palette color 4
5	—	—	Palette color 5
6	—	—	Palette color 6
7	—	—	Palette color 7 or EDP opcode
8	31/31	0/31	Mix opcode
9	27/31	4/31	Mix opcode
10	22/31	9/31	Mix opcode
11	18/31	13/31	Mix opcode
12	13/31	18/31	Mix opcode
13	9/31	22/31	Mix opcode
14	4/31	27/31	Mix opcode
15	0/31	31/31	Mix opcode

Table 5. *Advanced-4 Mix Values*

Advanced-8 encoding uses 8-bit pixels and offers 223 palette colors with 32 mixes, resulting in 792,096 CEG colors. The eight bits of the pixel value refer to either a color in the palette or to an opcode as shown in Table 6.

Mix Value	Ratio		Description
	Color A	Color B	
0-190	—	—	Palette colors
191	—	—	Palette color or EDP opcode
192	31/31	0/31	Mix opcode
193	30/31	1/31	.
194	29/31	2/31	.
195	28/31	3/31	.
.	.	.	.
.	.	.	.
.	.	.	.
221	2/31	29/31	.
222	1/31	30/31	.
223	0/31	31/31	Mix opcode
224-255	—	—	Palette colors

Table 6. *Advanced-8 Mix Values*

The Edsun Dynamic Palette

The two Advanced CEG encoding methods can use the Edsun Dynamic Palette, allowing the CEG/DAC to load palette colors from the bitmap. With EDP enabled, an entry from the color palette is reserved as the EDP opcode (7 in Advanced-4, 191 in Advanced-8). The data following this opcode describes the new color to load and specifies the palette address. Note that CEG/DAC addresses are ANDed with the mask register; to avoid mis-addressing an EDP entry, load the mask with 255. See *Mask Register* for more information.

The EDP opcode and data are not displayed on the screen. Instead, the color value preceding the EDP opcode is repeated in place of the palette load sequence pixels. The two pixels preceding the EDP opcode must be of the same kind (two colors or two mixes). For example, *Color, Color$_2$ EDP* is a valid sequence, but *Mix Color EDP* is not.

EDP Examples

In the Advanced-8 encoding method, an EDP sequence requires five pixels: one for the opcode (191), three for the new color, and one for the palette address. Figure 9 shows the sequence.

Pixel Number	1	2	3	4	5
Contents	EDP Opcode	New Red	New Green	New Blue	Palette Address

Figure 8. *EDP Opcode Sequence (Advanced-8)*

In 4-bits-per-pixel graphics, two pixels are needed to specify one 8-bit color value; therefore, in the Advanced-4 encoding, an EDP sequence requires eight pixels: one for the opcode (7), six for the new color (two each for red, green and blue), and one for the palette address. Figure 10 shows the EDP opcode sequence.

Pixel Number	1	2	3	4	5	6	7	8
Contents	EDP Opcode	New Red	New Red	New Green	New Green	New Blue	New Blue	Palette Address
Color Bits		R7-R4	R3-R0	G7-G4	G3-G0	B7-B4	B3-B0	

Figure 9. *EDP Opcode Sequence (Advanced-4)*

Figure 11 shows an example of an EDP opcode in Advanced-4, and how the opcode alters the palette and affects the display. In this example, the color at palette address 2 is reassigned with the EDP. As the new color is loaded into the palette, CEG displays the pixel to the left of the opcode, color 3, on the screen. After CEG loads the new color (shown as $R_2G_2B_2$) at palette address 2, it is displayed whenever color 2 is used.

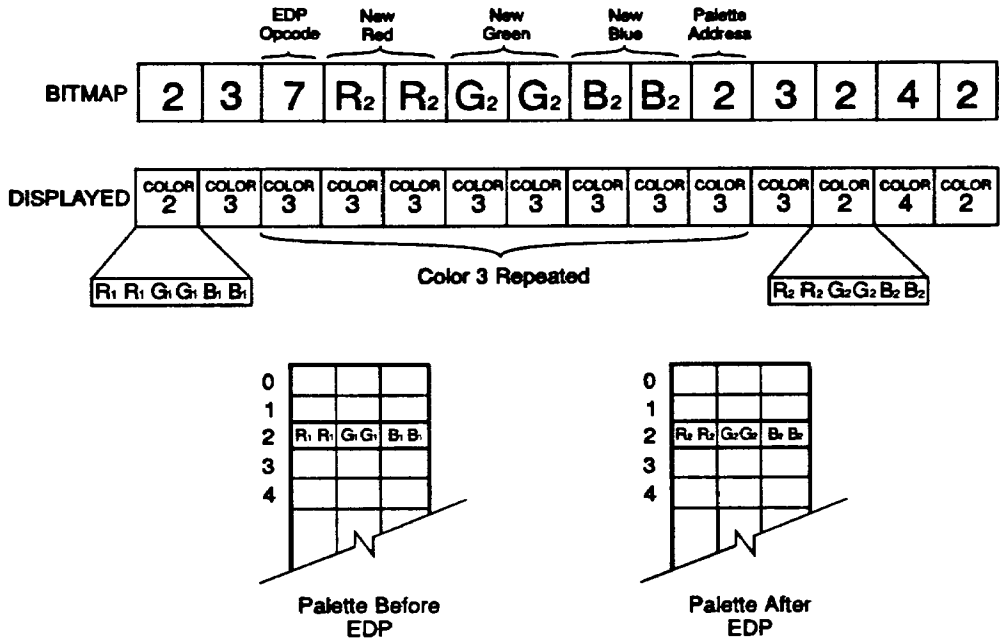


Figure 10. *EDP Opcode in the Bitmap*

Pixel Replication Compensation

Certain VGA controllers repeat each pixel twice to display low resolutions (such as 320 X 200). CEG, however, expects pixels in sequences and therefore the CEG/DAC provides pixel replication compensation to undo this duplication. When pixel replication compensation is enabled, the CEG/DAC chip samples P7-P0 every other PCLK to ignore the repeated data. Because the CEG/DAC is reversing a duplication made by the controller hardware, the compensation does not affect the graphics programmer. The bitmap is written as before. Figure 12 shows how pixel replication compensation works.

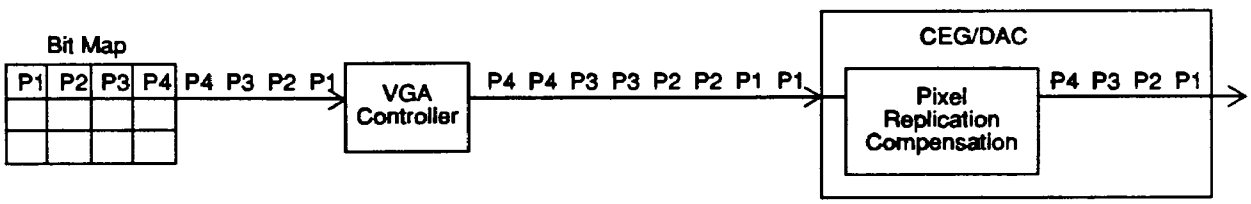


Figure 11. *Pixel Replication Compensation*

If the scan line period (video time plus BLANK time) has an even number of clock cycles, then even numbered pixels are displayed. That is, after the end of BLANK, the first pixel is ignored, the second is displayed, the third ignored, the fourth displayed, and so forth. If the scan line

period has an odd number of clock periods, then the first pixel after the end of BLANK is displayed, and the second is also displayed, and thereafter only even numbered pixels are displayed (the fourth, the sixth, etc.) Figure 13 shows which pixels are displayed under pixel replication compensation.

✓ = Pixel displayed

	Pixel						
Number of Clock Cycles	1	2	3	4	5	6	...
Even Number		✓		✓		✓	...
Odd Number	✓	✓		✓		✓	...

Figure 12. *Pixel Display*

Gamma Correction

The CEG/DAC automatically applies full gamma correction in all CEG modes to compensate for CRT characteristics. To avoid any incompatibility, gamma correction is disabled in the Compatibility Mode. The CEG/DAC uses a gamma value of 2.3 to perform gamma correction. Figure 14 shows the gamma curve.

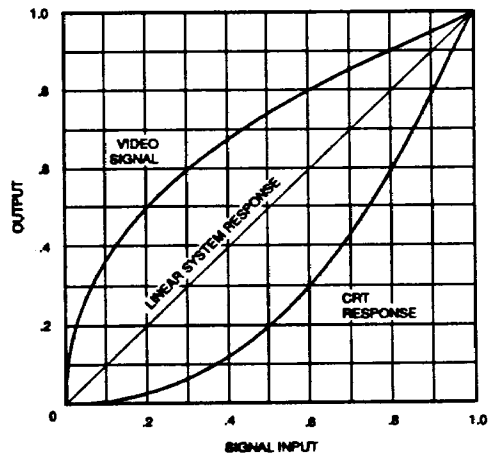


Figure 13. *Gamma Correction Curve*

CEG/DAC MODES

The CEG/DAC supports a number *modes*. A mode is a combination of attributes. The possible attributes are:

* CEG encoding (Basic-8, or Advanced-4, or Advanced-8)
* Edsun Dynamic Palette
* Pixel replication compensation

The mode is selected under software control by a key sequence followed by a mode byte.

Enabling CEG

CEG/DAC employs an unused sequence of palette accesses to enable the CEG logic. This long sequence was specially designed to prevent accidental mode changes. To enable the CEG/DAC the software must perform the following steps:

1. Write a palette RAM "read" address (222)
2. Write three specific bytes of palette RAM data
3. Repeat steps 1 and 2 twice more

There are eight bytes of special palette RAM data followed by the CEG mode byte which determines the CEG functionality. Table 7 shows the special palette RAM data and the mode byte; Table 8 shows the mode byte values. Appendix A shows the sequence of 8086/286/386 assembler code that sets the VGA CEG/DAC mode.

byte 1	byte 2	byte 3	byte 4	byte 5	byte 6	byte 7	byte 8	byte 9
67	69	71	69	68	83	85	78	mode

Table 7. *CEG Key Sequence (Decimal Values)*

The key sequence must be written exactly as shown and cannot be interrupted by any other palette access. The entire key sequence must be re-entered to change CEG modes. If the key sequence is wrong or the CEGDIS pin is high, the chip remains in Compatibility Mode. After the mode is set it can be read from palette location 223 blue. Note that, as with other palette data, the mode byte is shifted as it is written to the palette. (See *Compatibility*.)

Table 8 shows the CEG/DAC modes. Unpredictable results can occur if a mode not listed in Table 8 is used.

Mode	CEG Encoding Method	EDP	Pixel Replication
5	Basic-8		
6	Basic-8		✓
9	Advanced-4		
10	Advanced-4		✓
11	Advanced-4	✓	
13	Advanced-8		
14	Advanced-8		✓
15	Advanced-8	✓	

Table 8. *CEG/DAC Modes*

Writing palette data to location 223 immediately disables CEG operations and returns the device to full power-up Compatibility Mode (there are no side effects to this and no need to clear any registers).

Appendix A shows the 8086/286/386 assembler code that clears the CEG/DAC mode and returns the hardware to its initial power-up Compatibility Mode (in a VGA).

Mask Register

For full compatibility, when the CEG/DAC is in power-up Compatibility Mode the mask register is read and written normally. That is, values in the mask register are read back exactly as they were written.

All CEG/DAC addresses are ANDed with the mask register. In general, to avoid mis-addressing an EDP entry or other palette address, load the mask register with 255. Figure 15 shows the contents of the mask register ANDed with the palette address.

In a CEG mode, the four most significant bits of the mask register do not return the contents of the register when read. Instead, they return information about the CEG/DAC hardware version. See *Identifying a CEG/DAC* for more information about using the mask register to determine the revision code.

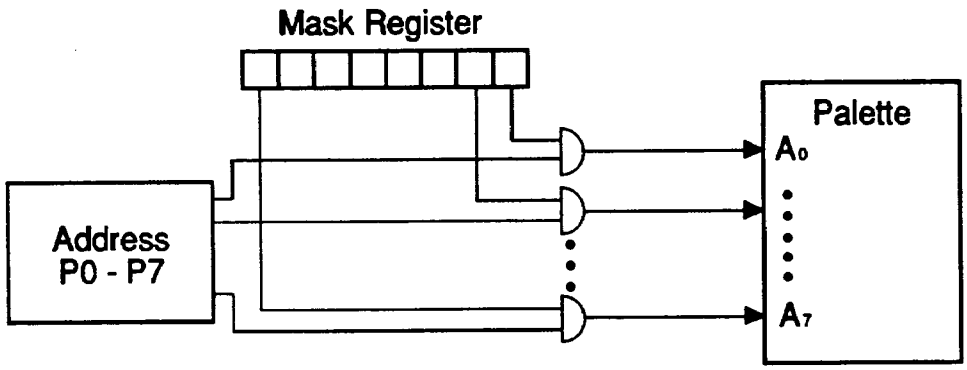


Figure 14. *Mask Register ANDed with Palette Addresses*

Identifying a CEG/DAC

Software determines whether a CEG/DAC is present by reading the mask register. Whenever a CEG mode is selected, the four most significant bits of the mask register become write-only. When read, the four most significant bits of the mask register do not relay the contents of the mask, but rather, give information about the CEG hardware installed.

Mask register bit D7 is reserved and bits D6 - D4 read back the revision code of the CEG/DAC chip. The revision number always contains at least one "0" to allow software to distinguish CEG/DAC chips from other DACs. An ordinary palette DAC returns the full eight bits of the mask register.

In other words, by enabling CEG, loading the mask register with 255, and then reading the mask register, the software can determine whether or not the hardware uses a CEG/DAC. Devices that return the value loaded (those which read back 255) do not have CEG, while those that return a different value use an Edsun Laboratories CEG/DAC. Appendix A shows sample assembler code to determine the version by inspecting the mask register.

Microprocessor Interface

The system microprocessor can access the palette address registers, palette data register, and mask register. Register select signals specify which register the microprocessor accesses, as shown in Table 9.

RS1	RS0	Microprocessor Operation
0	0	Address Register (RAM Write Mode)
1	1	Address Register (RAM Read Mode)
0	1	Color Palette Data Register
1	0	Mask Register

Table 9. *Register Select Signals*

The microprocessor should not access the palette when the palette is being loaded from the bitmap with an EDP. When using EDP, the microprocessor should perform palette reads and writes during re-trace (BLANK) time.

To write color data, the microprocessor loads the palette address register (at RS = 00) with the address of the palette location to modify. The microprocessor performs three successive write cycles to the palette data register (8-bits or 6-bits each of red, green, and blue). Following the blue write cycle, the three bytes of color information are stored in the palette location specified by the address register. The address register then increments to the next location, and that can be modified by simply writing another sequence of red, green and blue data. The address register overflows to 0 following a write cycle to palette location 255.

To read color data, the microprocessor loads the address register (at RS = 11) with the address of the palette location to read. The microprocessor then performs three successive read cycles (eight or six bits each of red, green, and blue), from the palette data register. Following the read operation, the address register increments to the next location, allowing the microprocessor to continue reading successive palette locations.

Appendix A shows the 8086/286/386 assembler code for the VGA sequence to write to the palette. Appendix A also shows the 8086/286/386 assembler code for the VGA sequence to read the palette.

Anti-Sparkle

The microprocessor interface operates asynchronously to the pixel clock and can access the palette at any time. In traditional palette DACs, when the microprocessor interrupts the pixel palette lookup, a dot appears on the screen. The CEG/DAC employs anti-sparkle logic to reduce the impact on the screen of a palette access by the microprocessor. Anti-sparkle logic compensates for this interruption by the microprocessor by repeating the currently displayed pixel. Thus, the palette may be accessed at any time with minimal disturbance to the display. Figure 16 illustrates the anti-sparkle logic.

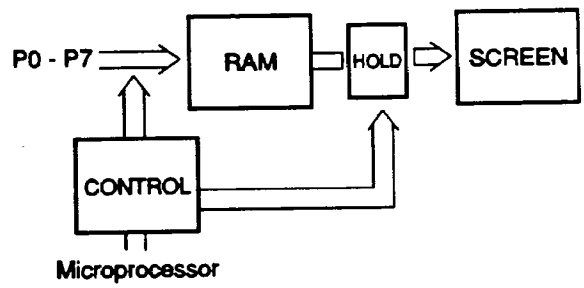
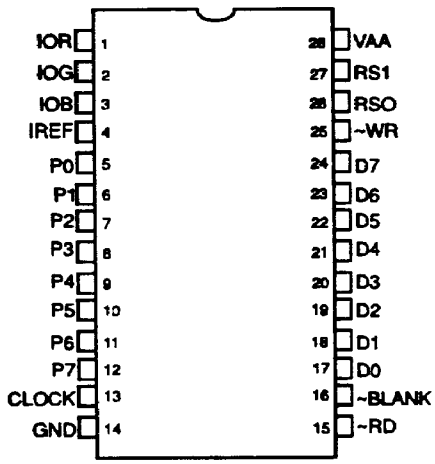


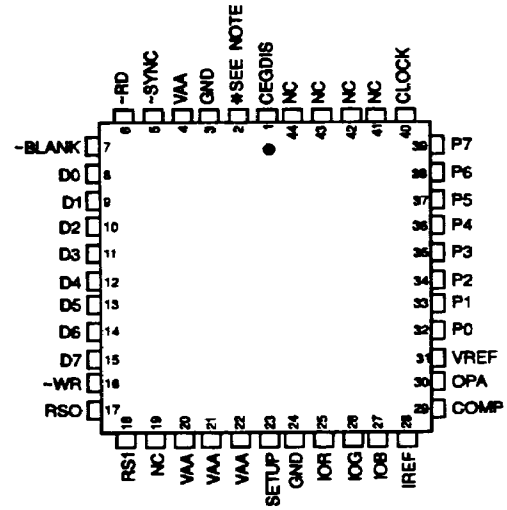
Figure 15. *Anti-sparkle Block Diagram*

PACKAGING

Pin Diagram – EL171



Pin Diagram – EL471 and EL478



*NOTE: EL471CEG - NC
EL478CEG - B/~B

Pin Descriptions

Signal	171	471	478	I/O	Description
~RD	5	6	6	I	Read control input. To read data from the device, ~RD must be a logical 0. RS0 and RS1 are latched on the falling edge of ~RD during microprocessor read operations.
~WR	25	6	6	I	Write control input. To write data to the device, ~WR must be a logical 0. RS0 and RS1 are latched on the falling edge of ~WR during microprocessor write operations. Data is latched on the rising edge of ~WR.

Signal	171	471	478	I/O	Description
RS0-RS1	26,27	17,18	17,18	I	Register select inputs. These specify the type of read or write operation performed, as described in *Microprocessor Interface.*
8/~6	—	—	2	I	6- or 8-bit palette select (EL478 only). The power-up condition (Compatibility Mode) is a 6-bit palette interface if this pin is unconnected or tied low. Strapping this pin high at power-up forces the microprocessor interface to 8-bits.
CEGDIS	—	1	1	I	CEG disable. Driving this pin high disables all CEG functions by disabling the CEG logic. This pin is internally pulled down if unconnected.
D0-D7	17-24	8-15	8-15	I/O	Host processor data bus. D0 is the LSB.
PCLK	13	40	40	I	Clock input. The rising edge of clock latches the P0-P7, BLANK, and SYNC signals. The clock input is typically the pixel clock rate of the video system.
P0-P7	5-12	32-39	32-39	I	Video data, typically from the frame buffer. In non-CEG mode one of the 256 palette colors is specified by each pixel. In CEG modes, these inputs specify either a CEG opcode or a color.
~BLANK	16	7	7	I	Blank. When this signal is low, it forces a 0 at the input to the palette DAC.
~SYNC	–	5	5	I	Composite sync control. This input switches a 40 IRE current source on the video outputs. This input floats low if left unconnected.
~SETUP	–	23	23	I	Setup control input. When low, this input disables a 7.5 IRE blanking pedestal. This pin is internally pulled down if unconnected. V_{AA} = 1 and GND = 0.
IOR	1	25	25	O	Red output. This signal can drive a doubly terminated 75 ohm load.
IOG	2	26	26	O	Green output. This signal can drive a doubly terminated 75 ohm load.

Signal	171	471	478	I/O	Description
IOB	3	27	27	O	Blue output. Can drive doubly terminated 75 ohm load.
I_{REF}	4	28	28	I	External current source input. In current mode, this input specifies the peak DAC currents. In voltage mode, it specifies full scale adjust. A resistor to ground can set the peak DAC current as described in *DAC Configuration*.
COMP	–	29	29	I	Compensation pin. If a current reference is used, connect this pin to I_{REF} and to a 0.1 µF bypass capacitor. If a voltage reference is used, connect this pin connected to OPA.
V_{REF}	–	31	31	I	Voltage reference input. If a voltage reference is used, supply a stable 1.2 volts DC. In current reference mode, leave this pin floating except for the 0.1 µF bypass capacitor.
OPA	–	30	30	O	Reference amplifier output. If a voltage reference is used, connect this output to COMP; otherwise, it should float.
V_{AA}	28	4,20, 21,22	4,20, 21,22	I	Analog power. All V_{AA} pins must be connected to the analog power plane. Power-on-reset is initiated at power-up or whenever V_{AA} dips below 1.2 volts for 10 ms and then returns to working voltage. Once reset is initiated, four clocks must pass before the chip is available for work.
GND	14	3,24	3,24	I	Analog ground. All GND pins must be connected to the analog power plane.

CEG/DAC Configuration

This section describes the CEG/DAC setup pins and the analog outputs. All models of the Edsun CEG/DAC require an external reference. Models EL471 and EL478 can be used with either a current reference or a voltage reference. Model EL171 requires a current reference.

Using a Current Reference

An external current source sets the maximum DAC output current. See Figure 17 for a circuit diagram showing current reference mode for the EL171. When using a current reference for the EL471 or EL478, leave OPA unconnected, connect V_{REF} to a 0.1 µF bypass capacitor, and tie COMP to I_{REF}, as shown in the circuit diagram in Figure 18.

The following general equation gives the maximum DAC output current :

$$I_{REF} = I_{OUTMAX}/K$$

The formulas for I_{REF} are as follows:

$I_{REF} = I_{OUTMAX}$ (mA) / 2.125	EL171
$I_{REF} = I_{OUTMAX}$ (mA) / 3.05	EL471 and EL478, SETUP = 0
$I_{REF} = I_{OUTMAX}$ (mA) / 3.22	EL471 and EL478, SETUP = 1

	RS-170 I_{OUTMAX} = 26.67mA	RS-343A I_{OUTMAX} = 19.05mA
EL171	not recommended	8.96 mA
EL471 and EL478 SETUP = 0	8.74 mA	6.25 mA
EL471 and EL478 SETUP = 1	8.28 mA	5.92 mA

Table 10. *Values for I_{REF} with a Current Reference*

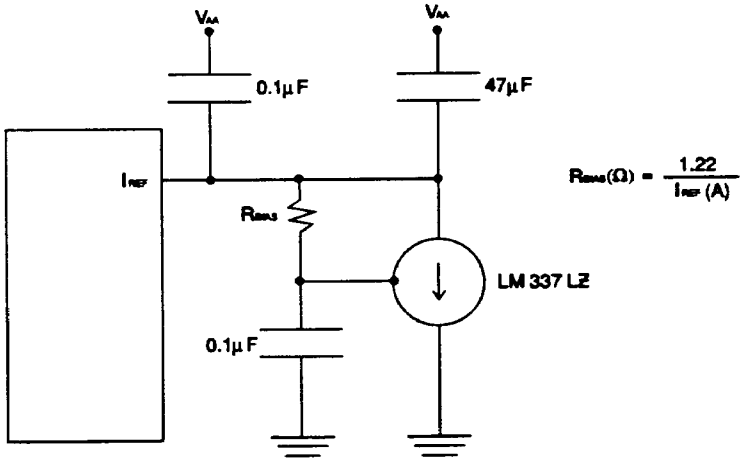


Figure 16. *Circuit Diagram – Using a Current Reference with EL171*

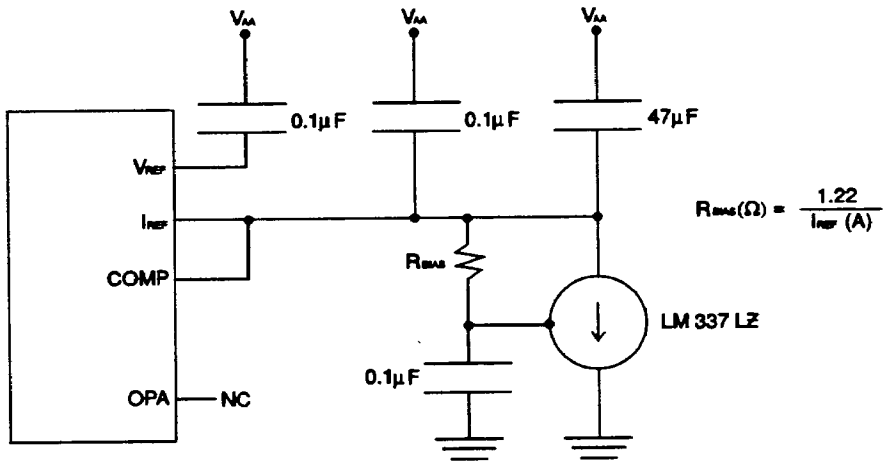


Figure 17. *Circuit Diagram – Using a Current Reference with EL471 and EL478*

Using a Voltage Reference

Models EL471 and EL478 can use a voltage reference instead of a current reference to set the maximum DAC output current. When a voltage reference is used, a stable 1.2 volt DC reference must be tied to V_{REF}, and COMP and OPA must be connected as shown in the circuit diagram in Figure 19.

The resistor R_{SET} and V_{REF} set the current from the general equation:

$$R_{SET} = V_{REF} * K / I_{OUTMAX}$$

The equations for calculating R_{SET} are as follows:

R_{SET} (ohm) = V_{REF} (V) * 3050 / I_{OUTMAX} (mA) SETUP = 0

R_{SET} (ohm) = V_{REF} (V) * 3220 / I_{OUTMAX} (mA) SETUP = 1

	RS-170 I_{OUTMAX} = 26.67 mA	RS-343A I_{OUTMAX} = 19.05 mA
SETUP = 0	137 ohm	192 ohm
SETUP = 1	145 ohm	203 ohm

Table 11. *R_{SET} Values (V_{REF} = 1.2 V)*

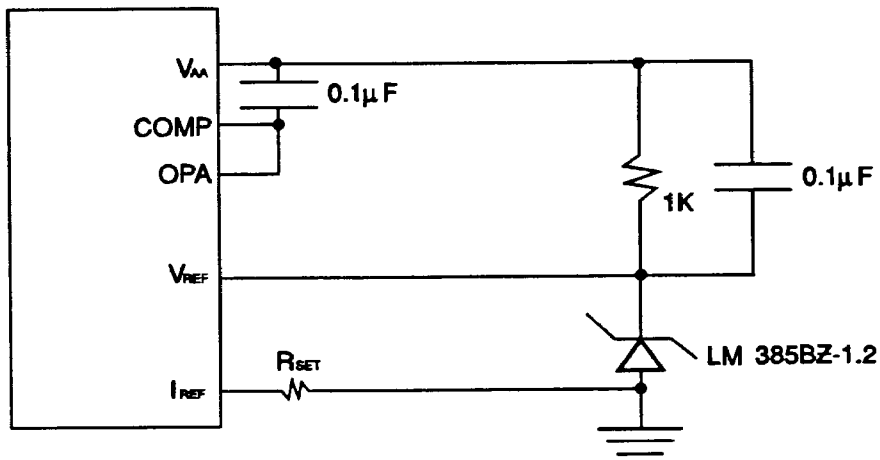
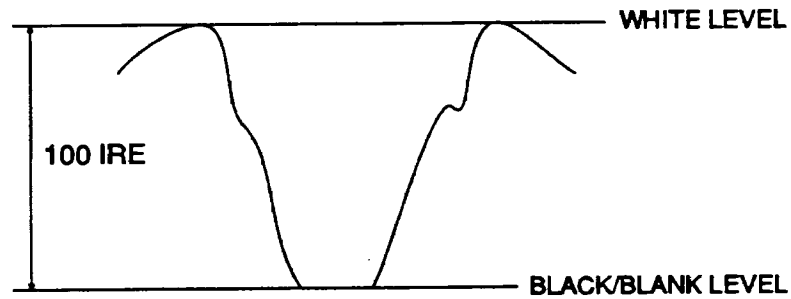


Figure 18. *Circuit Diagram – Using a Voltage Reference for EL471 and EL478*

Video Output

The data and control signals determine the video output levels. The following tables and diagrams describe the DAC outputs that correspond to various configurations.

mA	V
19.05	0.714
0.00	0.000



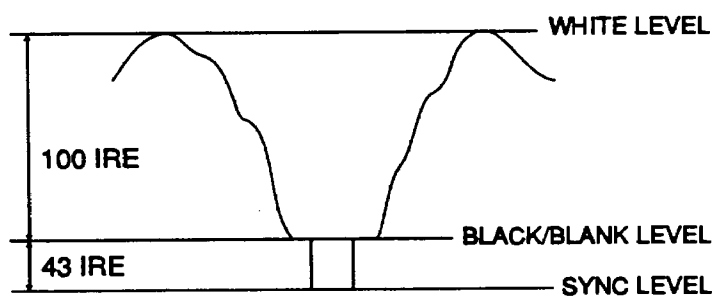
Notes:
1. Connected with a 75 ohm doubly terminated load.
2. Current reference adjusted for 19.05 mA full-scale output.
3. RS-343A levels and tolerances assumed on all levels.
4. The ~BLANK input is pipelined to maintain synchronization with the pixel data.

Figure 19. *Composite Video Output Waveform – EL171*

DAC In	~BLANK	I_{OUT} (mA)	Description
255	1	19.05	White Level
data	1	0.074 * data	Data
0	XX	0	Black Level
XX	0	0	Blank Level

Table 12. *Output Current – EL171*

mA	V
26.26	1.000
8.07	0.302
0.00	0.000

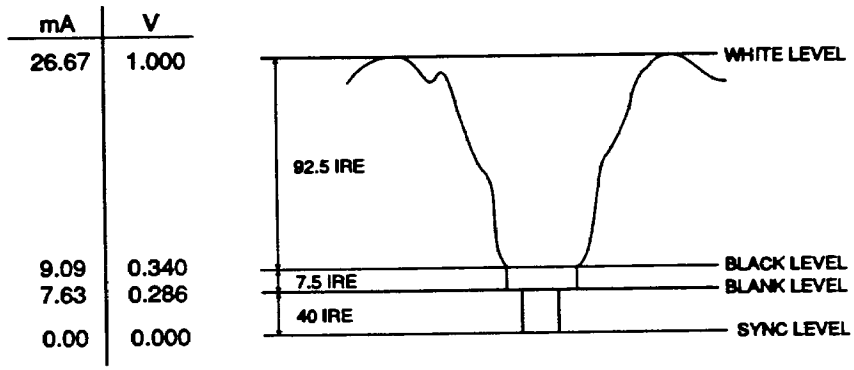


Notes:
1. Connected with a 75 ohm doubly terminated load, SETUP = 0.
2. External voltage or current reference adjusted for 26.67 mA full-scale output.
3. RS-170 levels and tolerances assumed on all levels.
4. The ~BLANK input is pipelined to maintain synchronization with the pixel data.

Figure 20. *Composite Video Output Waveform – EL471 and EL478 (SETUP = 0)*

DAC In	~SYNC	~BLANK	I_{OUT} (mA)	Description
255	1	1	26.67	White Level
data	1	1	(0.073 * data) + 8.07	Data
data	0	1	0.073 * data	Data & Sync
0	1	1	8.07	Black Level
0	0	1	0	Black & Sync
XX	1	0	8.07	Blank Level
XX	0	0	0	Sync Level

Table 13. *Output Current – EL471 and EL478 (SETUP = 0 and I_{OUTMAX} = 26.67 mA)*



Notes:
1. Connected with a 75 ohm doubly terminated load, SETUP = 1.
2. External voltage or current reference adjusted for 26.67 mA full-scale output.
3. RS-170 levels and tolerances assumed on all levels.
4. The ~BLANK input is pipelined to maintain synchronization with the pixel data.

Figure 21. *Composite Video Output Waveform – EL471 and EL478 (SETUP = 1)*

DAC In	~SYNC	~BLANK	I_{OUT}(mA)	Description
255	1	1	26.67	White Level
data	1	1	(0.069 * data) + 9.09	Data
data	0	1	(0.069 * data) + 1.46	Data & Sync
0	1	1	9.09	Black Level
0	0	1	1.46	Black & Sync
XX	1	0	7.63	Blank Level
XX	0	0	0	Blank & Sync

Table 14. *Output Current – EL471 and EL478 (SETUP = 1)*

OPERATING PARAMETERS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Storage Temperature	Ts		-50		+150	°C
Junction Temperature	TJ		+125			°C
Power Supply Voltage	V_{AA}		-0.5		7.0	V
Input Voltage (any input)	VI		-0.5		V_{AA}+0.5	V

Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Ambient Operating Temp.	Ta		0	25	+70	'C
Power Supply	V_{AA}		4.5	5.0	5.5	V
DAC Output Load	R_L		33	37.5		Ohms
Voltage Reference	V_{REF}		1.1	1.200	1.3	V
Current Reference	I_{REF}		-3	-7	-10	mA

DAC Performance

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution			8			bits
Accuracy			±.5			LSB
Differential Linearity			±.5			LSB
Output Current	Idomax		17.3		27	mA
White Current-Black Current			17.3	17.62	18.9	mA
Black Current-Blank Current		SETUP = V_{AA}	0.95	1.44	1.9	mA
		SETUP = GND	0		50	uA
Blank Level	Iblank			5	50	uA
Sync Level	Isync			2	50	uA
DAC Matching					5	%
Output Compliance	Vdo		-1.0		+1.5	V
Output Impedance	Zdo			10		KOhm
Output Capacitance	Cdo				30	pF
Power Supply Rejection Ratio	PSRR	Ido vs V_{AA}			.5	% + %
Glitch Energy				150		pV-sec
Feedthrough					-20	dB

DC Electrical Parameters

Guaranteed over Ta and V_{AA}, I_{REF} = typical.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{AA}			200	350	mA
Input Low Voltage	Vil		-0.5		0.8	V
Input High Voltage	Vih		2.0		V_{AA}+.5	V
Input Current (low) [1]	Iil	Vil = 0.8 V			0.2	mA
Input Current (high) [1]	Iih	Vih = 2.0 V			0.2	mA
Input Current (low) [2]	Iil	Vil = 0.8 V			1	nA
Input Current (high) [2]	Iih	Vih = 2.0 V			1	nA
Output Voltage (low)	Vol	Iol = 3.2 mA			0.4	V
Output Voltage (high)	Voh	Ioh = -.4 mA	2.4			V
Tri-State Leakage (D7-D0)	Iz			50	100	nA
Input Capacitance	C_{IN}	1 MHz			7	pf

Notes:

1. For EL471 and EL478, this parameter applies to the following input pins: SETUP, 8/~6, ~BLANK, CEGDIS, and ~SYNC. For EL171, it applies to BLANK.
2. This parameter applies to all other inputs not mentioned in Note 1.

AC Electrical Parameters

Guaranteed over Ta, V_{AA}, all conditions = typical.

		-35 Devices		-50 Devices		-66 Devices		
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
RS Setup Time	t1	10		10		10		ns
RS Hold Time	t2	10		10		10		ns
~RD to Data Bus Driven	t3	5		5		5		ns
~RD to Data Valid	t4		40		40		40	ns
~RD to Data Bus Tri-State	t5		20		20		20	ns
Read Data Hold Time	t6	5		5		5		ns
Write Data Setup Time	t7	10		10		10		ns
Write Data Hold Time	t8	10		10		10		ns
~RD, ~WR Pulse Width Low	t9	50		50		50		ns
~RD, ~WR Pulse Width High	t10	4*t13		4*t13		4*t13		ns
Pixel and Control Setup Time	t11	5		4		3		ns
Pixel and Control Hold Time	t12	5		4		3		ns
Clock Cycle Time	t13	28		20		15		ns
Clock Pulse Width High	t14	12		8		6		ns
Clock Pulse Width Low	t15	12		8		6		ns
Analog Output Delay	t16		30		30		30	ns
Analog Output Rise/Fall Time	t17		10		8		6	ns
Analog Output Settling Time †	t18		35		35		35	ns
Pipeline Delay								
(Compatibility Mode)	t19	3*t13		3*t13		3*t13		ns
(CEG Mode)	t19	6*t13		6*t13		6*t13		ns

Note: † ± 1 LSB

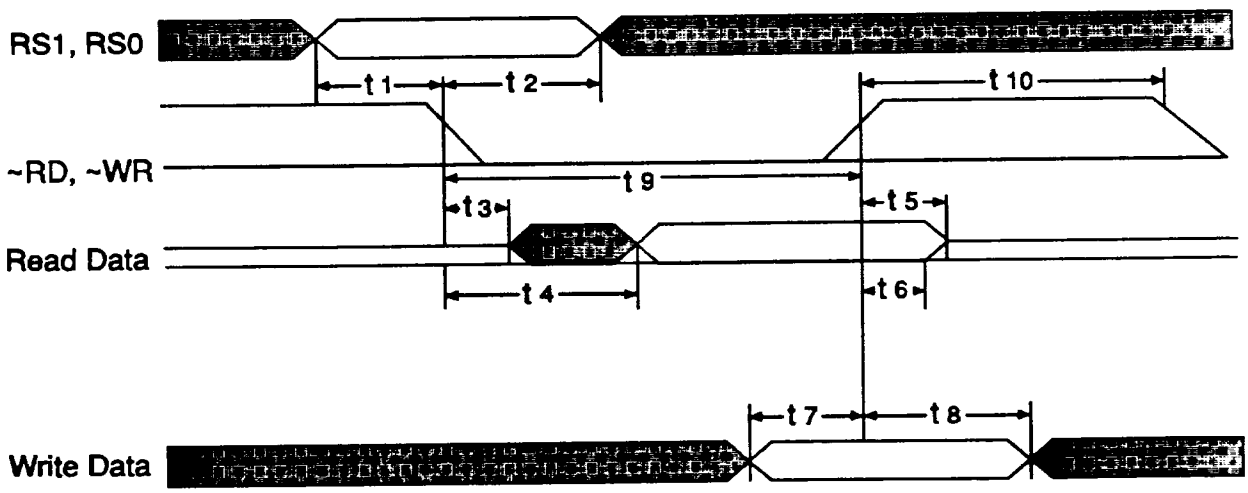


Figure 22. *Microprocessor Interface Timing*

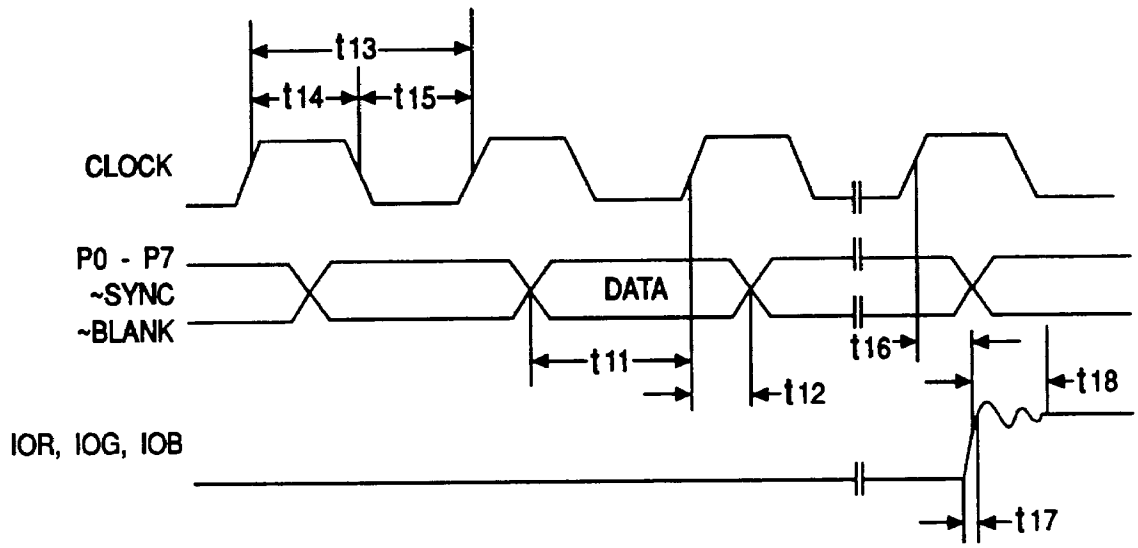


Figure 23. *Video Input/Output Timing*