

**NMOS SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)****DESCRIPTION**

The EF 6852 synchronous serial data adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organised systems such as the 6800 microprocessor systems.

The bus interface of the EF 6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

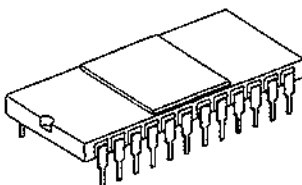
**MAIN FEATURES**

- Programmable interrupts from transmitter, receiver, and error detection logic.
- Character synchronization on one- or two-sync codes.
- External synchronization available for parallel-serial operation.
- Programmable sync code register.
- Up to 1.5 MHz transmission.
- Peripheral/modem control functions.
- Three bytes of FIFO buffering on both transmit and receive.
- 7-, 8-, or 9-bit transmission.
- Optional even and odd parity.
- Parity, overrun, and underflow status.

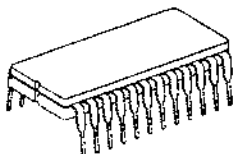
**SCREENING / QUALITY**

This product is manufactured in full compliance with either:

- MIL-STD-883 (class B).
- NFC 96863 class G.
- or according to TMS standards.



**C suffix  
DIL 24  
Ceramic Side Brazed package**



**J suffix  
DIL 24  
Ceramic Cerdip package**



**E suffix  
LCCC 28  
Leadless Ceramic Chip Carrier package**

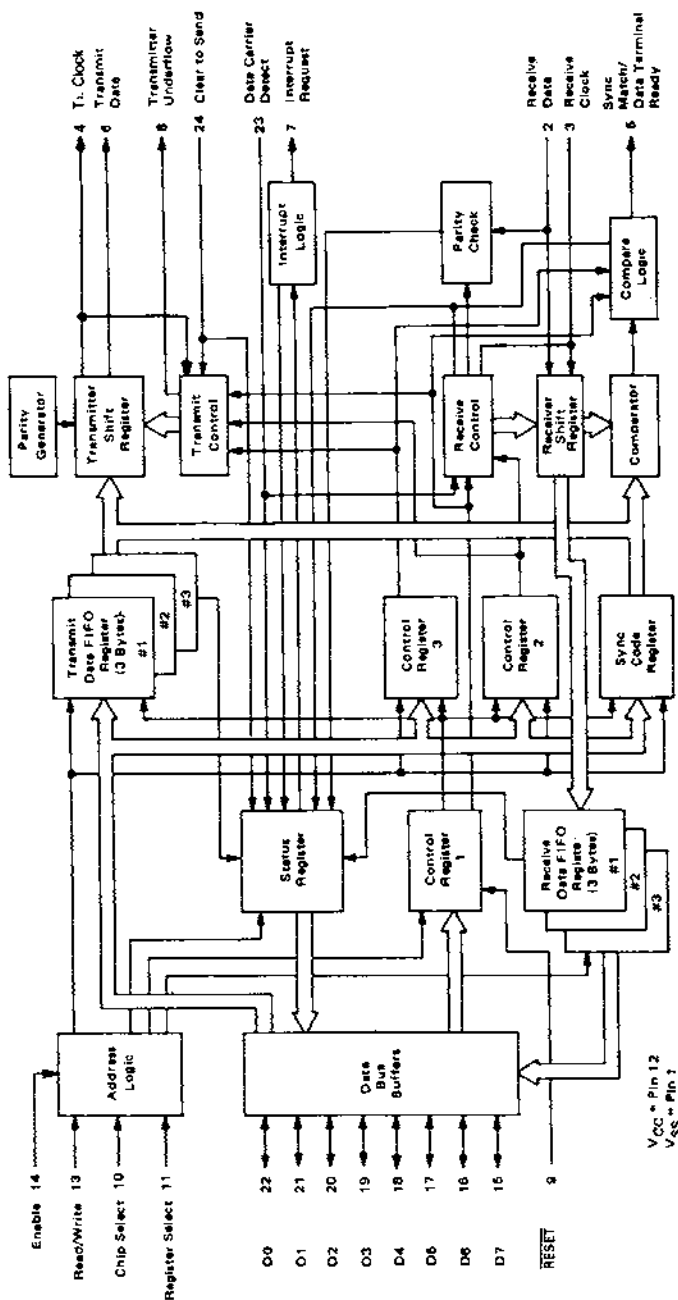
See the ordering information page 21.

Pin connection : see page 20.

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Figure 1: Expanded block diagram.

## A - GENERAL DESCRIPTION

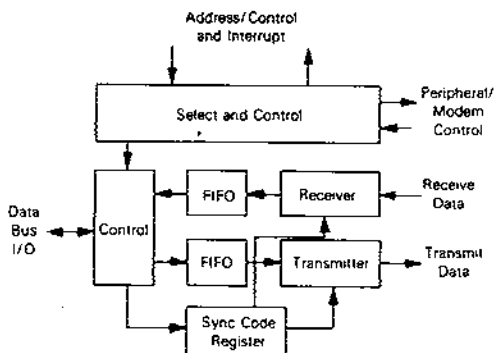


Figure 2: Synchronous serial data adapter block diagram.

## B - DETAILED SPECIFICATIONS

### 1 - SCOPE

This drawing describes the specific requirements for the peripherals EF 6852, 1 and 1.5 MHz, in compliance either with MIL-STD-883 class B.

### 2 - APPLICABLE DOCUMENTS

#### 2.1 - MIL-STD-883

- 1) MIL-STD-883 : test methods and procedures for electronics
- 2) MIL-M-38510 : general specifications for microcircuits

### 3 - REQUIREMENTS

#### 3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

#### 3.2 - Design and construction

##### 3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in § 10.1 and § 10.2.

##### 3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-M-38510 except finish C (as described in 3.5.6.1 of 38510).

##### 3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-M-38510 appendix C (when defined):

- 24 leads DIP Ceramic side brazed
- 24 leads DIP Ceramic cerdip
- 24 terminals SQ-LCCC.

The precise case outlines are described on pages 19 and 20.



## 3.3 - Electrical characteristics

## 3.3.1 - Absolute maximum ratings (see Table 1)

Table 1

Symbol	Parameter	Test conditions	Min	Max	Unit	
V <sub>CC</sub>	Supply voltage		-0.3	+7.0	V	
V <sub>I</sub>	Input voltage		-0.3	+7.0	V	
P <sub>dmax</sub>	Max Power dissipation	T <sub>case</sub> = -55°C		630	W	
		T <sub>case</sub> = +125°C		450	mW	
T <sub>case</sub>	Operating temperature	M suffix : EF 6852/EF 68A52	f = 1 and 1.5 MHz	-55	+125	°C
		V suffix : EF 6852/EF 68A52	f = 1 and 1.5 MHz	-40	+85	°C
		No suffix : EF 6852/EF 68A52	f = 1 and 1.5 MHz	0	+70	°C
T <sub>stg</sub>	Storage temperature		-55	+150	°C	
T <sub>J</sub>	Junction temperature			+180	°C	
T <sub>leads</sub>	Lead temperature	Max 5 sec. soldering		+270	°C	

**Note :** This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>CC</sub>).

## 3.4 - Thermal characteristics (at 25°C)

Table 2

Package	Symbol	Parameter	Value	Unit
DIL 24	θ <sub>JA</sub>	Thermal resistance - Ceramic junction to ambient	62	°C/W
	θ <sub>JC</sub>	Thermal resistance - Ceramic junction to case	15	°C/W
LCCC 28	θ <sub>JA</sub>	Thermal resistance - Ceramic junction to ambient	90	°C/W
	θ <sub>JC</sub>	Thermal resistance - Ceramic junction to case	18	°C/W

## Power considerations

The average chip junction temperature, T<sub>J</sub>, in °C can be obtained from :

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

T<sub>A</sub> = Ambient Temperature, °C

θ<sub>JA</sub> = Package Thermal Resistance, Junction-to-Ambient, °C/W

P<sub>D</sub> = P<sub>INT</sub> + P<sub>I/O</sub>

P<sub>INT</sub> = I<sub>CC</sub> × V<sub>CC</sub>, Watts — Chip Internal Power

P<sub>I/O</sub> = Power Dissipation on Input and Output Pins — User Determined

For most applications P<sub>I/O</sub> < P<sub>INT</sub> and can be neglected.

An approximate relationship between P<sub>D</sub> and T<sub>J</sub> (if P<sub>I/O</sub> is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P<sub>D</sub> (at equilibrium) for a known T<sub>A</sub>. Using this value of K, the values of P<sub>D</sub> and T<sub>J</sub> can be obtained by solving equations (1) and (2) iteratively for any value of T<sub>A</sub>.

The total thermal resistance of a package (θ<sub>JA</sub>) can be separated into two components, θ<sub>JC</sub> and θ<sub>CA</sub>, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ<sub>JC</sub>) and from the case to the outside ambient (θ<sub>CA</sub>). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ<sub>JC</sub> is device related and cannot be influenced by the user. However, θ<sub>CA</sub> is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ<sub>CA</sub> so that θ<sub>JA</sub> approximately equals θ<sub>JC</sub>. Substitution of θ<sub>JC</sub> for θ<sub>JA</sub> in equation (1) will result in a lower semiconductor junction temperature.

### 3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

### 3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

#### 3.6.1 - Thomson logo

#### 3.6.2 - Manufacturer's part number

#### 3.6.3 - Class B identification

#### 3.6.4 - Date-code of inspection lot

#### 3.6.5 - ESD identifier if available

#### 3.6.6 - Country of manufacturing

## 4 - QUALITY CONFORMANCE INSPECTION

### 4.1 - MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

## 5 - ELECTRICAL CHARACTERISTICS

### 5.1 - General requirements

All static and dynamic electrical characteristics specified. For inspection purpose, refer to relevant specification :

Table 3 : Static electrical characteristics for all electrical variants. See § 5.2.

Table 4 : Dynamic electrical characteristics. See § 5.3.

For dynamic characteristics, test methods refer to IEC 748-2 method number, where existing.

### 5.2 - Static characteristics

Table 3

$V_{CC} = 5.0 V_{dc} \pm 5\%$  ;  $V_{SS} = 0 V_{dc}$  ;  $T_C = -55^{\circ}C / +125^{\circ}C$  or  $-40^{\circ}C / +85^{\circ}C$  (See Figures 5 and 9)

Symbol	Characteristic	Min	Typ	Max	Unit
$V_{IH}$	Input high voltage	$V_{SS} + 2.0$			V
$V_{IL}$	Input low voltage			$V_{SS} + 0.8$	V
$I_{in}$	Input leakage current ( $V_{in} = 0$ to $5.25$ V) Tx CLK, Rx CLK, Rx data, Enable RESET, RS, R/W, CS, DCD, CTS		1.0	2.5	$\mu A$
$I_{IZ}$	$I_{IZ}$ (off-state) input current ( $V_{in} = 0.4$ to $2.4$ V, $V_{CC} = 5.25$ V) D0-D7		2.0	10	$\mu A$
$V_{OH}$	Output high voltage ( $I_{load} = -205 \mu A$ , Enable pulse width < 25 ms) ( $I_{load} = -100 \mu A$ , Enable pulse width < 25 ms) TX data, DTR, TUF D0-D7	$V_{SS} + 2.4$ $V_{SS} + 2.4$			V V
$V_{OL}$	Output low voltage ( $I_{load} = 1.6$ mA, Enable pulse width < 25 $\mu s$ )			$V_{SS} + 0.4$	V
$I_{OZ}$	Output leakage current (off state) ( $V_{OH} = 2.4$ V)		1.0	10	$\mu A$
$P_{INT}$	Internal power dissipation (measured at $T_C = -55^{\circ}C$ )		500	630	mW
$C_{in}$	Input capacitance ( $V_{in} = 0$ , $T_A = 25^{\circ}C$ , $f = 1.0$ MHz) D0-D7 All others			12.5 7.5	pF pF
$C_{out}$	Output capacitance ( $V_{in} = 0$ , $T_A = 25^{\circ}C$ , $f = 1.0$ MHz) Tx data, SMDTR, TUF IRC			10 5.0	pF pF



### 5.3 - Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and  $V_{\text{CC}}$  in the range 4.75 V to 5.25 V  $V_{\text{IL}} = 0.8$  V and  $V_{\text{IH}} = 2.0$  V.

Test conditions are defined in § 5.4.

Table 4 - AC electrical characteristics

$V_{\text{CC}} = 5.0$  V  $\pm 5\%$  ;  $V_{\text{SS}} = 0$  ;  $T_{\text{a}} = T_{\text{L}}$  to  $T_{\text{H}}$  (unless otherwise specified)

Symbol	Characteristic	EF 6852		EF 68A52		Unit
		Min	Max	Min	Max	
PWCL	Serial clock pulse width, low (Figure 3)	700		400		ns
PWCH	Serial clock pulse width, high (Figure 4)	700		400		ns
$f_{\text{C}}$	Serial clock frequency (Rx CLK, Tx CLK)		600		1000	kHz
$t_{\text{RDSU}}$	Receive data setup time (Figure 5)	350		200		ns
$t_{\text{RDH}}$	Receive data hold time (Figure 5)	350		200		ns
$t_{\text{SM}}$	Sync match delay time (Figure 5)		1.0		0.666	$\mu\text{s}$
TDD	Clock-to-data delay for transmitter (Figures 6, 8)		1.0		0.666	$\mu\text{s}$
$t_{\text{TUF}}$	Transmitter underflow (Figure 6)		1.0		0.666	$\mu\text{s}$
$t_{\text{DTR}}$	DTR delay time (Figure 7)		1.0		0.666	$\mu\text{s}$
$t_{\text{IR}}$	Interrupt request release time (Figure 7)		1.6		1.1	$\mu\text{s}$
$t_{\text{RESET}}$	RESET pulse width	1.0		0.666		$\mu\text{s}$
$t_{\text{CTS}}$	CTS setup time (Figure 8)	200		150		ns
$t_{\text{DCD}}$	DCD setup time (Figure 9)	500		350		ns
$t_{\text{r}}, t_{\text{f}}$	Input rise and fall times (except enable)		1.0*		1.0*	$\mu\text{s}$

\* 1.0  $\mu\text{s}$  or 10% of the pulse width, whichever is smaller.

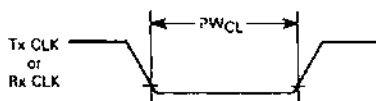


Figure 3: Clock pulse width, low-state.

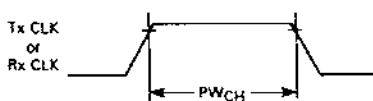


Figure 4: Clock pulse width, high-state.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

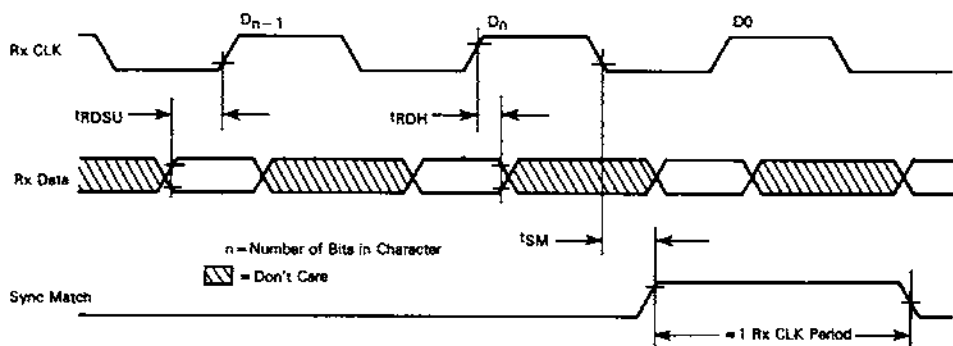


Figure 5: Receive data setup and hold times and sync match delay time.

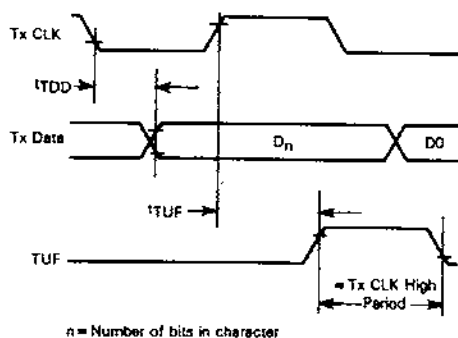


Figure 6: Transmit data output delay and transmitter underflow delay time.

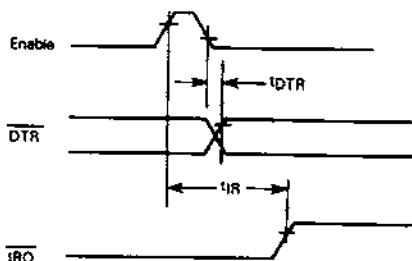


Figure 7: Data terminal ready and interrupt request release times.

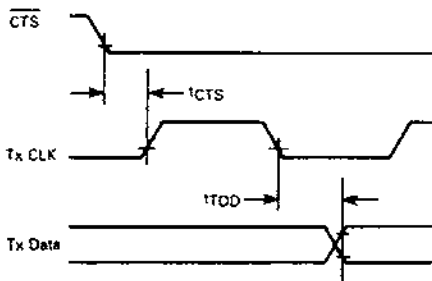
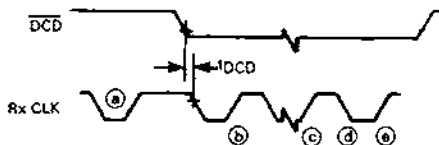


Figure 8: Clear-to-send setup time.



Notes:

- a. Must occur before  $\overline{\text{DCD}}$  goes low.
  - b. First data bit placed in Rx shift register.
  - c. Last data bit of byte placed in Rx shift register.
  - d. Rx data byte transferred from shift register to Rx FIFO.
  - e. Clock edge required for generation of  $\overline{\text{IRQ}}$  by RDA status.
- Note: Refer to Figure 3 for the Rx data setup and hold times.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

Figure 9: Data carrier detect setup time.



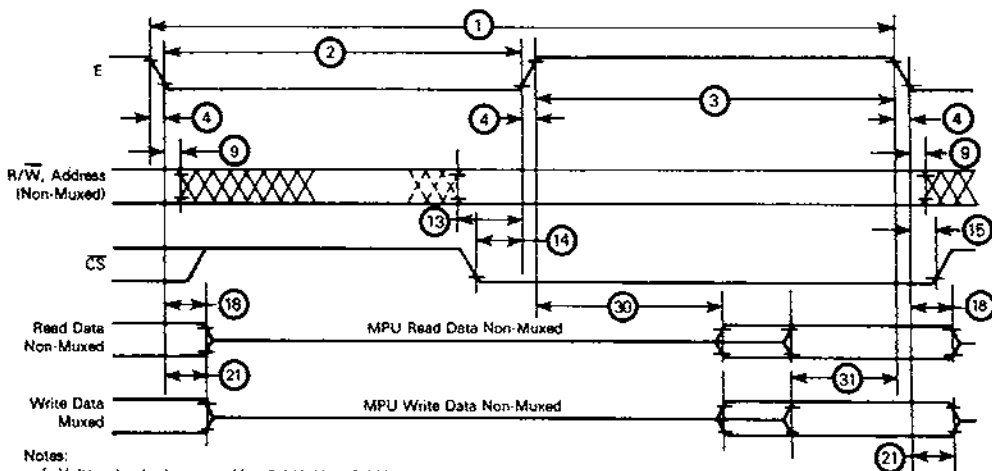
Table 5 - Bus timing characteristics - see Notes 1, 2 and Figure 10

Ident Number	Symbol	Characteristics	EF 6852		EF 68A52		Unit
			Min	Max	Min	Max	
1	$t_{cyc}$	Cycle time	1.0	10	0.67	10	$\mu s$
2	PWEL	Pulse width, E low	430		280		ns
3	PWEH	Pulse width, E high	450		280		ns
4	$t_r, t_f$	Clock rise and fall time		25		25	ns
9	$t_{AH}$	Address hold time	10		10		ns
13	$t_{AS}$	Address setup time before E	80		60		ns
14	$t_{CS}$	Chip select setup time before E	80		60		ns </td
15	$t_{CH}$	Chip select hold time	10		10		ns
18	$t_{DHR}$	Read data hold time	20	50*	20	50*	ns
21	$t_{DHW}$	Write data hold time	10		10		ns
30	$t_{DDR}$	Output data delay time		290		180	ns
31	$t_{DSW}$	Input data setup time	165		80		ns

\* The data bus output buffers are not longer sourcing or sinking current by  $t_{DHR}$  max (high impedance).

Note 1: Voltage levels shown are  $V_L \leq 0.4$  V,  $V_H \geq 2.4$  V, unless otherwise specified.

Note 2: Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.



Notes:

1. Voltage levels shown are  $V_L \leq 0.4$  V,  $V_H \geq 2.4$  V, unless otherwise specified.

2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

Figure 10: Bus timing characteristics (read/write information).

#### 5.4 - Test conditions specific to the device

##### 5.4.1 - Loading network

The figure here below shows the loading network applicable to the timing tables.

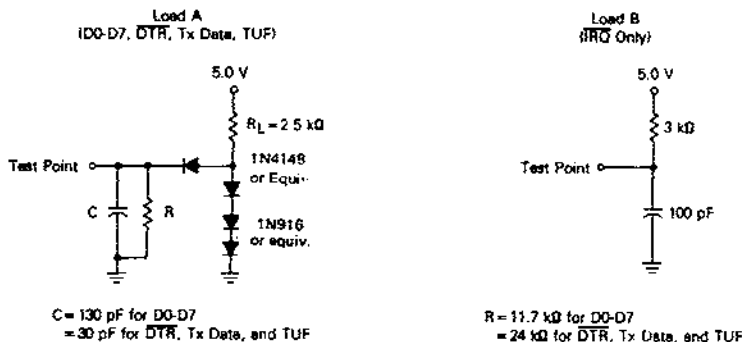


Figure 11 : Bus timing test loads.

## 6 - FUNCTIONAL DESCRIPTION

### 6.1 - Device operation

At the bus interface, the SSDA appears as two addressable memory locations. Internally, there are seven registers: two read-only and five write-only registers. The read-only registers are status and receive data; the write-only registers are control 1, control 2, control 3, sync code and transmit data. The serial interface consists of serial input and output lines with independent clocks, and four peripheral/modem control lines.

Data to be transmitted is transferred directly into the 3-byte transmit data first-in first-out (FIFO) register from the data bus. Availability of the input to the FIFO is indicated by the TDRA bit in the Status register; once data is entered, it moves through the FIFO to the last empty location. Data at the output of the FIFO is automatically transferred from the FIFO to the transmitter shift register as the shift register becomes available to transmit the next character. If data is not available from the FIFO (underflow condition), the transmitter shift register is automatically loaded with either a sync code or an all '1's' character. The transmit section may be programmed to append even, odd, or no parity to the transmitted word. An external control line (clear-to-send) is provided to inhibit the transmitter without clearing the FIFO.

Serial data is accumulated in the receiver based on the synchronization mode selected. In the external sync mode, used for parallel-serial operation, the receiver is synchronized by the DCD (data carrier detect) input (Figure 1) and transfers successive bytes of data to the input of the receiver FIFO. The single-sync-character mode requires that a match occur between the sync code register and one incoming character before data transfer to the FIFO begins. The two-sync-character mode requires that two sync codes be received in sequence to establish synchronization. Subsequent to synchronization in any mode, data is accumulated in the shift register, and parity is optionally checked. An indication of parity error is carried through the receiver FIFO with each character to the last empty location. Availability of a word at the FIFO output is indicated by the RDA status bit in the status register, as is a parity error (PE).

The SSDA and its internal registers are selected by RS, CS, read/write (R/W) and enable control lines. To configure the SSDA, control registers are selected and the appropriate bits set. The status register is addressable for reading status.

Other I/O lines, in addition to clear-to-send (CTS) and data carrier detect (DCD), include SM/DTR (sync match/data terminal ready) and transmitter underflow (TUF). The transmitter and receiver each have individual clock inputs allowing simultaneous operation under separate clock control. Signals to the microprocessor are the data bus and interrupt request (IRQ).

### 6.1.1 - Initialization

During a power-on sequence, the SSDA is reset via the RESET input and internally latched in a reset condition to prevent erroneous output transitions. The receiver shift register is set to all '1's'. The sync code register, control register 2, and control register 3 should be programmed prior to the programmed release of the transmitter and/or receiver reset bits; these bits in control register 1 should be cleared after the RESET line has gone high.

### 6.1.2 - Transmitter operation

Data is transferred to the transmitter section in parallel form by means of the data bus and transmit data FIFO. The transmit data FIFO is a 3-byte register whose status is indicated by the transmitter data register available status bit (TDRA) and its associated interrupt enable bit. Data is transferred through the FIFO on negative edges of enable (E) pulses. Two data transfer modes are provided in the SSDA. The 1-byte transfer mode provides for writing data to the transmitter section (and reading from the receiver section) one byte at a time. The 2-byte transfer mode provides for writing two data characters in succession.

Data will automatically transfer from the last register location in the transmit data FIFO (when it contains data) to the transmitter shift register during the last half of the last bit of the previous character. A character is transferred into the shift register by the transmitter clock. Data is transmitted LSB first, and odd or even parity can be optionally appended. The unused bit positions in short word length characters, from the data bus, are "don't care".

**Note:** the data bus inputs may be reversed for applications requiring the MSB to be transferred first, e.g., IBM format for floppy disks; however, care must be taken to properly program the control registers - Table 6 will have its bit positions reversed.

When the shift register becomes empty, and data is not available for transfer from the transmit data FIFO, an «underflow» occurs, and a character is inserted into the transmitter data stream to maintain character synchronization. The character trans-



mitted on underflow will be either a «mark» (all «1's») or the contents of the sync code register, depending upon the state of the transmit sync code on underflow control bit. The underflow condition is indicated by a pulse (= 1 Tx CLK high period) on the underflow output (when in Tx sync on underflow mode). The underflow output occurs coincident with the transfer of the last half of the last bit preceding the underflow character. The underflow status bit is set until cleared by means of the clear underflow control bit. This output may be used in floppy disk systems to synchronize write operations and for appending CRC's.

Transmission is initiated by clearing the transmitter reset bit in control register 1. When the transmitter reset bit is cleared, the first full positive half-cycle of the transmit clock will initiate the transmit cycle, with the transmission of data or underflow characters beginning on the negative edge of the transmit clock pulse which started the cycle. If the transmit data FIFO was not loaded, an underflow character will be transmitted (see Figure 6).

The clear-to-send (CTS) input provides for automatic control of the transmitter by means of external system hardware: e.g., the modem CTS output provides the control in a data communications system. The CTS input resets and inhibits the transmitter section when high, but does not reset the transmit data FIFO. The TDRA status bit is inhibited by CTS being high in either the one-sync character or two-sync character mode of operation. In the external sync mode, TDRA is unaffected by CTS in order to provide transmit data FIFO status for preloading and operating the transmitter under the control of the CTS input. When the transmitter reset bit (TxRS) is set, the transmit data FIFO is cleared and the TDRA status bit is cleared. After one E clock has occurred, the transmit data FIFO becomes available for new data with TDRA inhibited.

### 6.1.3 Receiver operation

Data and a presynchronized clock are provided to the SSDA receiver section by means of the receive data (Rx data) and receive clock (Rx CLK) inputs. The data is a continuous stream of binary data bits without means for identifying character boundaries within the stream. It is, therefore, necessary to achieve character synchronization for the data at the beginning of the data block. Once synchronization is achieved, it is assumed to be retained for all successive characters within the block.

Data communication systems utilize the detection of sync codes during the initial portion of the preamble to establish character synchronization. This requires the detection of a single code or two successive sync codes. Floppy disk and cartridge tape units require six or eight bits of defined preamble and cassettes require eight bits of preamble to establish the reference for the start of record. All three are functionally equivalent to the detection of sync codes. Systems which do not utilize code detection techniques require custom logic external to the SSDA for character synchronization and use of the parallel-to-serial (external sync) mode.

**Note:** The receiver shift register is set to ones when reset.

### 6.1.4 Synchronization

The SSDA provides three operating modes with respect to character synchronization: one-sync-character mode, two-sync-character mode, and external sync mode. The external sync mode requires synchronization and control of the receiving section through the data carrier detect (DCD) input (see Figure 9). This external synchronization could consist of direct line control from the transmitting end of the serial data link or from external logic designed to detect the start of the message block. The one-sync-character mode searches on a bit-by-bit basis until a match is achieved between the data in the shift register and the sync code register. The match indicates character synchronization is complete and will be retained for the message block. In the two-sync-character mode, the receiver searches for the first sync code match on a bit-by-bit basis and then looks for a second successive sync code character prior to establishing character synchronization. If the second sync code character is not received, the bit-by-bit search for the first sync code is resumed.

Sync codes received prior to the completion of synchronization (one or two character) are not transferred to the receive data FIFO. Redundant sync codes during the preamble or sync codes which occur as «fill characters» can automatically be stripped from the data, when the strip sync control bit is set, to minimize system loading. The character synchronization will be retained until cleared by means of the clear sync bit, which also inhibits synchronization search when set.

### 6.1.5 Receiving data

Once synchronization has been achieved, subsequent characters are automatically transferred into the receive data FIFO and clocked through the FIFO to the last empty location by E pulses (MPU system  $\phi$  2). The receiver data available status bit (RDA) indicates when data is available to be read from the last FIFO location (= 0) when in the 1-byte transfer mode. The 2-byte transfer mode causes the RDA status bit to indicate is available when the last two FIFO register locations are full. Data being available in the receive data FIFO causes an interrupt request if the receiver interrupt enable (RIE) bit is set. The MPU will then read the SSDA status register which will indicate that data is available for the MPU read from the receive data FIFO register. The IRQ and RDA status bits are reset by a read from the FIFO. If more than one character has been received and is resident in the receive data FIFO, subsequent E clocks will cause the FIFO to update and the RDA and IRQ status bits will again be set. The read data operation for the 2-byte transfer mode requires an intervening E clock between reads to allow the FIFO data to shift. Optional parity is automatically checked as data is received, and the parity status condition is maintained with each character until the data is read from the receive data FIFO. Parity errors will cause an interrupt request if the error interrupt enable (EIE) has been set. The parity bit is not transferred to the data bus but must be checked in the status register.

**Note:** In the 2-byte transfer mode, parity should be checked prior to reading the second byte, since a FIFO read clears the error bit.

Other status bits which pertain to the receiver section are receiver overrun and data carrier detect (DCD). The overrun status bit is automatically set when a transfer of a character to the receive data FIFO occurs and the first register of the receive data FIFO is full. Overrun causes an interrupt if error interrupt enable (EIE) has been set. The transfer of the overrunning character into the FIFO causes the previous character in the FIFO input register location to be lost. The overrun status bit is cleared by reading the status register (when the overrun condition is present), followed by a receive data FIFO register read. Overrun cannot occur and be cleared without providing an opportunity to detect its occurrence via the status register.

A positive transition on the DCD input causes an interrupt if the EIC control bit has been set. The interrupt caused by DCD is cleared by reading the status register when the DCD status bit is high, followed by a receive data FIFO read. The DCD status bit will subsequently follow the state of the DCD input when it goes low.



## 6.2 - INPUT/OUTPUT FUNCTIONS

### 6.2.1 - SSSA interface signals for MPU

The SSSA interfaces to the EF 6800 MPU with an 8-bit bi-directional data bus, a chip-select line, a register-select line, an interrupt-request line, read/write line, an enable line, and a reset line. These signals, in conjunction with the EF 6800 VMA output, permit the MPU to have complete control over the SSSA.

#### SSSA bi-directional data (D0-D7)

The bi-directional data lines (D0-D7) allow for data transfer between the SSSA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an SSSA read operation.

#### SSSA enable (E)

The enable signal, E, is a high impedance TTL-compatible input that enables the bus input/output data buffers, clocks data to and from the SSSA, and moves data through the FIFO registers.

#### Read/write (R/W)

The read/write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the SSSA's input/output data bus interface. When read/write is high (MPU read cycle), SSSA output drivers are turned on if the chip is selected and a selected register is read. When it is low, the SSSA output drivers are turned off and the MPU writes into a selected register. The read/write signal is also used to select read-only or write-only registers within the SSSA.

#### Chip select ( $\overline{CS}$ )

This high-impedance TTL-compatible input line is used to address the SSSA. The SSSA is selected when  $\overline{CS}$  is low. VMA should be used in generating the  $\overline{CS}$  input to insure that false selects will not occur. Transfers of data to and from the SSSA are then performed under the control of the enable signal, read/write, and register select.

#### Register select (RS)

The register select line is a high-impedance input that is TTL compatible. A high level is used to select control registers C2 and C3, the sync code register, and the transmit/receive data registers. A low level selects the control 1 and status registers (see table 6).

#### Interrupt request (IRQ)

Interrupt request is a TTL compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The interrupt request remains low until cleared by the MPU.

#### RESET input

The RESET input provides a means of resetting the SSSA from an external source. In the low state, the  $\overline{RESET}$  input causes the following:

1. Receiver reset (Tx Rs) and transmitter reset (Rx Rs) bits are set causing both the receiver and transmitter sections to be held in a reset conditions.
2. Peripheral control bits PC1 and PC2 are reset to zero, causing the SMDTR output to be high.
3. The error interrupt enable (EIE) bit is reset.
4. An internal synchronization mode is selected.
5. The transmitter data register available (TDRA) status bit is cleared and inhibited.
6. The receiver shift register is set to 1's.

When  $\overline{RESET}$  returns high (the inactive state), the transmitter and receiver sections will remain in the reset state until the receiver reset and transmitter reset bits are cleared via the data bus under software control. The control register bits affected by  $\overline{RESET}$  (Rx Rs, Tx Rs, PC1, PC2, EIE, and E/I sync) cannot be changed when  $\overline{RESET}$  is low.

### 6.2.2 - Clock inputs

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data.

#### Transmit clock (Tx CLK)

The transmit clock input is used for the clocking of transmitted data. The transmitter shifts data on the negative transition of the clock.

#### Receive clock (Rx CLK)

The receive clock input is used for clocking in received data. The clock and data must be synchronized externally. The receiver samples the data on the positive transition of the clock.

### 6.2.3 - Serial input/output lines

#### Receive data (Rx data)

The receive data line is a high-impedance TTL-compatible input through which data is received in a serial format.

#### Transmit data (Tx data)

The transmit data output line transfers serial data to a modem or other peripheral.

### 6.2.4 - Peripheral/modem control

The SSSA includes several functions that permit limited control of a peripheral or modem. The functions included are clear-to-send, sync match/data terminal ready, data carrier detect, and transmitter underflow.



**Clear-to-send (CTS)**

The  $\overline{\text{CTS}}$  input provides a real-time inhibit to the transmitter section (the Tx data FIFO is not disturbed). A positive  $\overline{\text{CTS}}$  transition resets the Tx shift register and inhibits the TDRA status bit and its associated interrupt in both the one-sync-character and two-sync-character modes of operation. TDRA is not affected by the CTS input in the external sync mode. The positive transition of CTS is stored within the SSSA to insure that its occurrence will be acknowledged by the system. The stored CTS information and its associated IRQ (if enabled) are cleared by writing a «1» in the clear CTS bit in control register 3 or in the transmitter reset bit. The CTS status bit subsequently follows the CTS input when it goes low. The CTS input provides character timing for transmitter data when in the external sync mode. Transmission is initiated on the negative transition of the first full positive clock pulse of the transmitter clock (Tx CLK) after the release of CTS (see Figure 6).

**Data carrier detect (DCD)**

The DCD input provides a real-time inhibit to the receiver section (the Rx FIFO is not disturbed). A positive DCD transition resets and inhibits the receiver section except for the receive FIFO and the RDRA status bit and its associated IRQ. The positive transition of DCD is stored within the SSSA to insure that its occurrence will be acknowledged by the system. The stored DCD information and its associated IRQ (if enabled) are cleared by reading the status register and then the receiver FIFO, or by writing a «1» into the receiver reset bit. The DCD status bit subsequently follows the DCD input when it goes low. The DCD input provides character synchronization timing for the receiver during the external sync mode of operation. The receiver will be initialized and data will be sampled on the positive transition of the first full receive clock cycle after release of DCD (see Figure 9).

**Sync match/data terminal ready (SM/DTR)**

The SM/DTR output provides four functions (see Table 6) depending on the state of the PC1 and PC2 control bits. When the sync match bit is selected (PC = «1», PC2 = «0»), the output provides a one-bit-wide pulse when a sync code is detected. This pulse occurs for each sync code match even if the receiver has already attained synchronization. The SM output is inhibited when PC2 = «1». The DTR mode (PC1 = «0») provides an output level corresponding to the complement of PC2 (DTR = «0» when PC2 = «1»). (See Table 6).

Table 6 - SSSA programming model

Register	Control Inputs		Address Control		Register Content							
	RS	R/W	AC2	AC1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status (S)	0	1	X	X	Interrupt Request (IRQ)	Receiver Parity Error (PE)	Receiver Overrun (Rx Ovrn)	Transmitter Underflow (TUF)	Clear-to-Send (CTS)	Data Carrier Detect (DCD)	Transmitter Data Register Available (TDRA)	Receiver Data Available (RDA)
Control 1 (C1)	0	0	X	X	Address Control 2 (AC2)	Address Control 1 (AC1)	Receiver Interrupt Enable (RIE)	Transmitter Interrupt Enable (TIE)	Clear Sync	Strip Sync Characters (Strip Sync)	Transmitter Reset (Tx Rs)	Receiver Reset (Rx Rs)
Receive Data FIFO	1	1	X	X	D7	D6	D5	D4	D3	D2	D1	D0
Control 2 (C2)	1	0	0	0	Error Interrupt Enable (EIE)	Transmit Sync Code on Underflow (Tx Sync)	Word Length Select 3 (WS3)	Word Length Select 2 (WS2)	Word Length Select 1 (WS1)	1-Byte/2-Byte Transfer (1-Byte/2-Byte)	Peripheral Control 2 (PC2)	Peripheral Control 1 (PC1)
Control 3 (C3)	1	0	0	1	Not Used	Not Used	Not Used	Not Used	Clear Transmitter Underflow Status (CTUF)	Clear CTS Status (Clear CTS)	One-Sync-Character/Two-Sync-Character Mode Control (1 Sync/2 Sync)	External/Internal Sync Mode Control (E/I Sync)
Sync Code	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Transmit Data FIFO	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

X - Don't care

**STATUS REGISTER**

IRQ	Bit 7	The IRQ flag is cleared when the source of the $\overline{\text{IRQ}}$ is cleared. The source is determined by the enables in the control registers : TIE, RIE, EIE.
PE	Bits 6-0	Indicate the SSSA status at a point in time, and can be reset as follows :
Rx Ovrn	Bit 6	Read Rx data FIFO, or a «1» into Rx Rs (C1 bit 0).
TUF	Bit 5	Read status and then Rx data FIFO, or a «1» into Rx Rs (C1 bit 0).
CTS	Bit 4	A «1» into CTUF (C3 bit 3) or into Tx Rs (C1 bit 1).
DCD	Bit 4	A «1» into clear CTS (C3 bit 2) or a «1» into Tx Rs (C1 bit 1).
TDRA	Bit 2	Read status and then Rx data FIFO or a «1» into Rx Rs (C1 bit 0)
RDA	Bit 1	Write into Tx data FIFO
	Bit 0	Read Rx data FIFO.

## CONTROL REGISTER 1

AC2, AC1	Bits 7, 6	Used to access other registers, as shown above.
RIE	Bit 5	When «1», enables interrupt on RDA (S bit 0).
TIE	Bit 4	When «1», enables interrupt on TDRA (S bit 1).
Clear sync	Bit 3	When «1», clears receiver character synchronization.
Strip sync	Bit 2	When «1», strips all sync codes from the received data stream.
Tx Rs	Bit 1	When «1», resets and inhibits the transmitter section.
Rx Rs	Bit 0	When «1», resets and inhibits the receiver section.

## CONTROL REGISTER 3


CTUF	Bit 3	When «1», clears TUF (S bit 4), and $\overline{IRQ}$ if enabled.
Clear CTS	Bit 2	When «1», clears CTS (S bit 3), and $\overline{IRQ}$ if enabled.
1 sync/2 sync	Bit 1	When «1», selects the one-sync-character mode; when «0», selects the two-sync-character mode.
$\overline{E}$ sync	Bit 0	When «1», selects the external sync mode; when «0», selects the internal sync mode.

## CONTROL REGISTER 2

EIE	Bit 7	When «1», enables the PE, Rx Ovrn, TUF, $\overline{CTS}$ , and $\overline{DCD}$ interrupt flags (S bits 6 through 2).
Tx Sync	Bit 6	When «1», allows sync code contents to be transferred on underflow, and enables the TUF status bit and output. When «0», an all mark character is transmitted on underflow.
WS3, 2, 1	Bit 5-3	Word length select.

Bit 5 WS3	Bit 4 WS2	Bit 3 WS1	Word Length
0	0	0	6 Bits + Even Parity
0	0	1	6 Bits + Odd Parity
0	1	0	7 Bits
0	1	1	8 Bits
1	0	0	7 Bits + Even Parity
1	0	1	7 Bits + Odd Parity
1	1	0	8 Bits + Even Parity
1	1	1	8 Bits + Odd Parity

1-byte/2-byte	Bit 2	When «1», enables the TDRA and RDA bits to indicate when a 1-byte transfer can occur; when «0», the TDRA and RDA bits indicate when a 2-byte transfer can occur.
PC2, PC1	Bit 1-0	SM/DTR output control.

Bit 1 PC2	Bit 0 PC1	SM/DTR Output at Pin 5
0	0	1
0	1	Pulse  1 Bit Wide, on SM
1	0	0
1	1	SM inhibited, 0

**Note:** When the SSDA is used in applications requiring the MSB of data to be received and transmitted first, the data bus inputs to the SSDA may be reversed (D0 to D7, etc.). Caution must be used when this is done since the bit positions in this table will be reversed, and the parity should not be selected.

## Transmitter underflow (TUF)

The underflow output indicates the occurrence of a transfer of a «fill character» to the transmitter. It is asserted when the last location (= 3) in the transmit data FIFO is empty. The underflow output pulse is approximately one T<sub>CLK</sub> high period wide and occurs during the last half of the last bit of the character preceding the «underflow» (see Figure 6). The underflow output pulse does not occur when the Tx sync bit is in the reset state.

## 6.3 - SSDA REGISTERS

Seven registers in the SSDA can be accessed by means of the data bus. The registers are defined as read-only or write-only according to the direction of information flow. The register select input (RS) selects two registers in each state, one being read-only and the other write-only. The read/write input (R/W) defines which of the two selected registers will actually be accessed. Four registers (two read-only and two write-only) can be accessed via the bus at any particular time. These registers and the required addressing are defined in Table 6.

## 6.3.1 - Control register 1 (C1)

Control register 1 is an 8-bit write-only register that can be directly addressed from the data bus. Control register 1 is accessed when RS = «0» and R/W = «0».

## Receiver reset (Rx Rs), C1 bit 0

The receiver reset control bit provides both a reset and inhibit function to the receiver section. When Rx Rs is set, it clears the receiver control logic, sync logic, error logic, Rx data FIFO control, parity error status bit, and  $\overline{DCD}$  interrupt. The receiver shift register is set to ones. The Rx Rs bit must be cleared after the occurrence of a low level on  $\overline{RESET}$  in order to enable the receiver section of the SSDA.



**Transmitter reset (Tx Rs), C1 bit 1**

The transmitter reset control bit provides both reset and inhibit to the transmitter section. When Tx Rs is set, it clears the transmitter control section, transmitter shift register, Tx data FIFO control (the Tx data FIFO can be reloaded after one E clock pulse) the transmitter underflow status bit, and the CTS interrupt, and inhibits the TDRA status bit (in the one-sync-character and two-sync-character modes). The Tx Rs bit must be cleared after the occurrence of a low level on RESET in order to enable the transmitter section of the SSDA. If the Tx FIFO is not preloaded, it must be loaded immediately after the Tx Rs release to prevent a transmitter underflow condition.

**Strip synchronization (strip sync), C1 bit 2**

If the strip sync bit is set, the SSDA will automatically strip all received characters which match the contents of the sync code register. The characters used for synchronization (one or two characters of sync) are always stripped from the received data stream.

**Clear synchronization (clear sync), C1 bit 3**

The clear sync control bit provides the capability of dropping receiver character synchronization and inhibiting resynchronization. The clear sync bit is set to clear and inhibit receiver synchronization in all modes and is reset to zero to enable resynchronization.

**Transmitter Interrupt enable (TIE), C1 bit 4**

TIE enables both the interrupt request output ( $\overline{IRQ}$ ) and interrupt request status bit to indicate a transmitter service request. When TIE is set and the TDRA status bit is high, the  $\overline{IRQ}$  output will go low (the active state) and the  $\overline{IRQ}$  status bit will go high.

**Receiver interrupt enable (RIE), C1 bit 5**

RIE enables both the interrupt request output ( $\overline{IRQ}$ ) and the interrupt request status bit to indicate a receiver service request. When RIE is set and the RDA status bit is high, the  $\overline{IRQ}$  output will go low (the active state) and the  $\overline{IRQ}$  status bit will go high.

**Address control 1 (AC1) and address control 2 (AC2), C1 bits 6 and 7**

AC1 and AC2 select one of the write-only registers - control 2, control 3, sync code, or Tx data FIFO - as shown in Table 6, when RS = «1» and RW = «0».

**6.3.2 - Control register 2 (C2)**

Control register 2 is an 8-bit write-only register which can be programmed from the data bus when the address control bits of control register 1 (AC1 and AC2) are reset, RS = «1» and RW = «0».

**Peripheral control (PC1) and peripheral control 2 (PC2), C2 bits 0 and 1**

Two control bits, PC1 and PC2, determine the operating characteristics of the sync match/DTR output. PC1, when high, selects the sync match mode. PC2 provides the inhibit/enable control for the SM/DTR output in the sync match mode. A one-bit-wide pulse is generated at the output when PC2 is «0», and a match occurs between the contents of the sync code register and the incoming data even if sync is inhibited (clear sync bit = «1»). The sync match pulse is referenced to the negative edge of R x-CLK pulse causing the match (see Figure 3).

The data terminal ready (DTR) mode is selected when PC1 is low. When PC2 = «1» the SM/DTR output = «0» and vice versa. The operation of PC2 and PC1 is summarized in Table 6.

**1-byte/2-byte transfer (1-byte/2-byte), C2, bit 2**

When 1-byte/2-byte is set, the TDRA and RDA status bits will indicate the availability of their respective data FIFO registers for a single-byte data transfer. Alternately, if 1-byte/2-byte is reset, the TDRA and RDA status bits indicate when two bytes of data can be moved without a second status read. An intervening enable pulse must occur between data transfers.

**Word length selects (WS1, WS2, WS3), C2 bits, 3, 4, 5**

Word length select bits WS1, WS2, and WS3 select word lengths of 7, 8 or 9 bits including parity as shown in Table 6.

**Transmit sync code on underflow (Tx sync), C2 bit 6**

When Tx sync is set, the transmitter will automatically send a sync character when data is not available for transmission. If Tx sync is reset, the transmitter will transmit a mark character (including the parity bit position) on underflow. When the underflow is detected, a pulse approximately one Tx CLK high period wide will occur on the underflow output if the Tx sync bit is set. Internal parity generation is inhibited during underflow except for sync code fill character transmission in 8-bit plus parity word lengths.

**Error interrupt enable (EIE), C2 bit 7**

When EIE is set, the  $\overline{IRQ}$  status bit will go high and the  $\overline{IRQ}$  output will go low if:

1. A receiver overrun occurs. The interrupt is cleared by reading the status register and reading the Rx data FIFO. The DCD input has gone to a «1». The interrupt is cleared by reading the status register and reading the Rx data FIFO. Internal parity error exists for the character in the last location (= 3) of the Rx data FIFO. The interrupt is cleared by reading the Rx data FIFO.
2. The DCD input has gone to a «1». The interrupt is cleared by writing a «1» in the clear CTS bit, C3 bit 2, or by a Tx reset.
3. The transmitter underflow occurs (in the Tx sync on underflow mode). The interrupt is cleared by writing a «1» into the clear underflow status bit, C3 bit 1.

When EIE is a «0», the CTS and DCD inputs and the  $\overline{IRQ}$  output are disabled for the above error conditions. A low level on the RESET input reset EIE to «0».

### 6.3.3 - Control register 3 (C3)

Control register 3 is a 4-bit write-only register which can be programmed from the data bus when  $\overline{RS} = \text{«1»}$  and  $\overline{RW} = \text{«0»}$  and address control bit AC1 = «1» and AC2 = «0».

#### External/Internal sync mode control (E/I sync), C3 bit 0

When the E/I sync mode bit is high, the SSDA is in the external sync mode and the receiver synchronization logic is disabled. Synchronization can be achieved by means to the DCD input or by starting Rx CLK at the midpoint of data bit 0 of a character with DCD low. Both the transmitter and receiver sections operate as parallel - serial converters in the external sync mode. The clear sync bit in control register 1 acts as a receiver sync inhibit when high to provide a bus controllable inhibit. The sync code register can serve as a transmitter fill character register and a receiver match register in this mode. A «low» on the RESET input resets the E/I sync mode bit placing the SSDA in the internal sync mode.

#### One-sync-character/two-sync-character mode control (1-sync/2-sync), C3 bit 1

When the 1-sync/2-sync bit is set, the SSDA will synchronize on a single match between the received data and the contents of the sync code register. When the 1-sync/2-sync bit is reset, two successive sync characters must be received prior to receiver synchronization. If the second sync character is not detected, the bit-by-bit search resumes from the first bit in the second character. See the description of the sync code register for more details.

#### Clear CTS status (clear CTS), C3 bit 2

When a «1» is written into the clear CTS bit, the stored status and interrupt are cleared. Subsequently, the CTS status bit reflects the state of the CTS input. The clear CTS control bit does not affect the CTS input nor its inhibit of the transmitter section. The clear CTS command bit is self-clearing, and writing a «0» into this bit is a nonfunctional operation.

#### Clear transmit underflow status (CTUF), C3 bit 3

When a «1» is written into the CTUF status bit, the CTUF bit and its associated interrupt are reset. The CTUF command bit is self-clearing and writing a «0» into this is a nonfunctional operation.

### 6.3.4 - Sync code register

The sync code register is an 8-bit register for storing the programmable sync code required for received data character synchronization in the one-sync-character and two-sync-character modes. The sync code register also provides for stripping the sync-fill characters from the received data (a programmable option) as well as automatic insertion of fill characters in the transmitted data stream. The sync code register is not utilized for receiver character synchronization in the external sync mode; however, it provides storage of receiver match and transmit fill characters.

The sync code register can be loaded when AC2 and AC1 are a «1» and «0», respectively, and  $\overline{RW} = \text{«0»}$  and  $\overline{RS} = \text{«1»}$ .

The sync code register may be changed after the detection of a match with the received data (the first sync code having been detected) to synchronize with a double-word sync pattern. (This sync code change must occur prior to the completion of the second character). The sync match (SM) output can be used to interrupt the MPU system to indicate that the first eight bits have matched. The service routine would then change the sync match register to the second half of the pattern. Alternately, the one-sync-character mode can be used for sync codes for 16 or more bits by using software to check the second and subsequent bytes after reading them from the FIFO.

The detection of the sync code can be programmed to appear on the sync match/DTR output by writing a «1» in PC1 (C2 bit 0) and a «0» in PC2 (C2 bit 1). The sync match output will go high for one bit time beginning at the character interface between the sync code and the next character (see Figure 5).

### 6.3.5 - Parity for sync character

#### Transmitter

Transmitter does not generate parity for the sync character except 9-bit mode.

- 9-bit (8-bit + parity)... 8-bit sync character + parity
- 8-bit (7-bit + parity)... 8-bit sync character (no parity)
- 7-bit (6-bit + parity)... 7-bit sync character (no parity)

#### Receiver

##### At synchronization

Receiver automatically stripes the sync character(s) (two sync characters if «2 sync» mode is selected) which is used to establish synchronization. Parity is not checked for these sync characters.

##### After synchronization is established

When «strip sync» bit is selected, the sync characters (fill characters) are stripped any parity is not checked for the stripped sync (fill) characters. When «strip sync» bit is not selected (low), the sync character is assumed to be normal data and it is transferred into FIFO after parity checking. (When non-parity format is selected, parity is not checked).

Strip Sync (C1, Bit 2)	WS0-WS2 (Data Format) (C2, Bits 3-5)	
1	X	No transfer of sync code No parity Check of sync code
0	With Parity	*Transfer data and sync codes Parity check
0	Without Parity	*Transfer data and sync codes No parity check

\*Subsequent to synchronization.



It is necessary to consider parity in the selected sync character in the following cases. Data format is (6 + parity), (7 + parity), strip sync is not selected (low), and when sync code is used as a fill character after synchronization.

The transmitter sends a sync character without parity, but the receiver checks the parity as if it is normal data. Therefore, the sync character should be chosen to match the parity check selected for the receiver in this special case. See the following section for unused bit assignment in short-word length.

### 6.3.6 - Receive data first : in first-out register (Rx data FIFO)

The receive data FIFO register consists of three 8-bit registers which are used for buffer storage of received data. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer from register to register occurs on E pulses. The RDA status bit will be high when data is available in the last location of the Rx data FIFO.

In an overrun condition, the overrunning character will be transferred into the full first stage of the FIFO register and will cause the loss of that data character. Successive overruns continue to overwrite the first register of the FIFO. This destruction of data is indicated by means of the overrun status bit. The overrun bit will be set when the overrun occurs and remains set until the status register is read, followed by a read of the Rx data FIFO.

Unused data bits for short word lengths (including the parity bit) will appear as '0's on the data bus when the Rx data FIFO is read.

### 6.3.7 - Transmit data first-in first-out register (Tx data FIFO)

The transmit data FIFO register consists of three 8-bit registers which are used for buffer storage of data to be transmitted. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer is clocked by E pulses.

The TDRA status bit will be high if the Tx data FIFO is available for data.

Unused data bits for short word lengths will be handled as 'don't cares'. The parity bit is not transferred over the data bus since the SSDA generates parity at transmission.

When an underflow occurs, the underflow character will be either the contents of the sync code register or an all '1's' character. The underflow will be stored in the status register until cleared and will appear on the underflow output as a pulse approximately one Tx CLK high period wide.

### 6.3.8 - Status register (S)

The status register is an 8-bit read-only register which provides the real-time status of the SSDA and the associated serial data channel. Reading the status register is a non-destructive process. The method of clearing status bits depends upon the function each bit represents and is discussed for each bit in the register.

#### Receiver data available (RDA), B bit 0

The receiver data available status bit indicates when receiver data can be read from the Rx data FIFO. The receiver data being present in the last register (= 3) of the FIFO causes RDA to be high for the 1-byte transfer mode. The RDA bit being high indicates that the last two registers (= 2 and = 3) are full when in the 2-byte transfer mode. The second character can be read without a second status read (to determine that the character is available). An E pulse must occur between reads of the Rx data FIFO to allow the FIFO to shift. Status must be read on a word-by-word basis if receiver data error checking is important. The RDA status bit is reset automatically when data is not available.

#### Transmitter data register available (TDRA), S bit 1

The TDRA status bit indicates that data can be loaded into the Tx data FIFO register. The first register (= 1) of the Tx data FIFO being empty will be indicated by a high level in the TDRA status bit in the 1-byte transfer mode. The first two registers (= 1 and = 2) must be empty for TDRA to be high when in the 2-byte transfer mode. The Tx data FIFO can be loaded with two bytes without an intervening status read; however, one E pulse must occur between loads. TDRA is inhibited by the Tx reset or RESET. When Tx reset is set, the Tx data FIFO is cleared and then released on the next E clock pulse. The Tx data FIFO can then be loaded with up to three characters of data, even though TDRA is inhibited. This feature allows preloading data prior to the release of Tx reset. A high level on the CTS input inhibits the TDRA status bit in either sync mode of operation (one-sync-character or two-sync-character). CTS does not affect TDRA in the external sync mode. This enables the SSDA to operate under the control of the CTS input with TDRA indicating the status of the Tx Data FIFO. The CTS input does not clear the Tx data FIFO in any operating mode.

#### Data carrier detection (DCD), S bit 2

A positive transition on the DCD input is stored in the SSDA until cleared by reading both status and Rx data FIFO. A '1' written into Rx Rs also clears the stored DCD status. The DCD status bit, when set, indicates that the DCD input has gone high. The reading of status followed by reading of the receive data FIFO allows bit 2 of subsequent status reads to indicate the state of the DCD input until the next positive transition.

#### Clear-to-send (CTS), S bit 3

A positive transition on the CTS input is stored in the SSDA until cleared by writing a '1' into the clear CTS control bit or the Tx Rs bit. The CTS status bit, when set, indicates that the CTS input has gone high. The clear CTS command (a '1' into C3 bit 2) allows bit 3 of subsequent status reads to indicate the state of the CTS input until the next positive transition.

#### Transmitter underflow (TUF), S bit 4

When data is not available for the transmitter, an underflow occurs and is so indicated in the status register (in the Tx sync on underflow mode). The underflow status bit is cleared by writing a '1' into the clear underflow (CTUF) control bit or the Tx Rs bit. TUF indicates that a sync character will be transmitted as the next character. A TUF is indicated on the output only when the contents of the sync code register is to be transferred (transmit sync code on underflow = '1').



**Receiver overrun (Rx Ovrn), S bit 5**

Overrun indicates data has been received when the Rx data FIFO is full, resulting in data loss. The Rx Ovrn status bit is set when overrun occurs. The Rx Ovrn status bit is cleared by reading status followed by reading the Rx data FIFO or by setting the Rx Rs control bit.

**Receiver parity error (PE), S bit 6**

The parity error status bit indicates that parity for the character in the last register of the Rx data FIFO did not agree with selected parity. The parity error is cleared when the character to which it pertains is read from the Rx data FIFO or when Rx Rs occurs. The DCD input does not clear the parity error or Rx data FIFO status bits.

**Interrupt request ( $\overline{IRQ}$ ), S bit 7**

The interrupt request status bit indicates when the  $\overline{IRQ}$  output is in the active state ( $\overline{IRQ}$  output = «0»). The  $\overline{IRQ}$  status bit is subject to the same interrupt enables (RIE, TIE, and EIE) as the  $\overline{IRQ}$  output. The  $\overline{IRQ}$  status bit simplifies status inquiries for polling systems by providing single bit indication of service requests.

**7 - PREPARATION FOR DELIVERY****7.1 - Packaging**

Microcircuit are prepared for delivery in accordance with MIL-M-37510 or CECC 900.

**7.2 - Certificate of compliance**

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 56000 and guaranteeing the parameters are tested at extreme temperatures for the entire temperature range.

**8 - HANDLING**

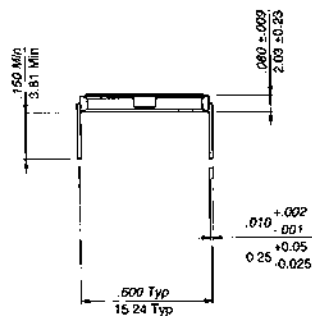
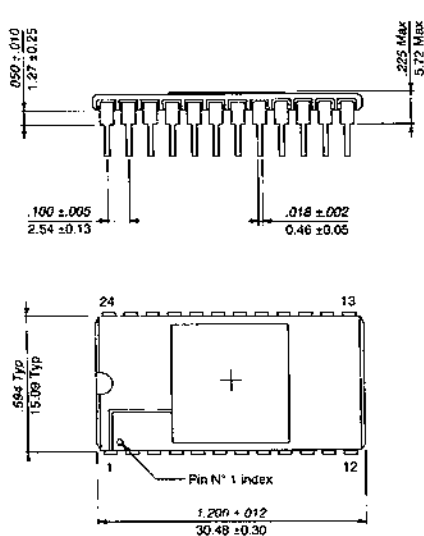
MOS device must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- a) Device should be handled on benches with conductive end grounded mats.
- b) Ground test equipment, tools and operator.
- c) Do not handle devices by the leads.
- d) Store devices in conductive bags or carriers.
- e) Avoid use of plastic mats or cork in MOS areas.
- f) Maintain relative humidity above 30 %, if practical.

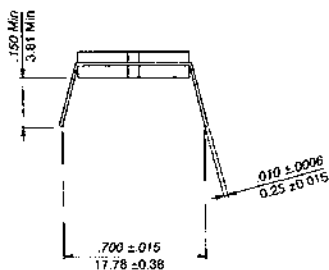
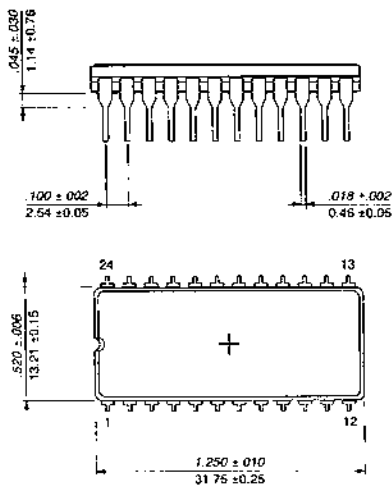


## 9 - PACKAGE MECHANICAL DATA

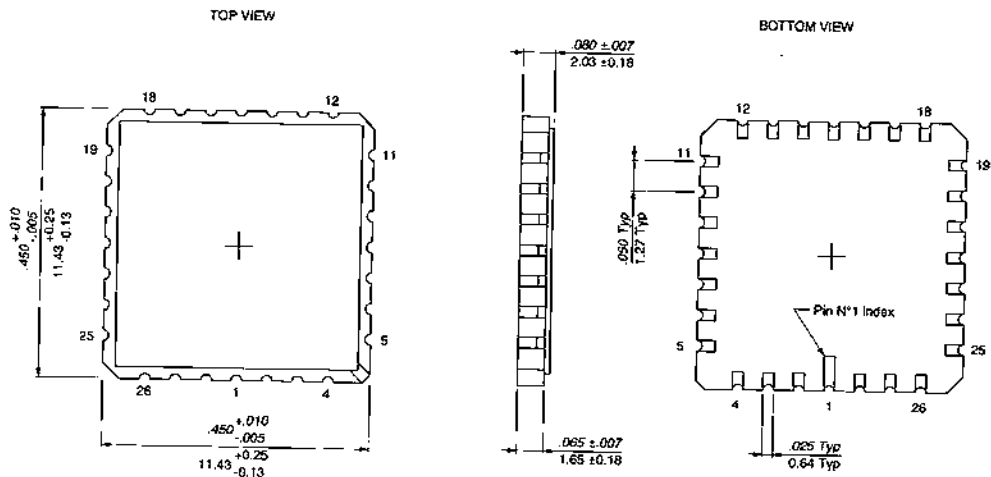
## 9.1 - 24 pins - DIL Ceramic Side Brazed



## 9.2 - 24 pins - DIL Cerdip

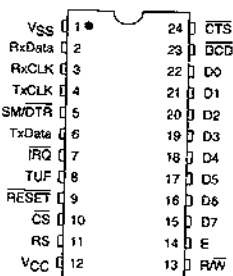


9.3 - 28 pins - LCCC Leadless Ceramic Chip Carrier

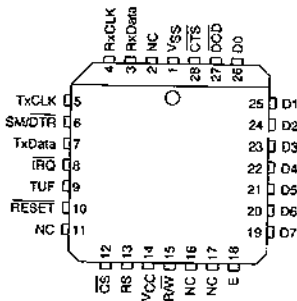


10 - TERMINAL CONNECTIONS

10.1 - 24 pins - DIL pin assignment



10.2 - 28 pins - LCCC Leadless Ceramic Chip Carrier



## 11 - ORDERING INFORMATION

## 11.1 - HI-REL product

Commercial TMS Part-Number (see Note)	Norms	Package	Temperature range T <sub>c</sub> (°C)	Frequency (MHz)	Drawing number
EF6852JMG/B	NFC 96863 class G	DIL Cerdip	-55 / +125	1	Data sheet
EF6852CMG/B*	NFC 96863 class G	DIL Side Brazed	-55 / +125	1	Data sheet
EF6852EMG/B	NFC 96863 class G	LCCC	-55 / +125	1	Data sheet
EF68A52JMG/B	NFC 96863 class G	DIL Cerdip	-55 / +125	1.5	Data sheet
EF68A52CMG/B*	NFC 96863 class G	DIL Side Brazed	-55 / +125	1.5	Data sheet
EF68A52EMG/B	NFC 96863 class G	LCCC	-55 / +125	1.5	Data sheet
EF6852JMB/B	MIL-STD-883 class B	DIL Cerdip	-55 / +125	1	Data sheet
EF6852CMB/B*	MIL-STD-883 class B	DIL Side Brazed	-55 / +125	1	Data sheet
EF6852EMB/B	MIL-STD-883 class B	LCCC	-55 / +125	1	Data sheet
EF68A52JMB/B	MIL-STD-883 class B	DIL Cerdip	-55 / +125	1.5	Data sheet
EF68A52CMB/B*	MIL-STD-883 class B	DIL Side Brazed	-55 / +125	1.5	Data sheet
EF68A52EMB/B	MIL-STD-883 class B	LCCC	-55 / +125	1.5	Data sheet

\* DIL Cerdip is the preferred package.

Note : THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.

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## 11.2 - Standard product

Commercial TMS Part-Number (see Note)	Norms	Package	Temperature range T <sub>c</sub> (°C)	Frequency (MHz)	Drawing number
EF6852CV*	TMS standard	DIL Side Brazed	-40 / +85	1	Data sheet
EF6852JV	TMS standard	DIL Cerdip	-40 / +85	1	Data sheet
EF68A52CV*	TMS standard	DIL Side Brazed	-40 / +85	1.5	Data sheet
EF68A52JV	TMS standard	DIL Cerdip	-40 / +85	1.5	Data sheet
EF6852JM	TMS standard	DIL Cerdip	-55 / +125	1	Data sheet
EF6852CM*	TMS standard	DIL Side Brazed	-55 / +125	1	Data sheet
EF6852EM	TMS standard	LCCC	-55 / +125	1	Data sheet
EF68A52JM	TMS standard	DIL Cerdip	-55 / +125	1.5	Data sheet
EF68A52CM*	TMS standard	DIL Side Brazed	-55 / +125	1.5	Data sheet
EF68A52EM	TMS standard	LCCC	-55 / +125	1.5	Data sheet
EF6852C*	TMS standard	DIL Side Brazed	0 / +70	1	Data sheet
EF6852J	TMS standard	DIL Cerdip	0 / +70	1	Data sheet
EF68A52J	TMS standard	DIL Cerdip	0 / +70	1.5	Data sheet
EF68B52J	TMS standard	DIL Cerdip	0 / +70	2	Data sheet

\* Cerdip package is preferred.

Note : THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.

EF6852 C M B/B

Type \_\_\_\_\_

## Packages:

C = Ceramic DIL (side brazed)  
 E = Ceramic LCCC  
 E1 = LCC+HOT Solder DIP  
 J = Tin dipped Cerdip DIL

## Screening:

\_\_\_ = Standard  
 G/B = NFC 96883 Cl.G  
 B/B = MIL STD 883 Cl.B Rev B

## Temperature /Tcase:

M = -55°C/ +125°C  
 V = -40°C/ +85°C  
 \_ = 0/ +70°C