HIGH-VOLTAGE MONOLITHIC IC

ECN2102/2112

ECN2102 / 2112 is a single chip row driver IC for electroluminescent (EL) display panel.

Functions

- Low-voltage serial to high-voltage parallel converter
- 34 outputs of totem pole type

Features

- Output terminal voltage up to 250V
- Source / Sink current 500mA

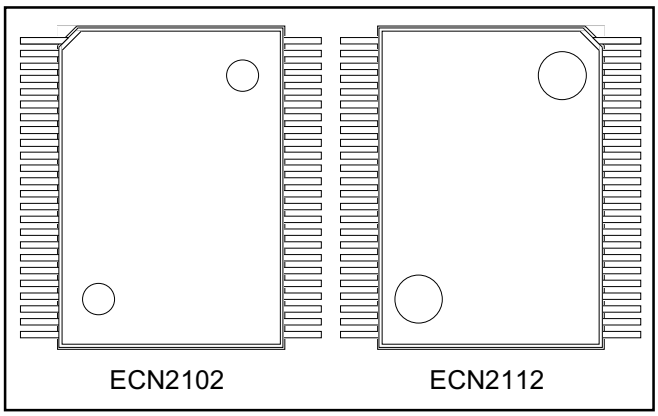
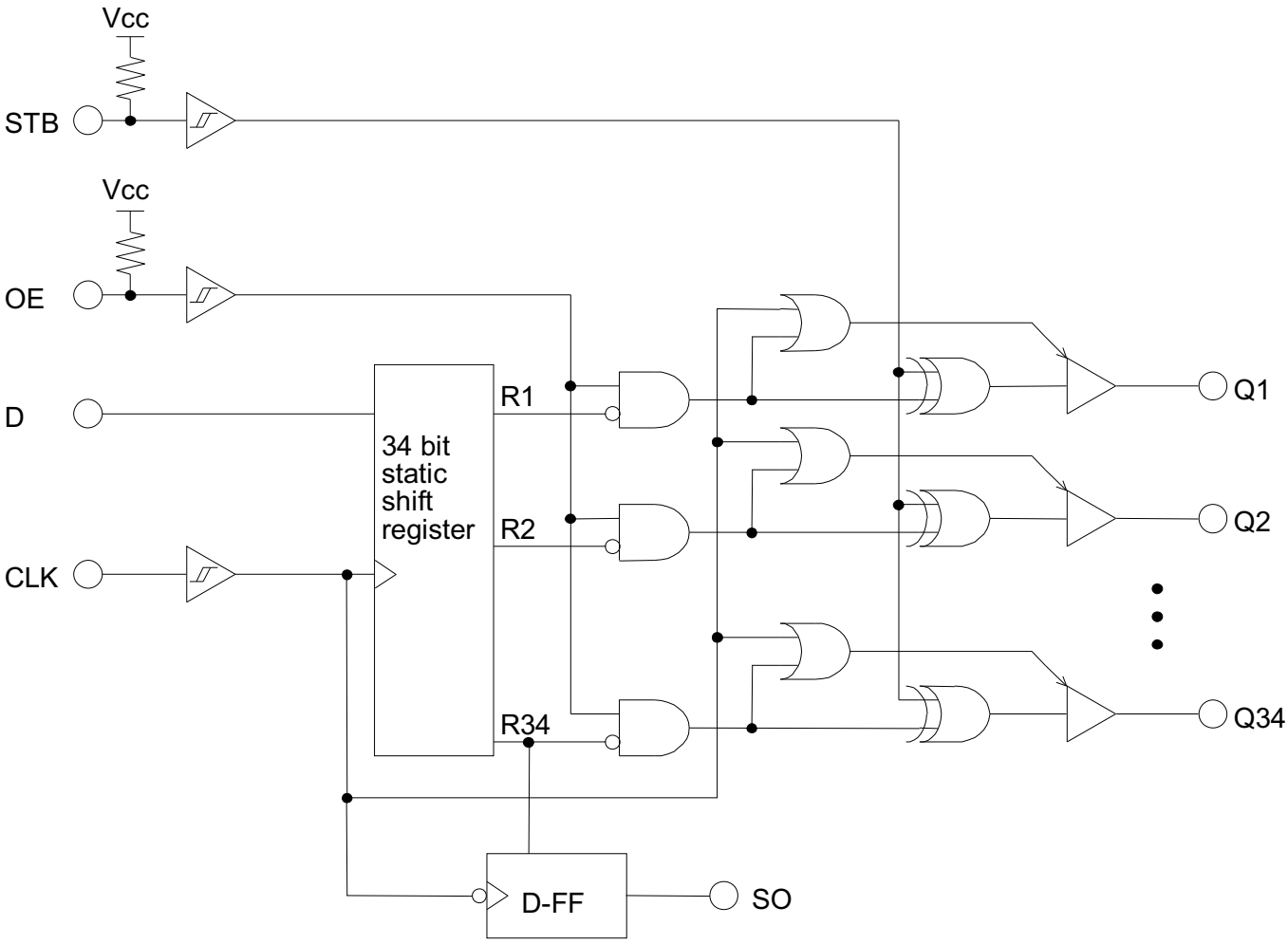


Fig. 1. OUTLINE OF FP-48 PACKAGE



Function Block Diagram (Positive Logic)

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1. GENERAL

(1) TYPE ECN2102/ECN2112

(2) APPLICATION Row line driver for Electroluminecent (EL) display panel

(3) STRUCTURE Monolithic IC, processed Dielectric Isolation.

(4) PACKAGE FP-48 (Fig.1)

2. MAXIMUM ALLOWABLE RATING (Ta=25°C)

No	ITEMS	SYMBOLS	RATINGS	UNITS	CONDITIONS
1	Supply Voltage (logic)	Vcc	-0.5 ~ +7.0	V	to GND terminal
2	Input Voltage (logic)	Vin	-0.5 ~ Vcc+0.5	V	to GND terminal
3	Vs - GND Voltage	VSG	Vcc	V	to GND terminal
4	Output Terminal Voltage	VQ	±250	V	Between Vs,Vcc,GND, Input and Q output
5	Allowable Power Dissipation	PT	800	mW	
6	Operating Temperature	TOP	-40 ~ +85	°C	
7	Storage Temperature	Tstg	-55 ~ +150	°C	

3. RECOMMENDED OPERATING CONDITIONS

No	ITEMS	SYMBOLS	Min.	Typ.	Max.	UNITS	CONDITIONS
1	Supply Voltage (logic)	Vcc	5.0	5.5	6.0	V	
2	Clock Frequency	fCLK	–	–	250	kHz	Vcc= 5.5V
3	Clock Pulse Width	twCLK	80	–	–	ns	Vin= 0V/5.5V
4	Data Setup Time	tsu	80	–	–	ns	
5	Data Hold Time	th	80	–	–	ns	
6	Output Terminal Voltage	VQ	–	±230	–	V	Vcc= 5.5V
7	Peak Output Source Current	HIOH	–	–	-500	mA	Note 1
8	Peak Output Sink Current	HIOL	–	–	+500	mA	Note 1

Note1 : Conduction period ≤ 5 μs per 1 IC

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4. ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta= 25°C, Vcc= 5.5V, HVCC=230V)

No	ITEMS	SYMBOLS	Min.	Typ.	Max.	UNITS	C O N D I T I O N S	
1	Output Voltage (logic)	V_{OL}	–	–	0.1	V	I_{OL}= 20μA	
		V_{OH}	5.4	–	–	V	I_{OH}=-20μA	
2	Output Current (logic)	I_{OL}	1.0	–	–	mA	V_{OL}= 0.8V	
		I_{OH}	-1.0	–	–	mA	V_{OLH} 4.7V	
3	Input Voltage (logic)	V_{IL}	–	–	1.0	V	D input	
		V_{IH}	3.5	–	–	V		
		V_{THL}	–	–	0.4	V	CLK,STB input	
		V_{TLH}	4.5	–	–	V		
4	Input Current (logic)	I_{IH}	–	–	10	μA	Vin=5.5V all input/1 input	
		I_{IL}	–	–	-10	μA	Vin=0V D,CLK/1 input	
			–	–	-100	μA	Vin=0V STB/1 input	
5	Dissipation Current(logic)	Istb	–	–	10	μA	No signal all input 5.5V, all output Off	
			–	–	25	mA	No signal, 1ch source output On	
			–	–	5	mA	No signal, 1ch sink output On	
6	Output Voltage	H_{VOL}	–	–	3.0	V	H_{IOL}=1mA	Q out-GND
			–	–	6.0	V	H_{IOL}=200mA	Q out-GND
		H_{VOH}	–	–	4.0	V	H_{IOH}=-1mA	Vs-Q out
			–	–	8.0	V	H_{IOH}=-200mA	Vs-Q out
7	Output SCR dv/dt capability	dv/dt1	200	–	–	V/μs	Vs~Q out,+dv/dt apply.Fig.6	
		dv/dt2	200	–	–	V/μs	Q out~GND,-dv/dt apply.Fig.7	
8	Output SCR Off Period	toff	–	–	6.0	μs	Source side	Fig.8
			–	–	7.0	μs	Sink side	

5. SWITCHING CHARACTERISTICS (Unless otherwise specified, Ta= 25°C, Vcc= 5.5V, Fig.5)

No	ITEMS	SYMBOLS	Min.	Typ.	Max.	UNITS	C O N D I T I O N S
1	Output Delay Time (logic)	t_{PLH}	–	–	300	ns	CL=15pF
		t_{PHL}	–	–	300	ns	
2	Output Delay Time	t_{QLH}	–	–	3	μs	RLQ=1kΩ
		t_{QHL}	–	–	3	μs	CLQ=2000pF

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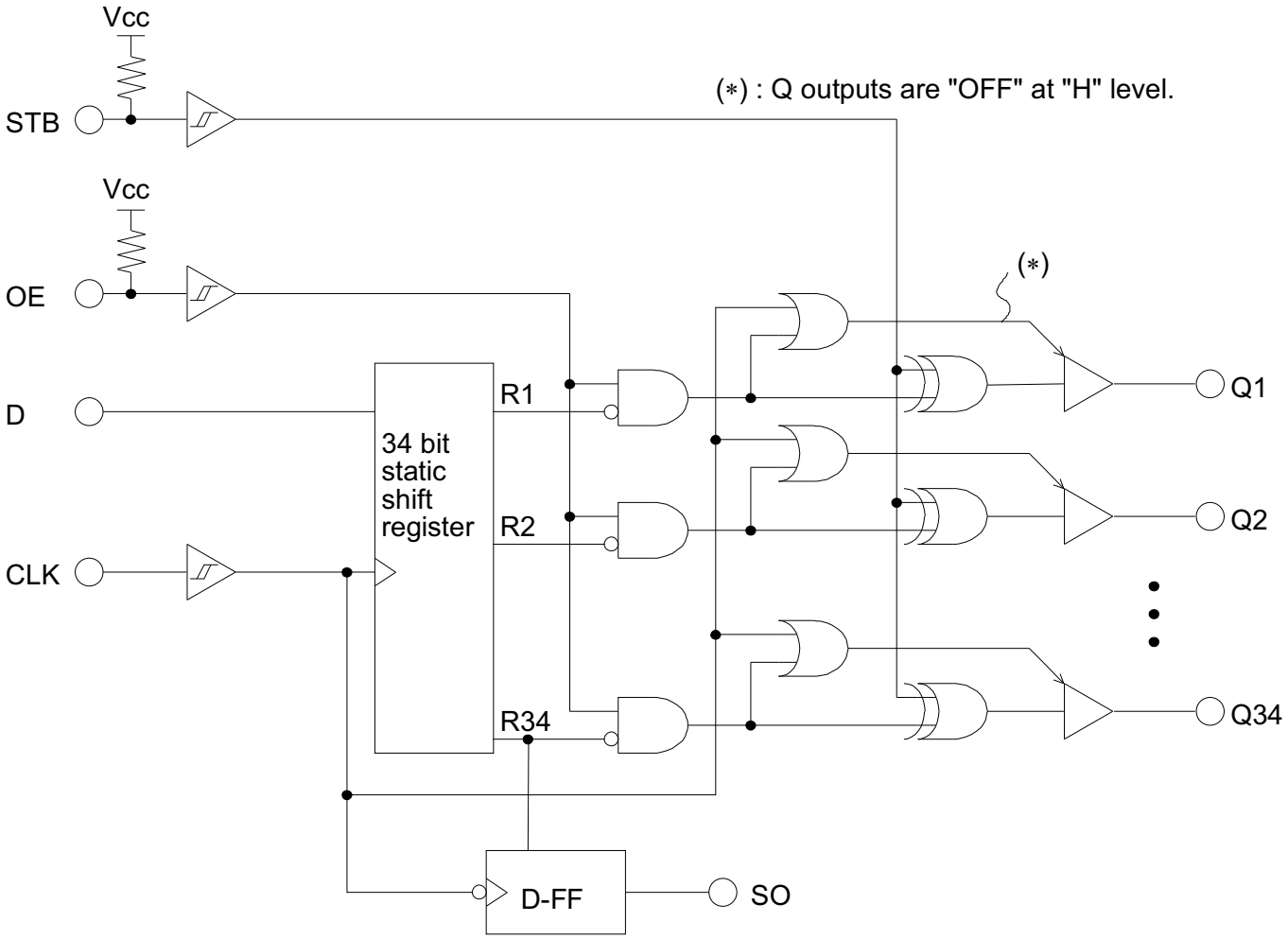

Fig. 2. Function Block Diagram (Positive Logic)

6. FUNCTION TABLE

	CONTROL INPUT				SHIFT REGISTER	OUTPUT	
	CLK	D	OE(*4)	STB	Rn	SO(*1)	Q
SHIFT	↑	∗	H	∗	shift	R34	
OPERATION	no↑	∗	H	∗	keep		
OUTPUT OPERATION	L	∗	H	H	H		H (*2)
					L		OFF
				L	H		L (*3)
					L		OFF
	H	∗	H	∗	∗		ALL OFF

(*1) 34th data is pushed out as output at the state of down edge↓ of clock signal.

(*2) When shift register is "H", source SCR of Q output is driven to ON.

(*3) When shift register is "H", sink SCR of Q output is driven to ON.

(*4) OE must be kept "H".

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7. INPUT / OUTPUT CIRCUIT

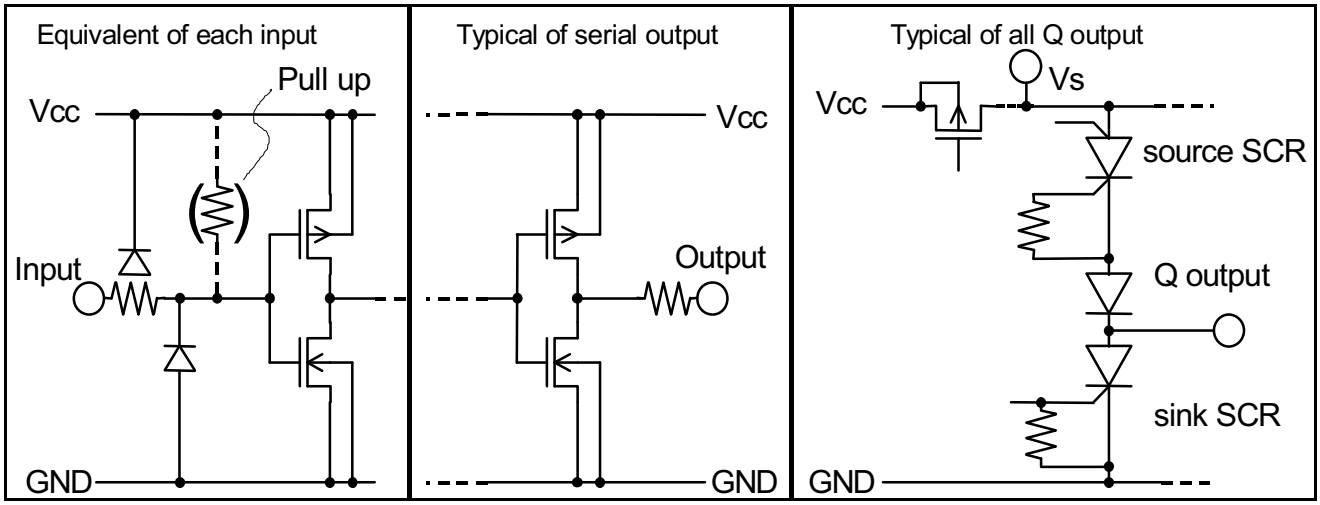

Fig. 3. Input / Output Circuit

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8. EXAMPLE OF OPERATING TIMING CHART

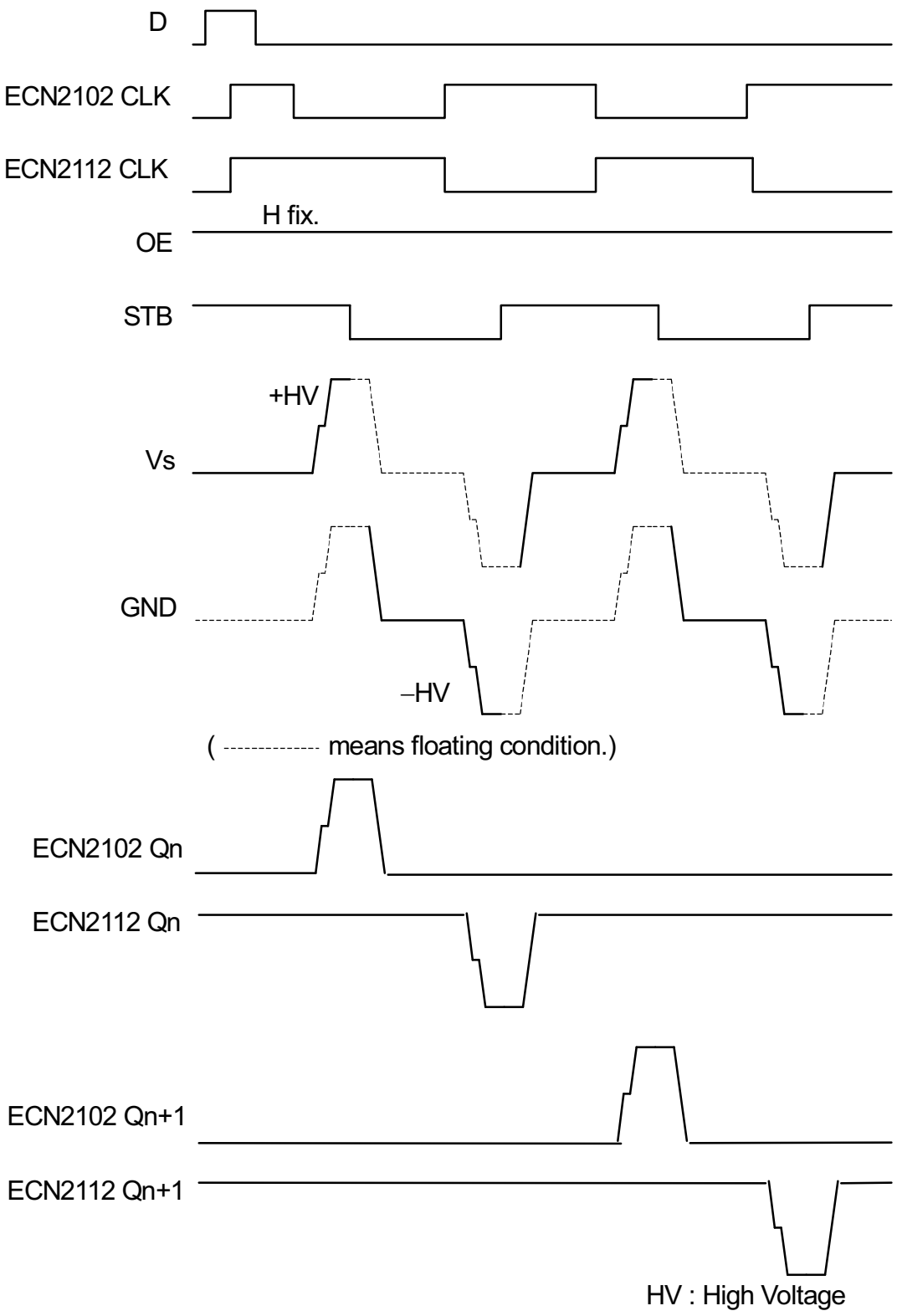

Fig. 4. Example of Operating Timing Chart

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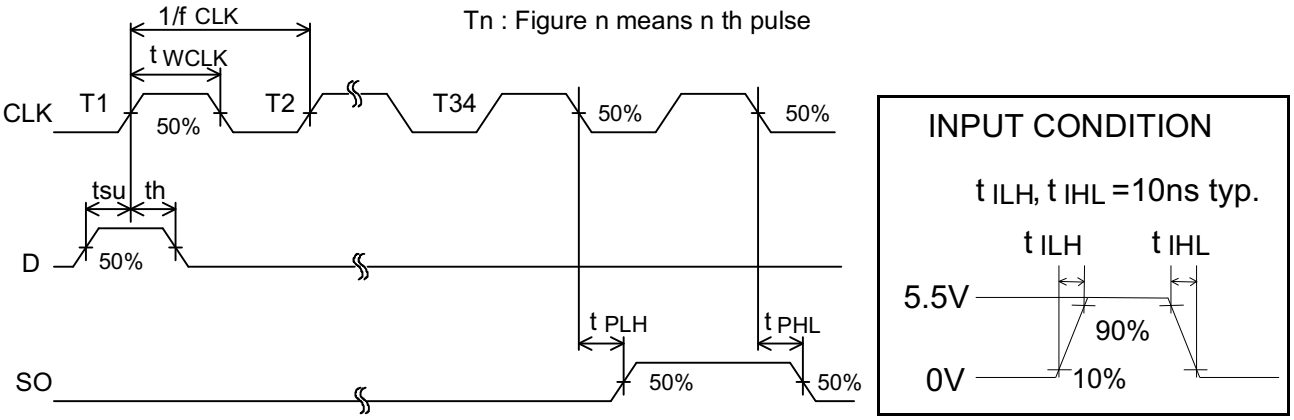
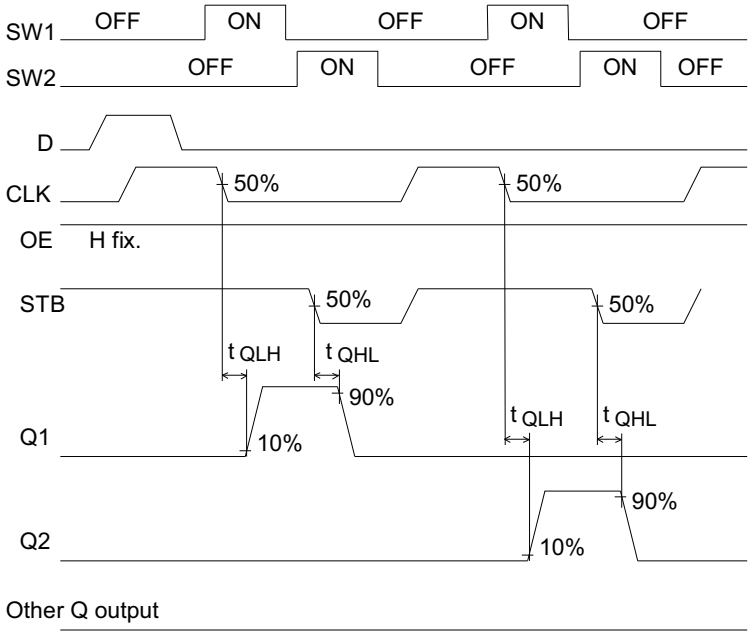
9. MEASUREMENT AND MEASUREMENT CIRCUIT



(a) Shift function (SW1→OFF, SW2,3→ON)



(b) Output Function (SW3→OFF)

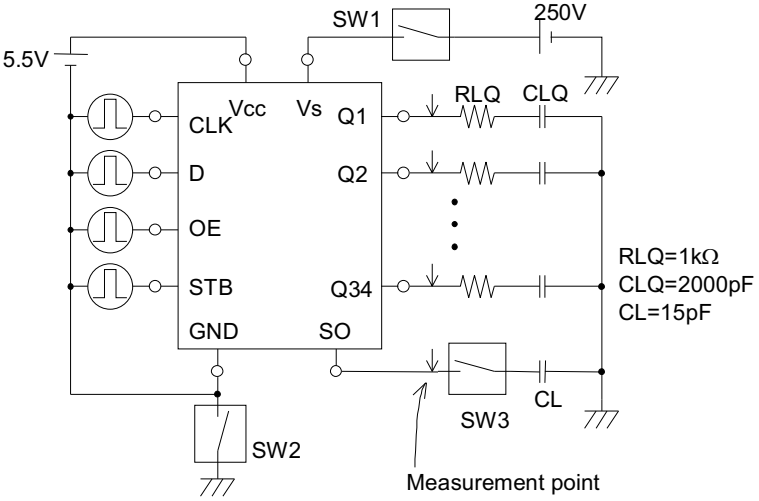


Fig. 5. Switching Characteristics Measurement Circuit

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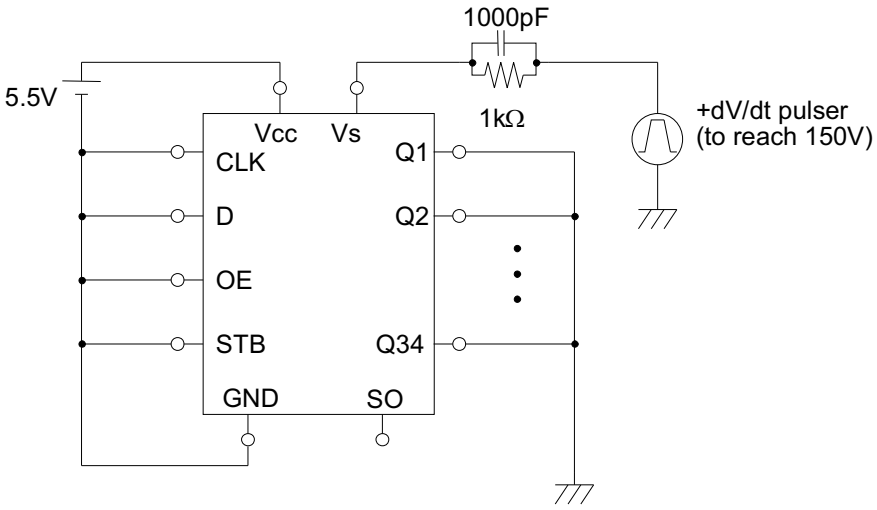

Fig. 6. Output SCR dV/dt capability (dV/dt1) Measurement Circuit

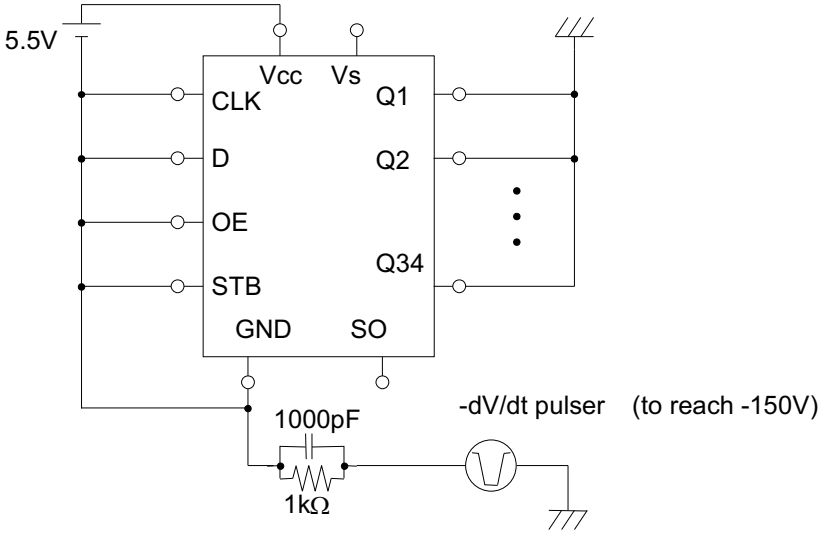

Fig. 7. Output SCR dV/dt capability (dV/dt2) Measurement Circuit

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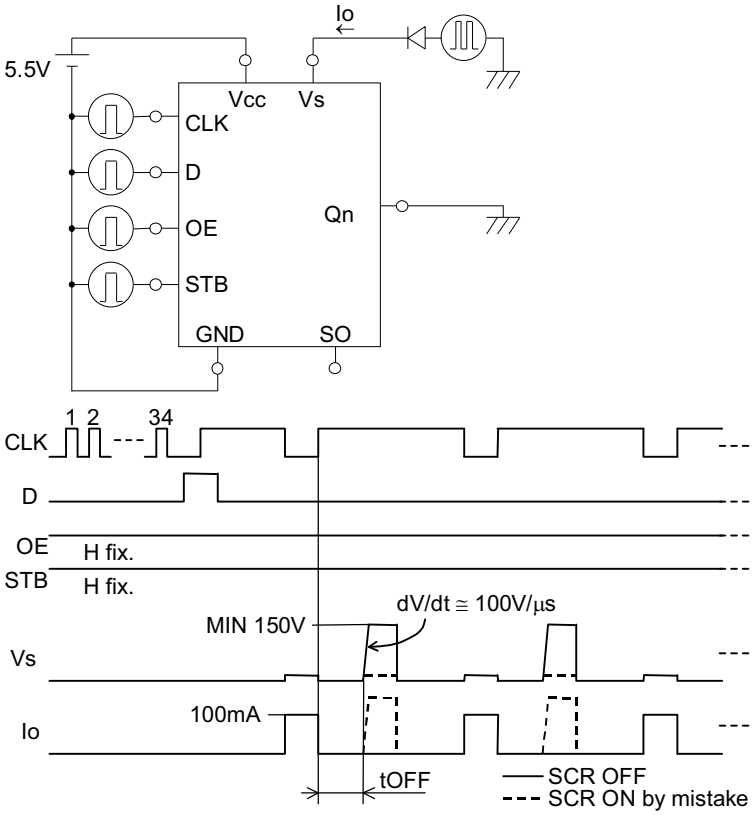
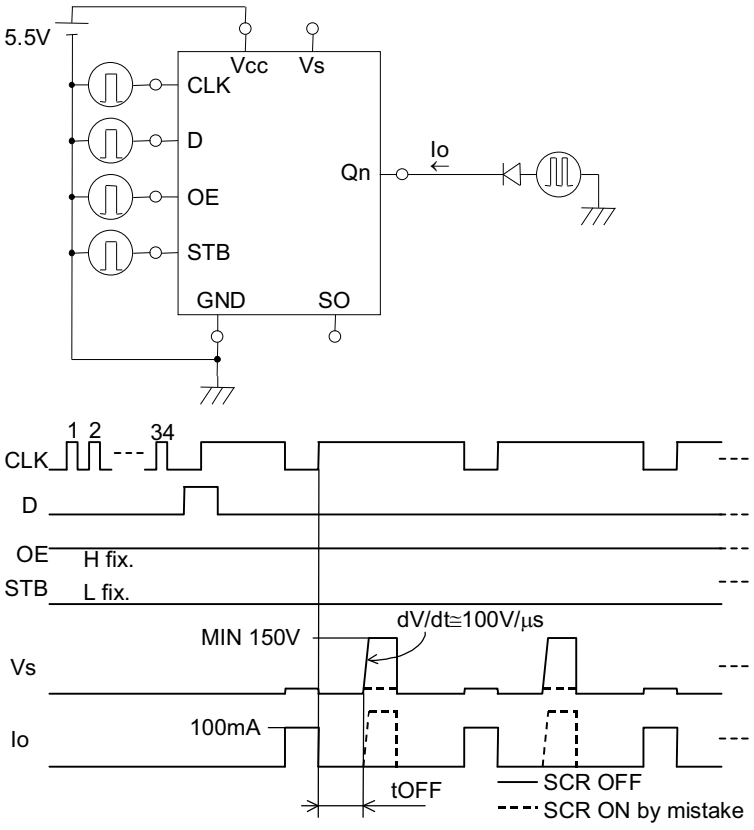


(a) Source SCR



(b) Sink SCR

Fig. 8. Output SCR tOFF Measurement

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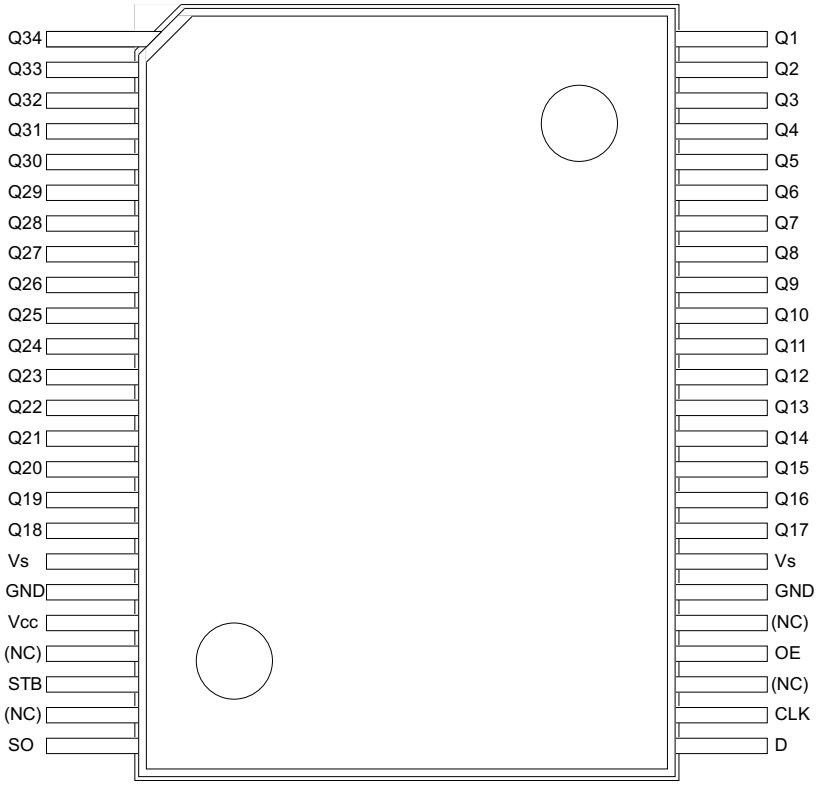
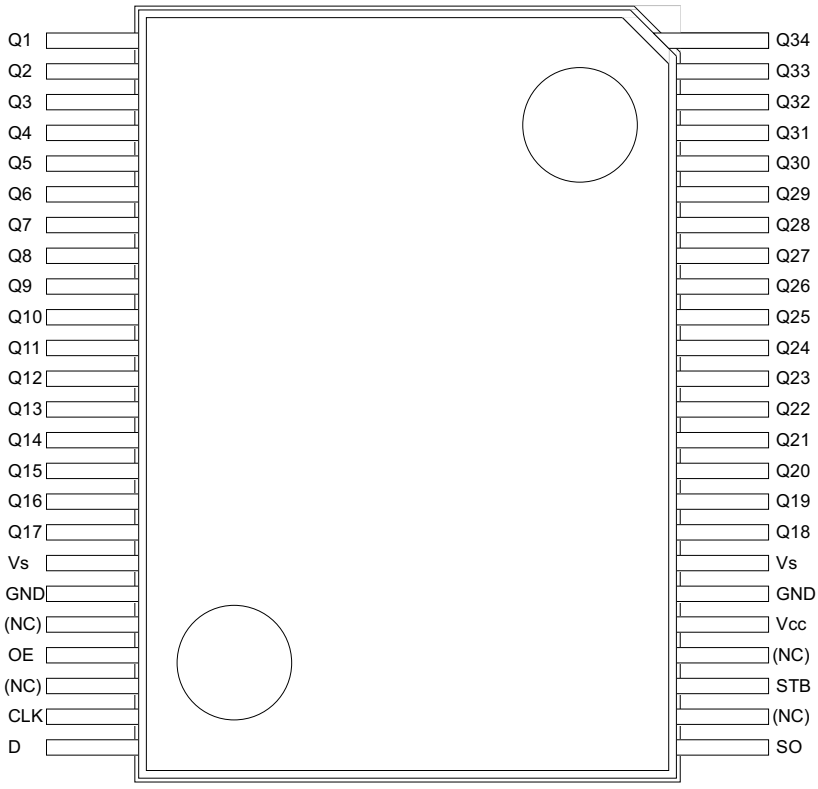
10. PIN LOCATION



(a) ECN2102



(b) ECN2112

Fig. 9. Pin Location (Top view)

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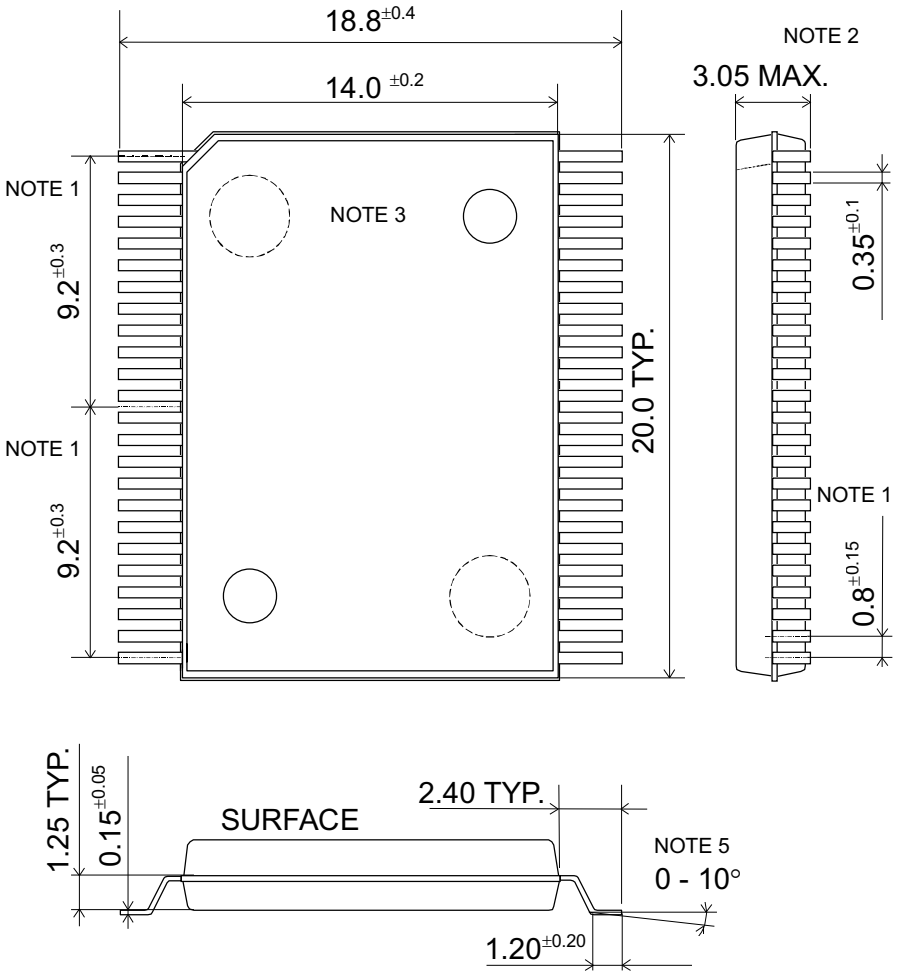
11. PACKAGE OUTLINE (Unit : mm)

(1) ECN2102



Notes.

1. THIS DIMENSION IS MEASURED AT ROOT OF LEAD. SPACING AT TIP OF LEAD IS MIN 0.2.
2. THIS DIMENSION INCLUDES A WARPAGE OF PACKAGE.
3. MARKING IS ON THE SURFACE OF PACKAGE, INCLUDING HITACHI MARK, TYPE NAME, LOT NUMBER, AND JAPAN MARK.
4. LEADS ARE SOLDER PLATED.
5. THIS IS THE BENDING ANGLE WITH HORIZONTAL PLANE.

Fig. 10. Package outline (ECN2102)

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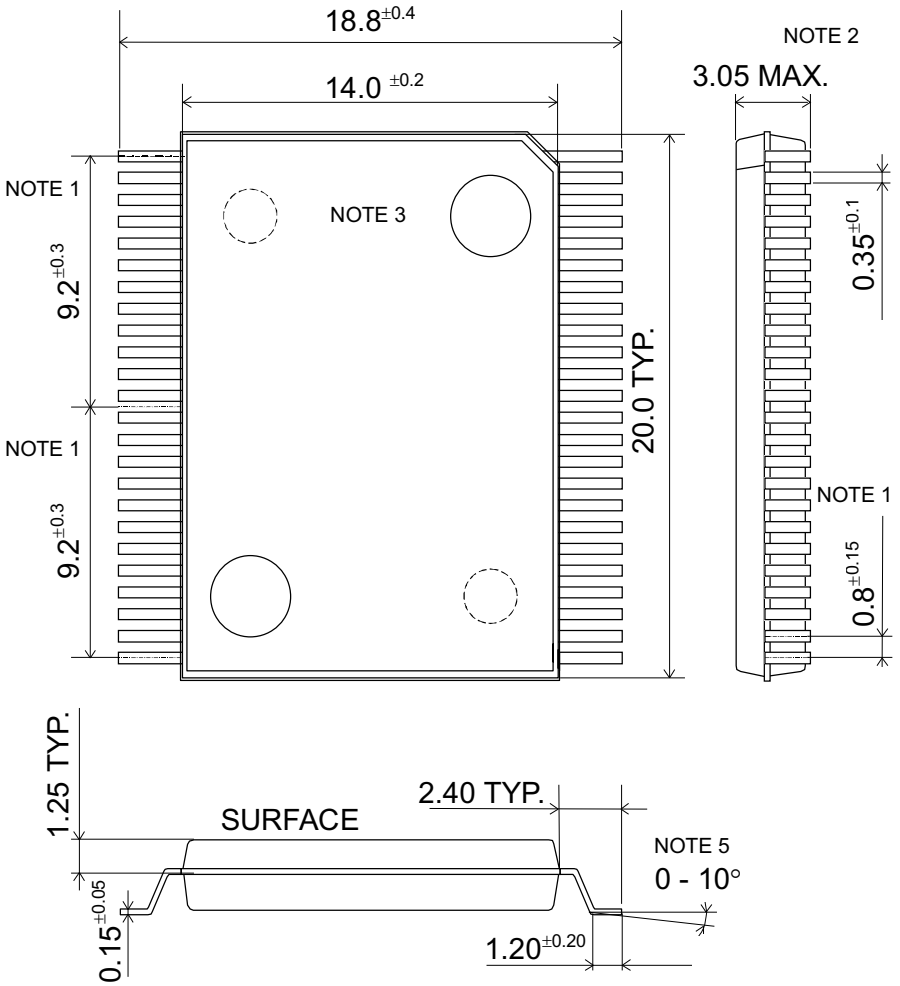
(Unit : mm)

(2) ECN2112



Notes.

1. THIS DIMENSION IS MEASURED AT ROOT OF LEAD. SPACING AT TIP OF LEAD IS MIN 0.2.
2. THIS DIMENSION INCLUDES A WARPAGE OF PACKAGE.
3. MARKING IS ON THE SURFACE OF PACKAGE, INCLUDING HITACHI MARK, TYPE NAME, LOT NUMBER, AND JAPAN MARK.
4. LEADS ARE SOLDER PLATED.
5. THIS IS THE BENDING ANGLE WITH HORIZONTAL PLANE.

Fig. 11. Package outline (ECN2112)

HITACHI POWER SEMICONDUCTORS

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