

Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n -bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 or S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n -bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead

generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 182 and S182 are:

$$C_{n+x} = \bar{G}0 + \bar{P}0 C_n$$

$$C_{n+y} = \bar{G}1 + \bar{P}1 \bar{G}0 + \bar{P}1 \bar{P}0 C_n$$

$$C_{n+z} = \bar{G}2 + \bar{P}2 \bar{G}1 + \bar{P}2 \bar{P}1 \bar{G}0 + \bar{P}2 \bar{P}1 \bar{P}0 C_n$$

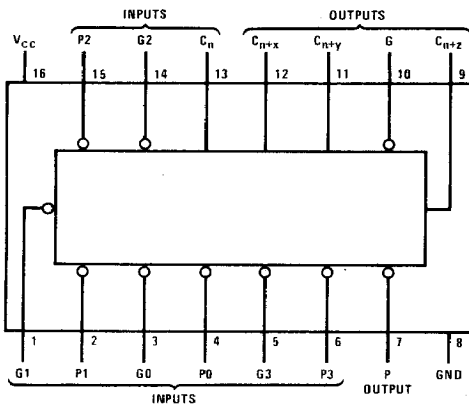
$$\bar{G} = \bar{G}3 (\bar{P}3 + \bar{G}2) (\bar{P}3 + \bar{P}2 + \bar{G}1) (\bar{P}3 + \bar{P}2 + \bar{P}1 + \bar{G}0)$$

$$\bar{P} = \bar{P}3 \bar{P}2 \bar{P}1 \bar{P}0$$

Features

TYPE	TYPICAL PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
182	12 ns	180 mW
S182	7 ns	260 mW

Connection Diagram



54182(J); 74182(J, (N); 74S182(N)

Pin Designations

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x} , C_{n+y} , C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE LOW CARRY GENERATE OUTPUT
P	7	ACTIVE LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54/74			DM74S			UNITS
				182			S182			
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V _{IH}	High Level Input Voltage			2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8			V
V _I	Input Clamp Voltage	V _{CC} = Min	I _I = 12 mA	1.5						V
			I _I = 18 mA				1.2			
I _{OH}	High Level Output Current			-800			-1000			μA
V _{OH}	High Level Output Voltage	V _{CC} = Min, V _{IH} = 2V	DM54	2.4			N/A			V
		V _{IL} = 0.8V, I _{OH} = Max	DM74	2.4			2.7 3.4			
I _{OL}	Low Level Output Current			16			20			mA
V _{OL}	Low Level Output Voltage	V _{CC} = Min, V _{IH} = 2V		0.4			0.5			V
		V _{IL} = 0.8V, I _{OL} = Max								
I _I	Input Current at Maximum Input Voltage	V _{CC} = Max, V _I = 5.5V		1			1			mA
I _{IH}	High Level Input Current	C _n Input	V _{CC} = Max V _I = 2.4V (182) V _I = 2.7V (S182)	80			50			μA
		P3 Input		120			100			
		P2 Input		160			150			
		P0, P1, or G3 Input		200			200			
		G0 or G2 Input		360			350			
		G4 Input		400			400			
I _{IL}	Low Level Input Current	C _n Input	V _{CC} = Max V _I = 0.4V (182) V _I = 0.5V (S182)	-3.2			2			mA
		P3 Input		-4.8			-4			
		P2 Input		-6.4			-6			
		P0, P1, or G3 Input		-8.0			-8			
		G0 or G2 Input		-14.4			-14			
		G1 Input		-16			-16			
I _{OS}	Short Circuit Output Current	V _{CC} = Max(2)		40			-40 -100			mA
I _{CCH}	Supply Current, All Outputs High	V _{CC} = 5V(3)		27			35			mA
I _{CCL}	Supply Current, All Outputs Low	V _{CC} = Max(4)	DM54	45 65		N/A			mA	
			DM74	45 72		69 109				

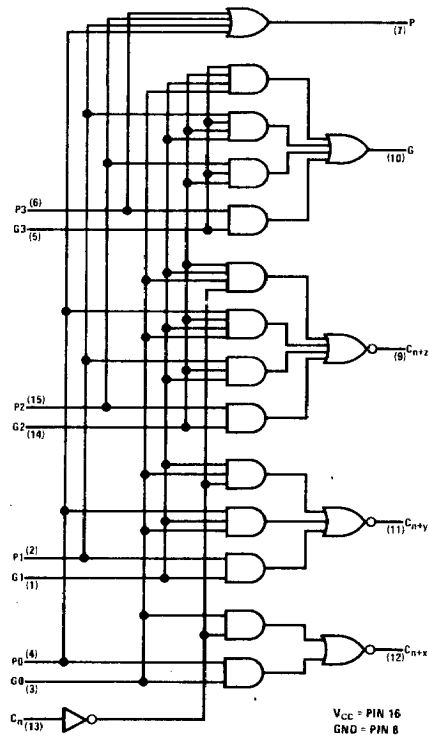
Notes

- (1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.
- (2) Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
- (3) I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.
- (4) I_{CCL} is measured with all outputs open; inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

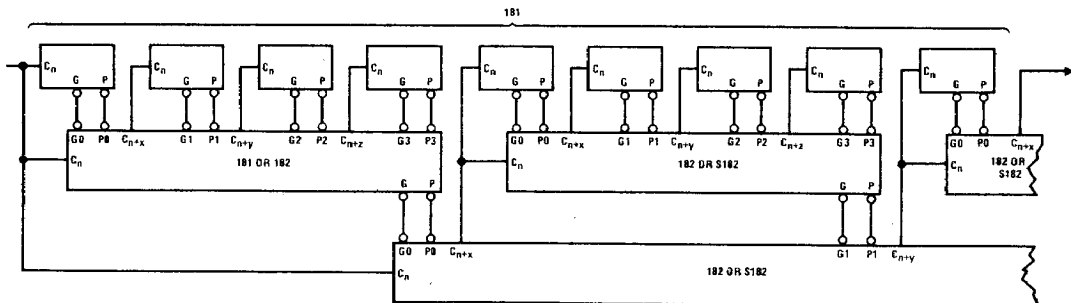
PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74			DM74S			UNITS
					182			S182			
					MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P0, P1, P2, or P3	C _{n+1,x} , C _{n+1,y} , or C _{n+1,z}	R _L = 400Ω C _L = 15 pF (182)	11	17		4	5	7	ns
t _{PHL}	Propagation Delay Time, High-to-Low Level Output				13	22		4	5	7	
t _{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P1, P2, or P3	G		11	17		5	7	10.5	ns
t _{PHL}	Propagation Delay Time, High-to-Low Level Output				13	22		7	10	10.5	
t _{PLH}	Propagation Delay Time, Low-to-High Level Output	P0, P1, P2, or P3	P	R _L = 280Ω C _L = 15 pF (S182)	11	17		4	5	6.5	ns
t _{PHL}	Propagation Delay Time, High-to-Low Level Output				13	22		6	5	10	
t _{PLH}	Propagation Delay Time, Low-to-High Level Output	C _n	C _{n+1,x} , C _{n+1,y} , or C _{n+1,z}		11	17		6	5	10	ns
t _{PHL}	Propagation Delay Time, High-to-Low Level Output				13	22		7	10	10.5	

Logic Diagram



Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



A and B inputs, and F outputs of 181 are not shown.