DF320/DF320A/DF322
CMOS Loop Disconnect Dialers

Siliconix

FEATURES

- 2.5 V to 5.5 V Operation
- 6 μW Standby Dissipation
- Selectable M/S and Impulsing Speed
- Integrated Functions for Fewer External Components

BENEFITS

- Operates on Long and Short Loops
- Presents No Load to Voice
- Versatile
- Low Cost System Implementation

APPLICATIONS

- Push Button Telephones
- Repertory Dialers
- Telex
- Mobile Telephones
- Emergency Number Dialers

DESCRIPTION

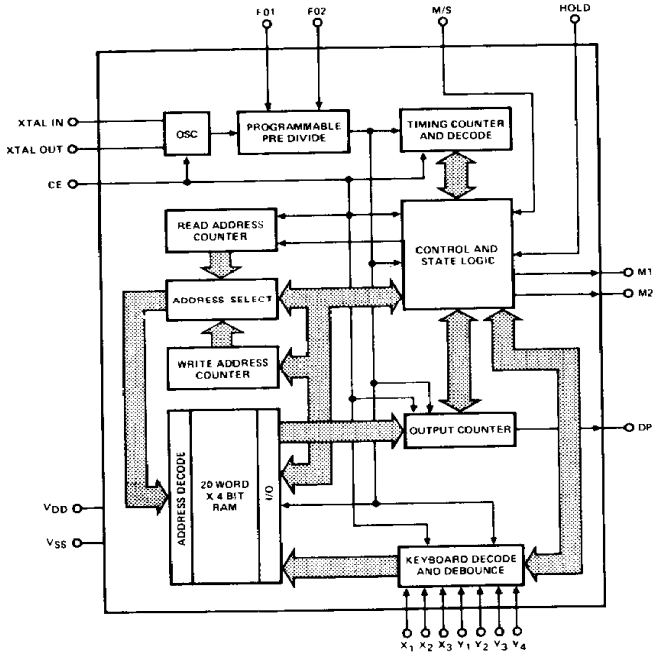
The DF320 series of monolithic CMOS Loop Disconnect Dialers each contain all the logic necessary to interface a standard double contact keyboard to a telephone system requiring loop disconnect signaling.

The DF320 provides the functions most commonly required in the push button telephone application. M1 is the masking option which remains at logic "1" throughout the dialing sequence. The DF322 is identical to the DF320 except that M2 is offered instead of M1. The M2 masking option is at logic "1" only during impulsing, allowing the telephone line to be monitered during the IDP. The DF320A has an extended post impulsing pause of 500 ms.

A dial pulsing output and two output options are provided to control the impulsing (loop disconnect) and muting functions. The circuit is capable of storing a number string of up to 20 digits and re-dialing this stored number automatically at a later time, initiated by a RE-DIAL input code. Impulsing mark/space ratio (M/S), and impulsing rate are pin programmable to meet most telephone authority specifications.

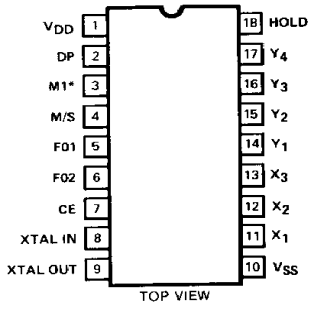
External component count is minimized by the inclusion of an on-chip clock oscillator, high impedance pull-down terminations to programming inputs as well as pull-up terminations to the keyboard giving direct interfacing.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

*M2 ON DF322DJ, DF322DK, DF322DP

Order Numbers:
DF320DJ, DF320ADJ, or DF322DJ
See Package 19
DF320DK, DF320ADK, or DF322DK
See Package 23
DF320DP, DF320ADP, DF322DP
See Package 20

7

ABSOLUTE MAXIMUM RATINGS

$V_{DD} - V_{SS}$ ..... −0.3 V to 8 V
Voltage on Any Pin ..... V_{SS} − 0.3 V to V_{DD} + 0.3 V
Current at Any Pin ..... 10 mA
Operating Temperature ..... −40 to +85° C
Storage Temperature (K Package) ..... −65 to +150° C
(J Package) ..... −65 to +125° C

Power Dissipation (J and K Package)* ..... 450 mW

*Derate 6.3 mW/° C above 25° C. All leads soldered to PC board.

ELECTRICAL CHARACTERISTICS[1, 2]

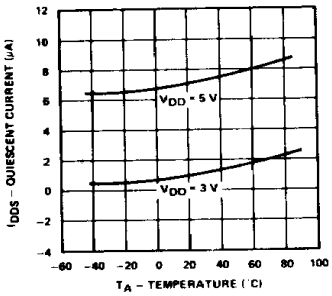
T_A = 25° C

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V_{DD} = 3.0 V, f_{CLK} = 3.579545 MHz	LIMITS MIN[3]	LIMITS TYP[4]	LIMITS MAX	UNIT
Supply Voltage Operating Range	V_{DD}		2.5		5.5	V
Standby Supply Current	I_{DSS}	CE = V_{SS}		2	10	μA
Operating Supply Current	I_{DD}	$C_{XTALOUT}$ = 12 pF		155	250	μA
Keypad Input Pull-Up Transistor Source Current	I_{ILK}	V_{IN} = V_{SS}	−10	−6	−0.5	μA
Keypad Input Leakage Current	I_{IHK}	V_{IN} = V_{DD}		0.1		nA
Programming Input Leakage Current	I_{ILP}	V_{IN} = V_{SS}		−0.1		nA
Programming Input Pull-Down Transistor Sink Current	I_{IHP}	V_{IN} = V_{DD}	0.5	3	10	μA
Input Logic "0" Level (All Inputs)	V_{IL}				0.65	V
Input Logic "1" Level (All Inputs)	V_{IH}		2.45			V
Output Voltage Low Level (DP, M1, M2)	V_{OL}	No Load		0	0.01	V
Output Voltage High Level (DP, M1, M2)	V_{OH}	No Load	2.99	3		V
Output Current Low Level (DP, M1, M2)	I_{OL}	V_{OUT} = +2.3 V	0.5	1.5		mA
Output Current High Level (DP, M1, M2)	I_{OH}	V_{OUT} = +0.7 V		−1.5	−0.5	mA
Output Rise Time (DP, M1, M2)	t_r	C_L = 50 pF		1		μs
Output Fall Time (DP, M1, M2)	t_f	C_L = 50 pF		1		μs
Maximum Clock Frequency	f_{CLK}		3.58			MHz
Mark To Space Ratio	M/S	See Table 1	3:2		2:1	
Interdigit Pause	IDP	T = Selected Impulsing Period (See Table 1)		8T		ms
Impulsing Rate = 1T		See Table 1	10		932	Hz
Clock Start Up Time	t_{ON}	Timed From CE = Logic "1"		1.5	4	ms
Input Capacitance	C_{IN}	Any Input		5		pF
Post Impulsing Pause	POIP	DF320, DF322		0.3T		ms
		DF320A		5T		ms

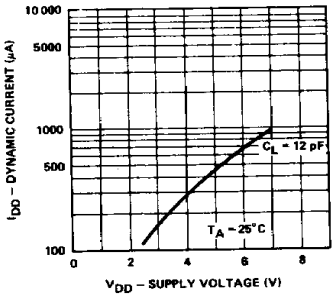
NOTES:
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. All voltages referenced to V_{SS} unless otherwise noted.
3. The algebraic convention whereby the most negative value is minimum, and the most positive value is maximum, is used in this data sheet.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TYPICAL CHARACTERISTICS

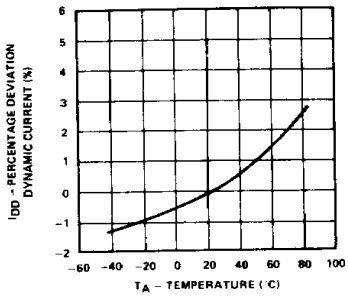
Typical Quiescent Current vs Temperature



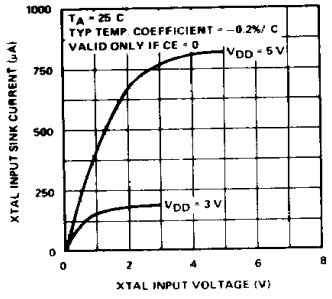
Typical Dynamic Current vs Supply Voltage



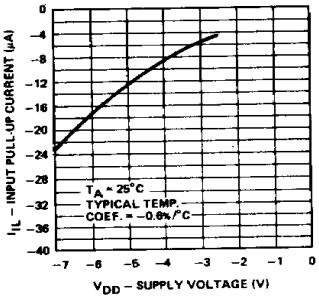
Typical Percentage Deviation of Dynamic Current vs Temperature (Normalized to 25°C)



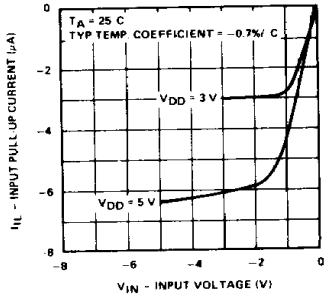
Typical XTAL IN Input Clamp Characteristics



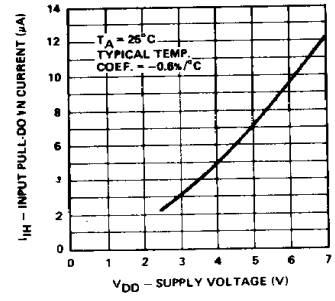
Typical Input Pull-Up Current vs Supply Voltage (X1, Y2, X3, Y1, Y2, Y3, Y4)



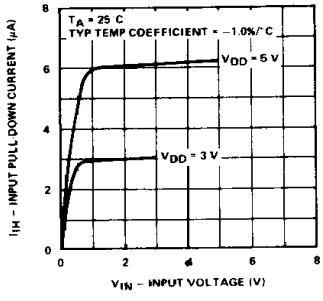
Typical Input Pull-Up Characteristics



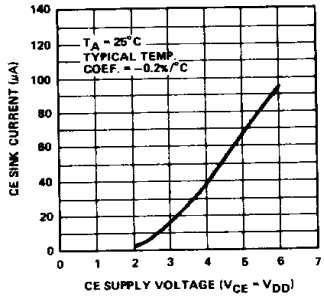
Typical Input Pull-Down Current vs Supply Voltage (M/S, FO1, FO2, Hold)



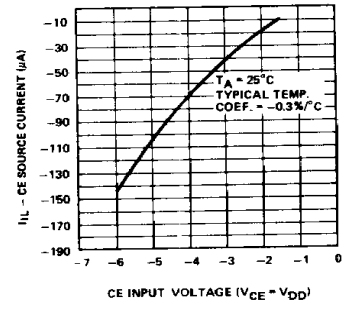
Typical Input Pull-Down Characteristics



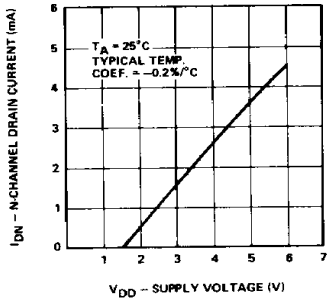
Typical CE Sink Current



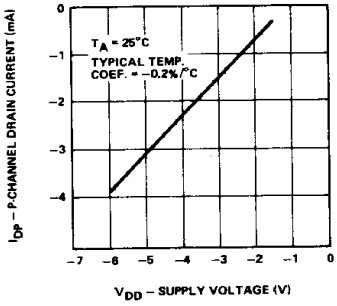
Typical CE Source Current



Typical N-Channel Output Drain Characteristics (DP, M1, M2)



Typical P-Channel Output Drain Characteristics (DP, M1, M2)



7

TYPICAL CHARACTERISTICS (Cont.)

Table 1

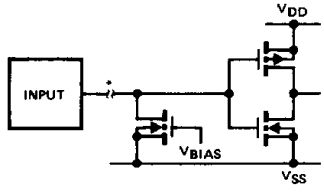
PIN FUNCTION	DESCRIPTION
V_{DD}	Positive voltage supply
DP	Dial Pulsing Output Buffer
M1	Mask 1 (Buffered Output) = Logic "1" during Dialing Sequence
M2	Mask 2 (Buffered Output) = Logic "1" during Impulsing
M/S	Mark/Space (Break/Make) Ratio select. On-chip active pull-down to V_{SS}. O C: 2:1 V_{DD}: 3:2 Note: O C = Open circuit, see Figure 7
F01, F02	Impulsing Rate Selection. On-chip active pull-down to V_{SS}.

F01	F02	Nominal Impulsing Rate	Actual* Impulsing Rate	System Clock Frequency
O C	O C	10 Hz	10.13 Hz	303.9 Hz
O C	V_{DD}	20 Hz	19.42 Hz	582.6 Hz
V_{DD}	O C	932 Hz	932.17 Hz	27,965.1 Hz
V_{DD}	V_{DD}	16 Hz	15.54 Hz	466.1 Hz

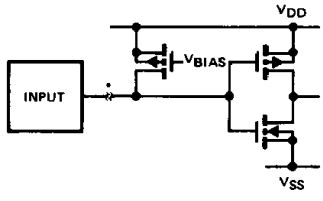
*Assumes f_{CLK} = 3.579545 MHz

CE	Chip Enable. Input/Output, left open it is internally controlled by keyboard decode logic. Can be externally forced for manually enabling chip.
XTAL IN	Crystal Input. Active, clamped low if CE = "0", high impedance if CE = "1".
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.
V_{SS}	System ground
X_1, X_2, X_3	Column keyboard inputs having active pull-ups to V_{DD}. Active LOW
Y_1, Y_2, Y_3, Y_4	Row keyboard inputs having active pull-ups to V_{DD}. Active LOW
HOLD	Prevents further impulsing. On-chip active pull-down to V_{SS} O C: Normal Operation V_{DD}: No Impulsing. If activated during impulsing, hold occurs when the current digit is complete.

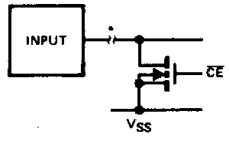
INPUT OUTPUT SCHEMATICS



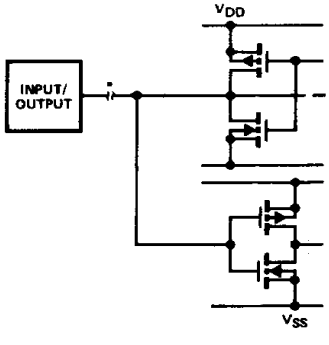
M/S F01, F02, HOLD
Figure 1



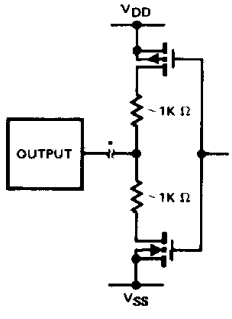
$X_1, X_2, X_3, Y_1, Y_2, Y_3, Y_4$
Figure 2



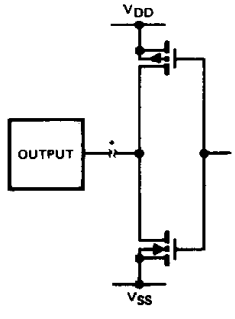
XTAL IN
Figure 3



CE
Figure 4



DP, M1, M2
Figure 5



XTAL OUT
Figure 6

*Circuit Protection Not Shown

FUNCTIONAL DESCRIPTION

1.0 Clock Oscillator – The on-chip oscillator amplifier is connected between the XTAL IN and XTAL OUT pins. The oscillator is completed by connecting a 3,579,545 Hz crystal in parallel with a 10M Ω resistor between XTAL IN and XTAL OUT. When CE = "0" an N-channel transistor clamp is activated, disabling oscillator operation. On the transition of CE to logic "1" a fast oscillator turn-on circuit kicks XTAL IN voltage to the amplifier bias point allowing oscillator operation within 4 ms. The basic clock frequency of 3.58 MHz is predivided by a programmable counter to provide the chip system clock.

As an alternative, an LC oscillator can be formed as shown in Figure 15. Selection of f_{CLK} = 38.4 kHz with F01 connected to V_{DD} will give an impulsing rate of 10 Hz.

It is also possible to control the DF320, DF320A, DF322 from an external clock applied to XTAL IN.

2.0 Chip Enable, CE – The Chip Enable pin is used to initialize the chip system. CE = "0" forces the chip into the static standby mode. In this mode the clock oscillator if OFF, internal registers are reset with the exception of the WRITE ADDRESS COUNTER and the circuit is ready to receive a new number or re-dial. While CE = "0" data cannot be received by the chip, but data previously entered and stored is maintained. When CE = "1" the clock oscillator is operating, the internal registers are enabled, and data can be entered from the keyboard up to a maximum of 20 digits.

CE is primarily controlled by a logic gate with function

F = KEYBOARD INPUT + M1 + HOLD

where + denotes logical OR.

To operate this gate, a resistor and capacitor should be connected in parallel between CE and V_{SS}. When the chip is used in the CE INTERNAL CONTROL MODE power ON reset occurs when V_{DD} is applied, since a logic "0" appears on the CE pin. The chip remains in the static standby condition until it receives the first valid keyboard input after V_{DD} is applied. This is statically decoded and causes CE = "1", hence enabling the clock oscillator. The debounce counter is then clocked by the system clock until the valid data condition is recognized. Data is then written into the on-chip RAM. CE is maintained at logic "1" by M1 during dialing.

The WRITE ADDRESS COUNTER is reset on recognition of the first valid debounced keyboard input provided that it is decoded during t_d of the pre-impulsing pause PIP (see Figure 8). In the CE INTERNAL CONTROL MODE this condition will always apply. When all keyed digits have been dialled, M1 goes to logic "0" and hence the chip returns to the static standby condition. If digits are subsequently keyed during the same OFF-hook period, after a pause in dialling for example, the digit string will be recognized as a new number. This is not important provided RE-DIAL operation is not required.

The alternative to the CE INTERNAL CONTROL MODE is to override the internal logic gate with an externally derived signal. This mode of operation is referred to as the CE EXTERNAL CONTROL MODE. Figure 7 shows that if CE goes to logic "1" in the absence of a keyboard input, a single pulse of duration t_d is generated on M1. This pulse is intended to initialize a bistable latching relay used as shown in Figure 12. Immediately prior to M1 going to logic "1", the WRITE ADDRESS COUNTER is reset. All digits keyed subsequently are entered into consecutive RAM locations up to a maximum of 20. After the WRITE ADDRESS COUNTER has been reset, the RE-DIAL input code will not be recognized by the circuit. It is necessary that CE be maintained at logic "0" $>$ 1 μs after V_{DD} is applied in order to ensure correct system initializing. If CE is linked to V_{DD} by the method shown in Figure 12, adequate delay is obtained.

3.0 Data Entry – Data is entered to the circuit via a double contact keyboard connected as shown in Figure 10. Keyboard inputs are active low and encoded as shown in Table 2.

Keyboard Code
Table 2

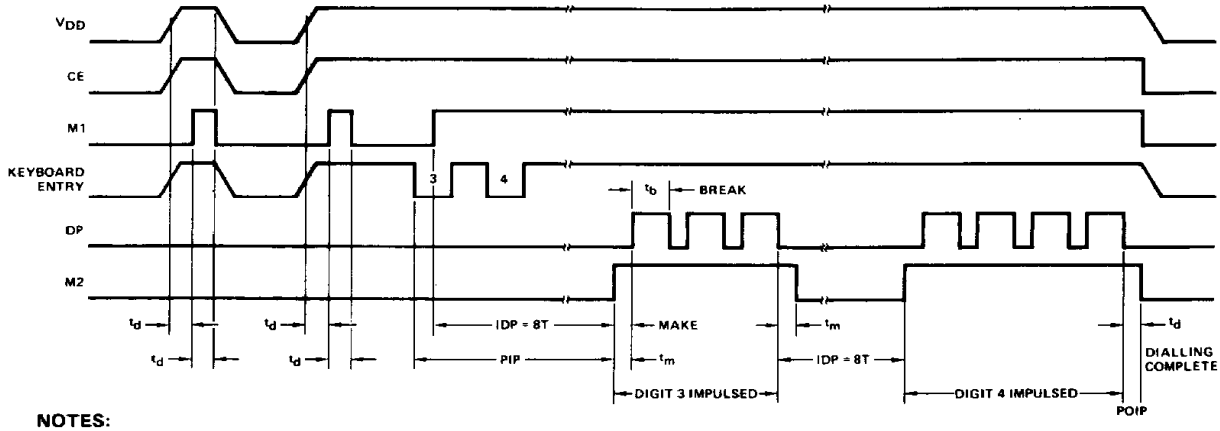
No. of O/P Pulses	Digit	Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0

NOTE: "0" indicates pin taken low.

Keyboard inputs are fully decoded eliminating any possibility of invalid codes being recognized. A BCD format is used on-chip for data storage. Valid inputs have contact bounce removed via the debounce counter. Operation is illustrated in Figure 9. Input data is not written into the RAM until the input code has been present for a minimum of 3P and maximum of 4P (P = System Clock Period). The 1P uncertainty arises since data entry is not synchronized to the system clock. This is indicated by the shaded area on the keyboard entry waveform of Figure 9. The trailing edge of a keyboard entry is also debounced. The operation

of the debounce circuitry results in a maximum data entry rate of SYS CLK ÷ 9. Referring to Figure 9, data must remain stable during the RAM data entry period. Maximum contact bounce rejection is 10 ms at 10 Hz, 6.3 ms at 16 Hz or 5 ms at 20 Hz impulsing rates. Minimum data valid time is 16.7 ms at 10 Hz, 10.4 ms at 16 Hz or 8.4 ms at 20 Hz impulsing rates.

Upon recognition of the first keyboard input of a number string, the dial out sequence is initiated by a pre-impulsing pause (Figure 7). The WRITE ADDRESS COUNTER is incremented on each digit entry. The contents of this counter indicate the length of the number to be dialed. The RE-DIAL code is recognized only if it is presented to the chip a maximum of 5P after CE = "1". Decoding of RE-DIAL then inhibits the reset of the WRITE ADDRESS COUNTER, initiates the dialing sequence and the previous number string entered is dialed. If the circuit application is to utilize RE-DIAL, external CE control is necessary in some cases to ensure that CE = "1" from the first keyboard entry throughout dialing in order to ensure all digits entered are stored consecutively should a delay occur during dialing.



NOTES:

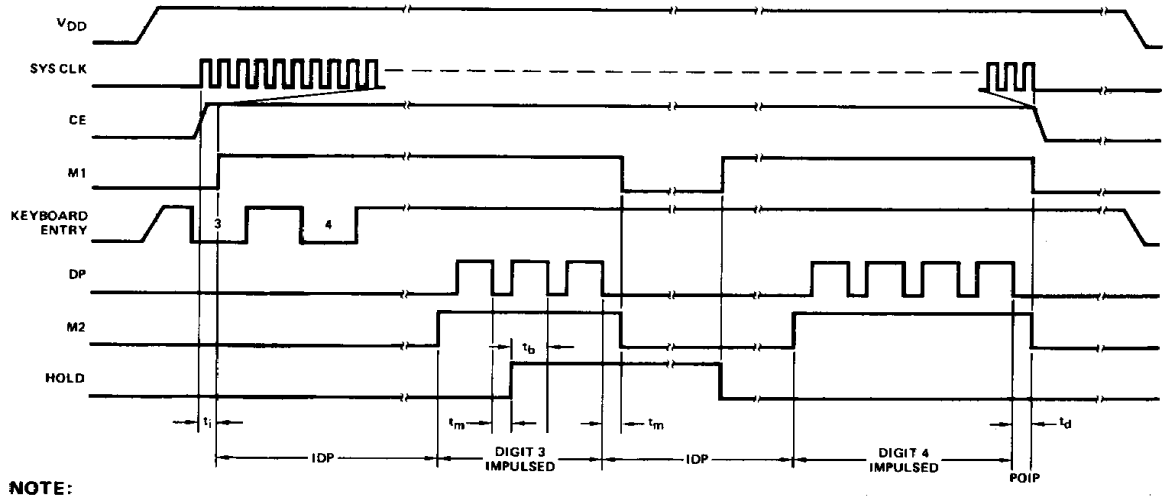
(1) t_d = 10 x P
P = System clock period = T/30
T is selected impulsing period

(2) Pre-Impulsing Pause (PIP) = 8T + t_d

(3) Post-Impulsing Pause (POIP) is equal to t_d ms on DF320, DF322 and 5T on DF320A.

(4) t_b/t_m is the BREAK/MAKE RATIO. T = (t_m + t_b) ms.
t_m = 10 x P for 2:1 M/S ratio. t_m = 12 x P for 3:2 M/S ratio.

Loop Disconnect Dialler Timing CE-External Control
Figure 7



NOTE:

(1) $t_i = t_{ON} + t_d$ where t_{ON} = Clock Start Up Time

Loop Disconnect Dialler Timing CE-Internal Control
Figure 8

FUNCTIONAL DESCRIPTION (Cont.)

4.0 Dialing Sequence - The dialing or impulsing sequence is initiated on recognition of the first keyboard entry after CE = "1". The dialling sequence is identical for both internal and external control of CE. (See Figure 7 and 8).

The basic impulsing pulse train is derived from the TIMING COUNTER AND DECODE. The IDP is timed by forcing a code on the OUTPUT COUNTER and inhibiting DP for the duration of IDP. The READ ADDRESS COUNTER then addresses the RAM and the first digit is used to program the decode of the OUTPUT COUNTER. A number of dial pulses is output via DP corresponding to the BCD data read from the RAM. At the completion of the digit, the READ ADDRESS COUNTER is incremented. The sequence continues until coincidence is recognized between the READ ADDRESS COUNTER contents and the WRITE ADDRESS COUNTER contents. The post-impulsing pause POIP, is then generated. The circuit then enters the dynamic standby condition if CE is maintained at logic "1" by external control, or the static standby condition if CE INTERNAL CONTROL MODE is used.

Impulsing rates, impulsing mark-to-space ratio and inter-digital pause are programmable as shown in Table 1.

The dialing sequence can be interrupted by applying logic "1" to HOLD. If HOLD = "1" is applied during dialing of a digit, the circuit does not enter the HOLD mode until the digit is complete. In the HOLD mode M1 = "0", allowing the telephone line to be monitored. When HOLD is released dialing continues preceded by an IDP. (See Figure 8). HOLD is used to extend the IDP allowing intermediate dial tone recognition if RE-DIAL is used in a PABX for example. Operation can be manual or via external control logic as shown in Figure 13.

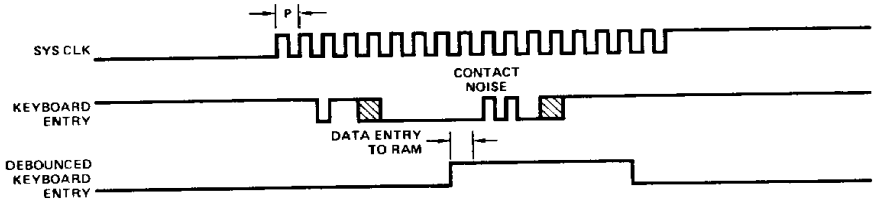
NOTES:

(1) The keyboard input decoding is mask programmable to suit different input codes.

(2) The timing circuitry is mask programmable to give different M/S ratios and IDP values.

(3) The clock predivision circuitry is mask programmable allowing use of different crystal or external clock frequencies.

(4) The logic sense of DP, M1 and M2 outputs is mask programmable.



Keyboard Input Debounce Timing Diagram
Figure 9

APPLICATIONS

The circuit of Figure 10 shows a method of connecting the DF320 in parallel with the telephone network.

When the handset is lifted and power applied to the circuit Q_2 is fed base current through R_2 which in turn drives Q_1. C_2 is charged via R_3 in series with D_1 to $(V_{Z1} - 0.7)V$. When the minimum operating V_{DD} voltage is reached, power ON reset occurs via the CE network of C_1 and R_8. Q_2 is maintained in the ON condition by G_1 while Q_3, and hence Q_4, are held OFF by G_2. The DF320 network appears in parallel with the telephone as an impedance $> 10K\ \Omega$ in the standby condition with the telephone network connected in circuit through Q_1.

On recognition of the first keyed digit, the DF320 clock is started. M1 then goes to logic "1" causing Q_2, Q_1 to turn OFF, and Q_3, Q_4 to turn ON. Hence the majority of the line loop current now flows through Q_4, and Z_1. When impulsing occurs Q_3 and Q_4 are turned OFF by DP acting on G_2. Line loop current is then reduced to approximately 50 μA taken through R_2, R_4 and G_2 in series.

When dialing is complete M1 goes to logic "0" causing the telephone network to be reconnected. The DF320 then returns to the static standby condition. If the line loop is interrupted by the cradle switch during dialing, impulsing will continue until C_2 discharges to a voltage such that R_8 pulls CE to logic "0" causing the DF320 to reset.

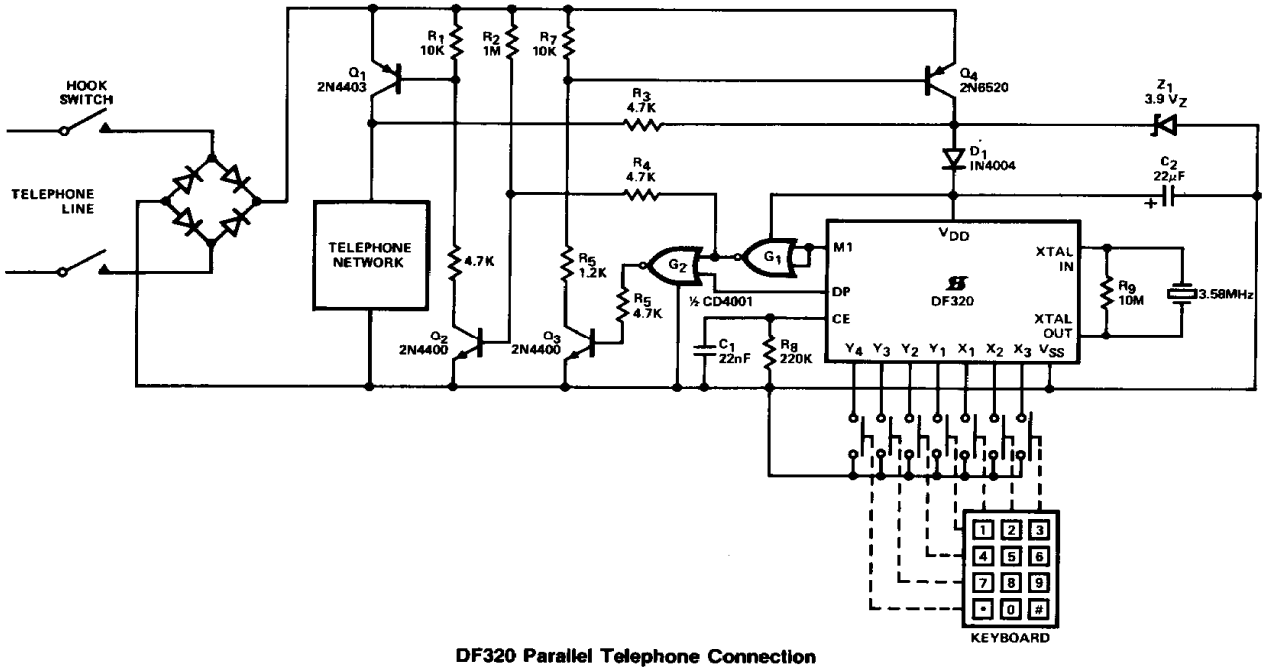
The diode bridge protects the network from line polarity reversal.

The circuit of Figure 11 shows a simple method of series connection of DF320 into the telephone set suitable for PABX or short line applications.

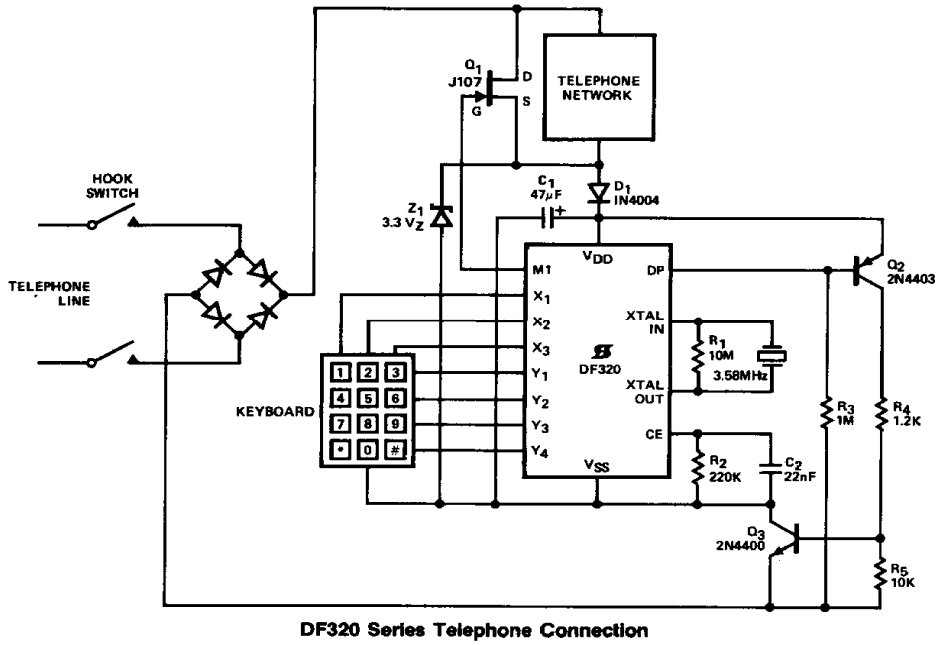
When the telephone handset is lifted, C_1 is charged via D_1 to (V_{Z1} − 0.7) volts and DF320 power ON reset occurs. When the first keyed digit is recognized, M1 goes to logic "1" muting the telephone network by switching on the low ON resistance JFET Q_1, and maximizing the line loop current for impulsing. Impulsing occurs through DP switching Q_2, and hence Q_3, OFF. Rapid discharge of C_1 through Z_1 is prevented during line break by the blocking diode D_1.

When dialing is complete the circuit returns to the static standby condition and Q_1 is switched OFF. Circuit reset during a line interruption by the cradle switch is as for the parallel connection mode.

If a requirement exists that no semiconductor components should appear in the telephone loop during normal speech, the circuit of Figure 12 is required.



DF320 Parallel Telephone Connection
Figure 10



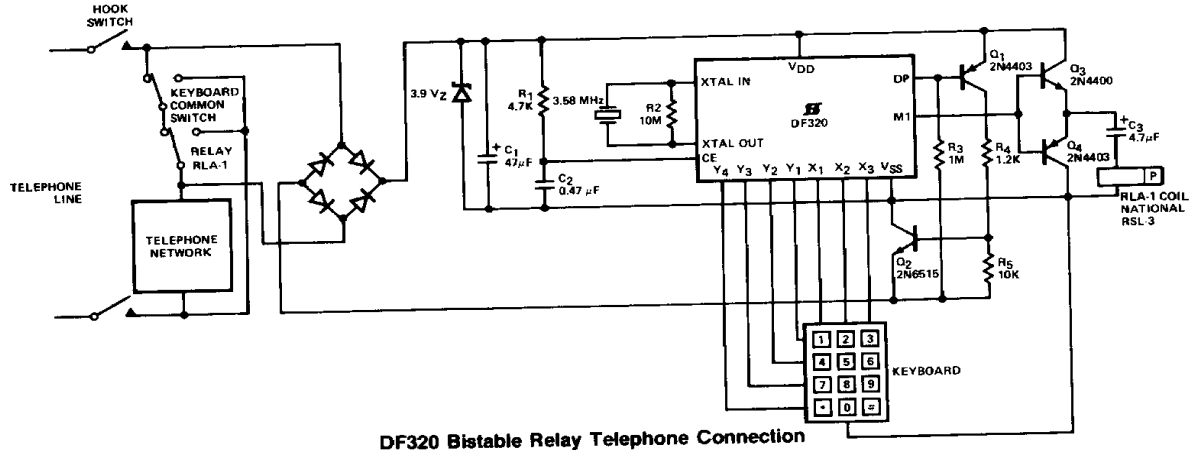
DF320 Series Telephone Connection
Figure 11

APPLICATIONS (Cont.)

While the circuits of Figures 10 and 11 did not require a common keyboard contact, it is necessary to have a common changeover switch in this case operating in conjunction with a bistable relay. In this application external control of CE is provided by the R_1, C_2 network. If, when the handset is lifted, the relay contact is such that the DF320 network is connected in circuit, it is necessary to initialize this relay to reconnect the telephone network. This is achieved by the single pulse which occurs on M1 if CE goes to logic "1" in the absence of a keyboard input (Figure 7).

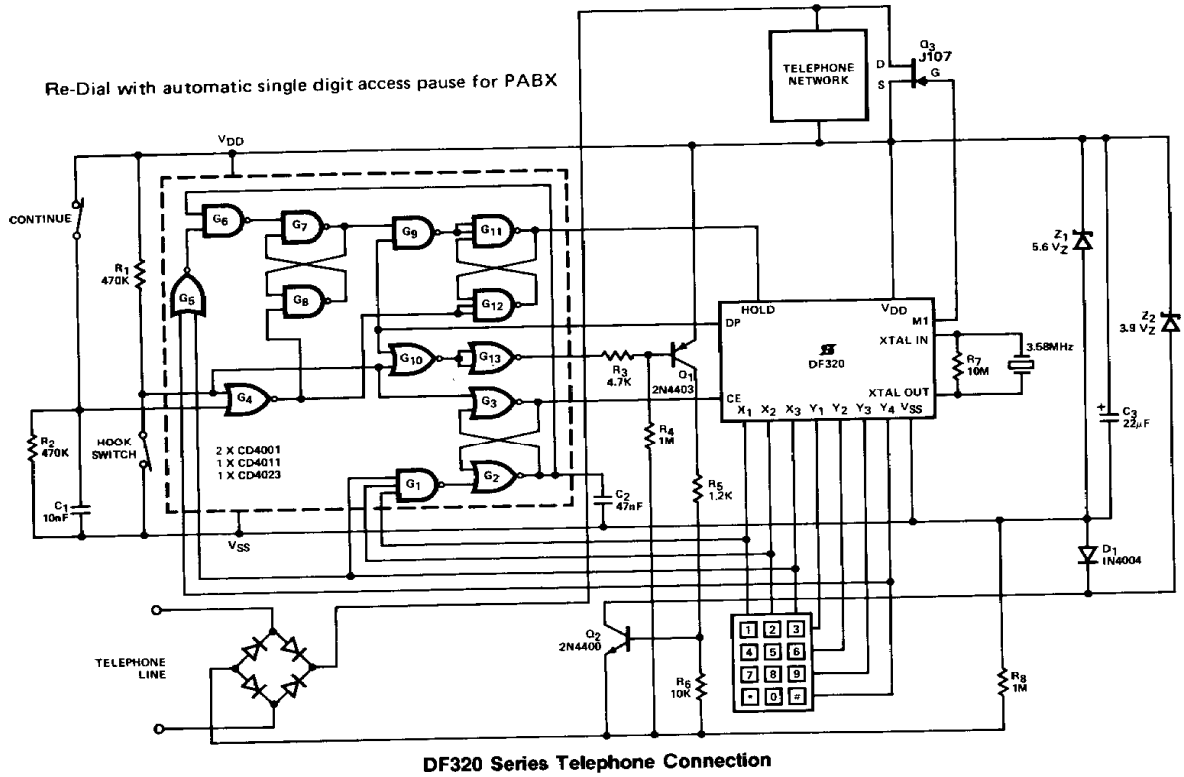
When the first digit is keyed, the DF320 network is connected into the telephone loop and the telephone network short circuited by the keyboard common switch. M1 then goes to logic "1" switching the bistable relay hence maintaining the DF320 network in circuit. Impulsing occurs through DP switching Q_1 OFF which in turn switches Q_2. When dialing is complete the bistable relay is pulsed, switching the telephone network back in circuit and short circuiting the DF320 network.

The circuit of Figure 13 shows additional gating circuitry to provide an automatic access pause after the first digit is dialed, by controlling HOLD. This is useful in PABX applications, eliminating the need for a manual hold facility if RE-DIAL is used.



DF320 Bistable Relay Telephone Connection
Figure 12

Re-Dial with automatic single digit access pause for PABX



DF320 Series Telephone Connection
Figure 13

The basic interface circuit is similar to that shown in Figure 11. Muting is achieved by Q_3 and line switching by Q_2 driven by Q_1.

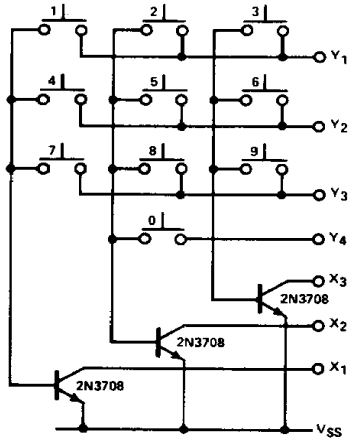
In the ON-hook condition, Q_1 is held OFF by G_{13} and standby current is supplied to the DF320 network by R_8; providing voltage limiting. CE is clamped to logic "0" by G_3. The DF320 is in the static standby mode and the previously dialled number is stored.

When the handset is lifted, G_{13} goes to logic "0" switching Q_1, and hence Q_2, ON. The DF320 network V_{DD} is now given by (V_{Z2} − 0.7) volts. The DF320 remains in the static standby mode until the first key operation. G_1 decodes the common key function toggling the latch formed by G_2 and G_3 causing CE = "1". CE remains at logic "1" throughout the remainder of the OFF-hook condition ensuring that all digits keyed are stored by the DF320 as one number string. (See FUNCTIONAL DESCRIPTION, 3.0 DATA ENTRY).

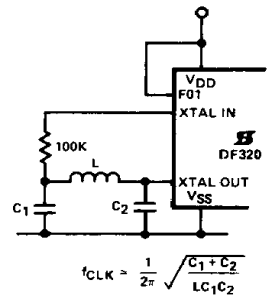
If the first key operated is RE-DIAL, this condition is decoded by G_5, and via G_6 sets the latch formed by G_7 and G_8. G_9 is enabled and the first dial pulse causes the latch formed by G_{11} and G_{12} to be set taking HOLD to logic "1". When the first digit is complete M1 goes to logic "0" enabling the telephone network. When dial tone is recognized the CONTINUE switch is operated causing HOLD = "0" by resetting the latches formed by G_{11}, G_{12} and G_7, G_8. The remainder of the number is then re-dialed. Subsequent operation of RE-DIAL is blocked by G_6.

Figure 14 shows a simple method of interfacing a single contact matrix-type keyboard to the DF320. Operation of a key causes the on-chip pull-up transistor of the Y input to provide base drive current to the corresponding X input external bipolar transistor, which sinks the X input pull-up current through its collector. Hence, a valid code is presented.

As an alternative to the crystal oscillator it is possible to operate the DF320 from an LC combination connected as shown in Figure 15. F01 is connected to V_{DD} selecting the 932 Hz impulsing condition. An oscillator frequency of 38.4kHz will give a 10 Hz impulsing rate.



Single Contact Keyboard Interface
Figure 14



LC Oscillator
Figure 15