21150 PCI-to-PCI Bridge

Specification Update

October 2001

Notice: The 21150 may contain design defects or errors known as errata. Characterized errata that may cause the 21150's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278258-009

Contents

Revision History

Date	Version	Description
10/3/01	009	The following changes have been made in this Specification Update: • Updated Errata table status column on page 7. Updated status for Erratas 2, 3, 4, 5, and 6. • Added fix recommendation1 for Errata 6 "Secondary Clocks Outputs s_clk_o <9:0> may not start-up properly under some conditions". Moved previously existing fix recommendations for Errata 6 to become the second and third recommendations. • Updated Specification Clarification 1 title description on page 16
5/21/01	008	The following changes have been made in this Specification Update: • Updated the title and description of Section 2, "CLK to Signal Valid Delay - Bused Signals (Tval) and Input Hold Timer from CLK (Th) Violations of 66 MHz PCI Signals on the 21150" on page 10. • Updated the status and description of Section 3, "Setup Violations of 66 MHz PCI Control Signals on the 21150" on page 11. • Updated the steppings in Table , "Errata" on page 7. • Updated the 21150 markings naming conventions throughout this document. • Updated the revision of the *PCI Local Bus Specification* from 2.1 to 2.2 within this document.
10/03/00	007	Added new errata item 6:Secondary Clocks Outputs s_clk_o <9:0> may not start-up properly under some conditions.
9/15/00	006	Added documentation change item 13: note added for pull-up resistor for output clocks. Added documentation change items 14 and 15: descriptions of two signals when bus speed is set for 66 MHz.
5/5/00	005	PBGA added, trst_l updates, format of gpio serial data changed, note changed.
11/23/99	004	Modify description of the clamp circuit errata.
9/1/99	003	Added documentation change item 3 for 66 MHz operation. Updated Hold time errata. Added clamp circuit errata.
5/3/99	002	Removed related documents section. Updated errata to reflect stepping C to D status. Added two document changes. See Summary Table of Changes for list.
12/18/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
21150 PCI-to-PCI Bridge Preliminary Datasheet	278106-002
21150 PCI-to-PCI Bridge Evaluation Board User's Guide	278125-001
Considerations When Using the 66 MHz 21150 as an AGP - PCI Bridge White Paper	278214-001
21150 PCI-to-PCI Bridge Hardware Implementation Application Note	278064-002

Nomenclature

Errata are design defects or errors. These may cause the 21150's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 21150 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	G[a]	C	D			
1		X		10	Fixed	"P_FRAME_L, P_IRDY_L, P_TRDY_L, S_FRAME_L, S_IRDY_L and S_TRDY_L Return Inverted Version of Proper Level During JTAG Mode".
2	X	X	X	10	No Fix	"CLK to Signal Valid Delay - Bused Signals (Tval) and Input Hold Timer from CLK (Th) Violations of 66 MHz PCI Signals on the 21150"
3				11	Fixed	"Setup Violations of 66 MHz PCI Control Signals on the 21150"
4	X	X	X	11	No Fix	"Tlow and Tsclk Min Violations of 66 MHz PCI Clock Signals on the 21150"
5		X	X	11	No Fix	"Clamp circuit may not function properly under all conditions."
6		X	X	11	No Fix	Secondary Clocks Outputs s_clk_o <9:0> may not start-up properly under some conditions

a. Stepping for legacy component from Digital Semiconductor.

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	G[a]	C	D			
1			X	15		The 21150 is now available in a 256-pin Plastic Ball Grid Array package.

a. Stepping for legacy component from Digital Semiconductor.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	G[a]	C	D			
1				16		Signal trst_l must be driven low to disable JTAG for normal operation

a. Stepping for legacy component from Digital Semiconductor.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	278106-002	17	Doc	Section 3.0, Figure 5, 21150 Pin Assignment
2	278106-002	18	Doc	Section 10.2, Secondary Clock Control, Figure 20
3	278106-002	18	Doc	Section 10.2, Secondary Clock Control, Table 33

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
4	278106-002	18	Doc	Section 16.6.2, Table 38, Boundary-Scan Order, Pages 138 Through 140.
5	278125-001	21	Doc	Section 4.3, Page 22, Paragraph 1:
6	278064-002	21	Doc	Section 5.1, Initialization, Description
7	278064-002	22	Doc	Serial Clock Mask Shift, Section 4.4.1, Table 4
8	278214-001	22	Doc	Introduction: Section 1.0
9	278106-002	22	Doc	Introduction: Section 1.0
10	278064-002	25	Doc	Section 6.3.1, Signal trst_l Pull-down Resistor, new section
11	278106-002	26	Doc	Section 2.8, JTAG signals, Table 11
12	278106-002	27	Doc	Section 10.2, Secondary Clock Control, Figure 19
13	278064-002	27	Doc	Section 4.2, 21150 Output Clocks
14	278106-002	27	Doc	Section 2.7, Miscellaneous Signals, Table 10
15	278106-002	27	Doc	Section 2.3, Secondary Bus Arbitration Signals, Table 6

Identification Information

Markings

The 21150 is a legacy component that was initially introduced by Digital Semiconductor, a business division of Digital Equipment Corporation. The characteristics are described in the following table:

21150 Marking

Package Markings	Legacy Marking	REV_ID Register Value[a]	Package Type	Speed (MHz)	Stepping
21150AB DC1030G	Yes (Digital Semiconductor)	04h	208-PQFP	33	G[b]
21150BB DC1030G	Yes (Digital Semiconductor)	04h	208-PQFP	66	G[b]
21150AC DC1111C	Yes (Digital Semiconductor)	05h	208-PQFP	33	C
21150BC DC1111C	Yes (Digital Semiconductor)	05h	208-PQFP	66	C
SB21150AC	No	06h	208-PQFP	33	D
SB21150BC	No	06h	208-PQFP	66	D
GD21150AC	No	06h	256-PBGA	33	D
GD21150BC	No	06h	256-PBGA	66	D

a. Identified in a PCI system by reading the value in the REV_ID register.
b. Stepping of legacy component from Digital Semiconductor.

Errata

1. P_FRAME_L, P_IRDY_L, P_TRDY_L, S_FRAME_L, S_IRDY_L and S_TRDY_L Return Inverted Version of Proper Level During JTAG Mode

Problem: This problem exists for parts with REV_ID 5.

For the 21150AC and 21150BC (DC1111C), the P_FRAME_L, P_IRDY_L, P_TRDY_L, S_FRAME_L, S_IRDY_L, and S_TRDY_L pins are incorrect during JTAG testing. This has no effect on the normal functional operation of the device. However, during JTAG testing, errors will be seen.

Correct functionality for JTAG input signals requires that the signal is non-inverting from the pad and that no other pin latches the JTAG input signal. For these 6 pins, the signal is inverted entering the JTAG logic. All other signals are correct (non-inverted).

Implication: Incorrect values will be returned on the affected pins during JTAG testing. This erratum will have no influence on the part in normal application.

Workaround: There are no workarounds for this erratum.

Status: Fixed. Full JTAG functionality has been restored in the DC1111D revision of the part.

2. CLK to Signal Valid Delay - Bused Signals (T_{val}) and Input Hold Timer from CLK (T_h) Violations of 66 MHz PCI Signals on the 21150

Problem: This problem exists for parts with REV_ID 4, REV_ID 5, and REV_ID 6.

Tval violations on 66 MHz PCI signals. The *PCI Local Bus Specification, Revision 2.2*, specifies a Tval time of 6ns in Section 7.6.4.2. The 21150BC requires a maximum Tval time of 6.5ns.

Hold time violations on both 33 MHz and 66 MHz PCI signals. The *PCI Local Bus Specification, Revision 2.2*, specifies a hold time of 0 ns in Section 7.6.4.2. The 21150AB requires a minimum hold time of 1.5 ns. Both the 21150 AC and 21150BC require a minimum hold time of 1.45 ns.

Implication: For hold time, in general, there will be no impact on performance of the 21150. Most PCI devices do not require 0 ns hold.

For Tval on PCI signals other than control, the erratum will slightly reduce the flight time (Tprop). For Tval on control signals, the implication is covered under Erratum #3.

Workaround: There are no workarounds for this erratum.

Status: No Fix.

3. Setup Violations of 66 MHz PCI Control Signals on the 21150

Problem: This problem was thought to exist for parts with REV_ID 5 and REV_ID 6.

Setup time violations on 66 MHz PCI control signals: p_frame_l, p_irdy_l, p_devsel_l, p_stop_l, p_trdy_l, p_lock_l, s_frame_l, s_irdy_l, s_devsel_l, s_stop_l, s_trdy_l, s_lock_l. The *PCI Local Bus Specification, Revision 2.2*, specifies a Setup time of 3 ns in Section 7.6.4.2. The 21150BC requires a maximum setup time of 4.5 ns.

Implication: The combined errata for Setup and Tval on the PCI bus control signals reduce flight time (Tprop) from 5 ns to 3 ns.

Workaround: There are no workarounds for this erratum.

Status: Fixed. The problem was a test fixture setup problem for all versions. It was not a problem with the 21150.

4. Tlow and Tsclk Min Violations of 66 MHz PCI Clock Signals on the 21150

Problem: This problem exists for parts with REV_ID 5 and REV_ID 6.

Tlow violations on 66 MHz PCI clock signals: p_clk, s_clk. The *PCI Local Bus Specification, Revision 2.2*, specifies a Tlow time of 6 ns in Section 7.6.4.1. The 21150BC requires a maximum Tlow time of 7.0 ns.

Tsclk minimum violations on 66 MHz PCI clock signals: p_clk, s_clk. The *21150 PCI-to-PCI Bridge Datasheet* specifies a Tsclk minimum time of 0 ns. The 21150BC requires a minimum Tsclk time of 0.5 ns.

Implication: For Tlow, use of the 21150BC requires tighter conformance to a 50% duty cycle.

For Tsclk minimum, s_clk must lag p_clk by a minimum of 0.5 ns. This condition is met as long as s_clk is an internally or externally buffered version of p_clk and is not generated via PLL to be coincident to p_clk.

Workaround: There are no workarounds for this erratum.

Status: No Fix.

5. Clamp circuit may not function properly under all conditions.

Problem: This problem has been found on parts with REV_ID 5 and REV_ID 6. When either the primary or secondary vio pins are connected to 3.3 volts, the 21150's clamping circuit may not function properly.

Implication: Dependent on the application environment, oscillations or "ringing" have been observed on some PCI control signals (for example, STOP#). The circuitry to generate the input clamp voltages of both the 21150AC and 21150BC is different than that of the 21150AB.

Workaround: When the application topology allows it (short bus lengths, direct etch runs), connecting 3.3 volts to these pins should produce desired results. The use of p_vio and s_vio for both the 21150AC and 21150BC will be determined by the customer application. Designs that adhere to the "Expansion Board Specification" of the *PCI Local Bus Specification*, Revision 2.2 are not affected. Designs whose topology might include long bus lengths might find that connecting s_vio or p_vio to 5 volts leads to improved signal integrity for the corresponding bus. As such, Intel recommends thorough signal integrity analyses prior to a decision on which voltage to connect to these pins.

If there is any 5-volt PCI device on a bus segment, the vio pin for that segment should be tied to the 5 volt supply.

Status: No Fix.

6. Secondary Clocks Outputs s_clk_o <9:0> may not start-up properly under some conditions

Note: This errata only applies to applications that use the 21150 for secondary clocks.

Problem: This problem has been found on the 21150AC and 21150BC. Under repeated and frequent power cycling, the secondary clock circuits may not power up in the proper state, resulting in the device not coming out of reset after power up.

Implication: In a system with a 21150AC or 21150BC that has one of its **s_clk_o<9:0>** outputs fed back to provide the **s_clk**, it is possible that the **s_clk_o<9:0>** output clocks will be driven and remain low, keeping **s_rst_l** asserted, during system power up.

This happens occasionally when a latch whose output disables the serial shift registers on the Secondary clock control powers up in a high state and the shift register bit corresponding to the **s_clk_o<9:0>** output that is fed back also powers up in the high state.

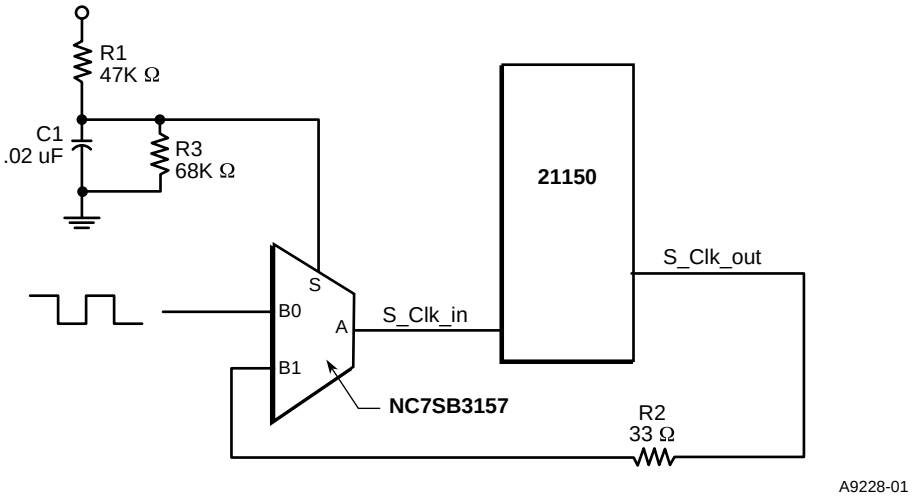
Workaround: Three alternative workarounds are provided for this errata:

- The first is the recommended workaround which will ensure proper operation of the secondary clock outputs s_clk_0<0:9>.
- The second is easier to implement but will not completely eliminate the possibility of failure.
- The third workaround will ensure the secondary clock outputs will operate properly but could result in contention between the s_ckl_0 output and the buffer.

1. Figure 1 illustrates the first recommendatoin - a circuit where an on-board pulse source is gated via the B0 input of the multiplexer to the S_Clock_in pin of the 21150.

   At time 0, the S input of the multiplexer is low, allowing pulses from the on-board pulse source, connected to the B0 input, to be provided to the 21150 S_Clk input pin. When the time determined by the R/C network is satisfied, the S input pin will be in a logic High state. The Multiplexer will then shut off the input pulse from S0 and will direct the S_Clock_out pulses via the B1 multiplexer input, into S_Clock_in.

Figure 1. S_Clock Multiplexer Workaround Circuit for Errata 6.



The values used for the R/C network should be selected to allow a minimum of 2 pulses to be delivered to the 21150 after Vdd has reached 3.0V at a frequency not to exceed the appropriate PCI component. i.e. 30 ns for a 33Mhz bridge. These values should be chosen based on the rise time of the power supply and the frequency of the on board pulse source. The values given for R1, R3, and C1 are for example purposes only.

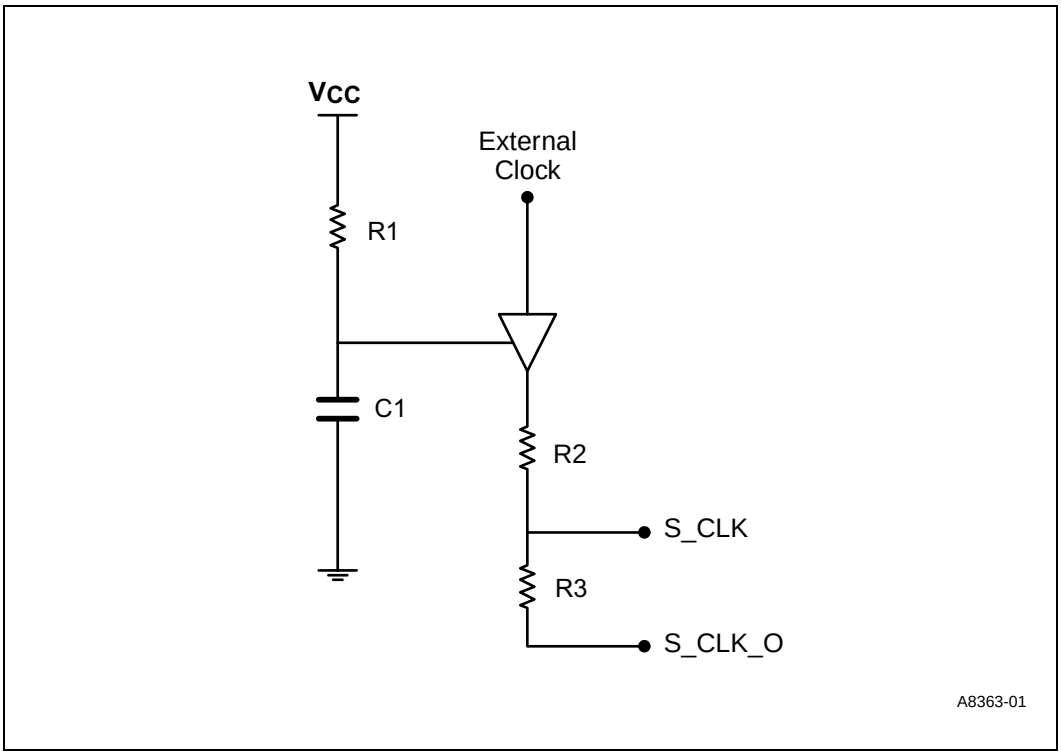
Note: The NC7SB3157 2:1 Multiplexer / Demultiplexer Bus Switch used in this example has a maximum propagation delay of 800ps that should be taken into consideration when matching trace lengths of the clock lines to avoid introducing excessive skew in the clocks. All S_Clock etch lengths must be matched to within 2ns @ 33Mhx or 1ns @66Mhz. The addition of this circuit requires that the etch length for the S_clock_in signal be reduced to compensate for the 800ps delay.

2. In the second recommendation, a pull-up resistor of 22Kohm connected between 3.3V Vcc and the **s_clk** input of the 21150AC and 21150BC part will cause the **s_clk_0<9:0>** outputs to function normally upon power-up. The pull-up resistor tied to Vcc generates a single pulse on the **s_clk** input. This pulse will allow the shift register output to flow through the **s_clk** latch and block the serial shift registers and allow the Secondary Clock Control to clear. When the Secondary Clock Control register is cleared, the **s_clk_o<9:0>** outputs will be enabled. This work around has shown to improve the initialization of the **s_clk** circuits but does not work in all cases.

3. In the third recommendation, to guarantee the proper initialization of the **s_clk** circuits the addition of an external circuit that would provide a minimum of two transitions on the **s_clk** input during the power-up ramp is necessary. This can be done using a solution that drives an external clock onto the **s_clk** input while 3.3V Vcc is ramping during power up.

   Figure 2 illustrates the use of a tristable buffer to provide multiple pulses to the **s_clk** input. The Vcc ramp rate and R1,C1 time constant determine the duration and amplitude of the pulses generated during power up. The R2-R3 values are chosen based on applicable board etch impedance-matching requirements.

Figure 2. Recommended Circuit for a Tristable Buffer



The following should be considered in calculating the R1,C1 time constant

— Make the time constant of the circuit as short as possible, while still ensuring that a minimum of two pulses are generated during the Vcc ramp.

— Phase delay between **s_clk_o** and the external clock should be minimized.

— Matching the external clock and **s_clk_o** frequencies to reduce contention**.**

— Laboratory experiments using **p_clk** as the external clock and a R1C1 time constant between 40 and 60 percent of the Vcc ramp have been successful using this configuration. However the use of **p_clk** as the external clock violates the PCI bus specification for loading of the primary clock.

Status: No Fix.

Specification Changes

1. The 21150 is now available in a 256-pin Plastic Ball Grid Array package.

Specification Clarifications

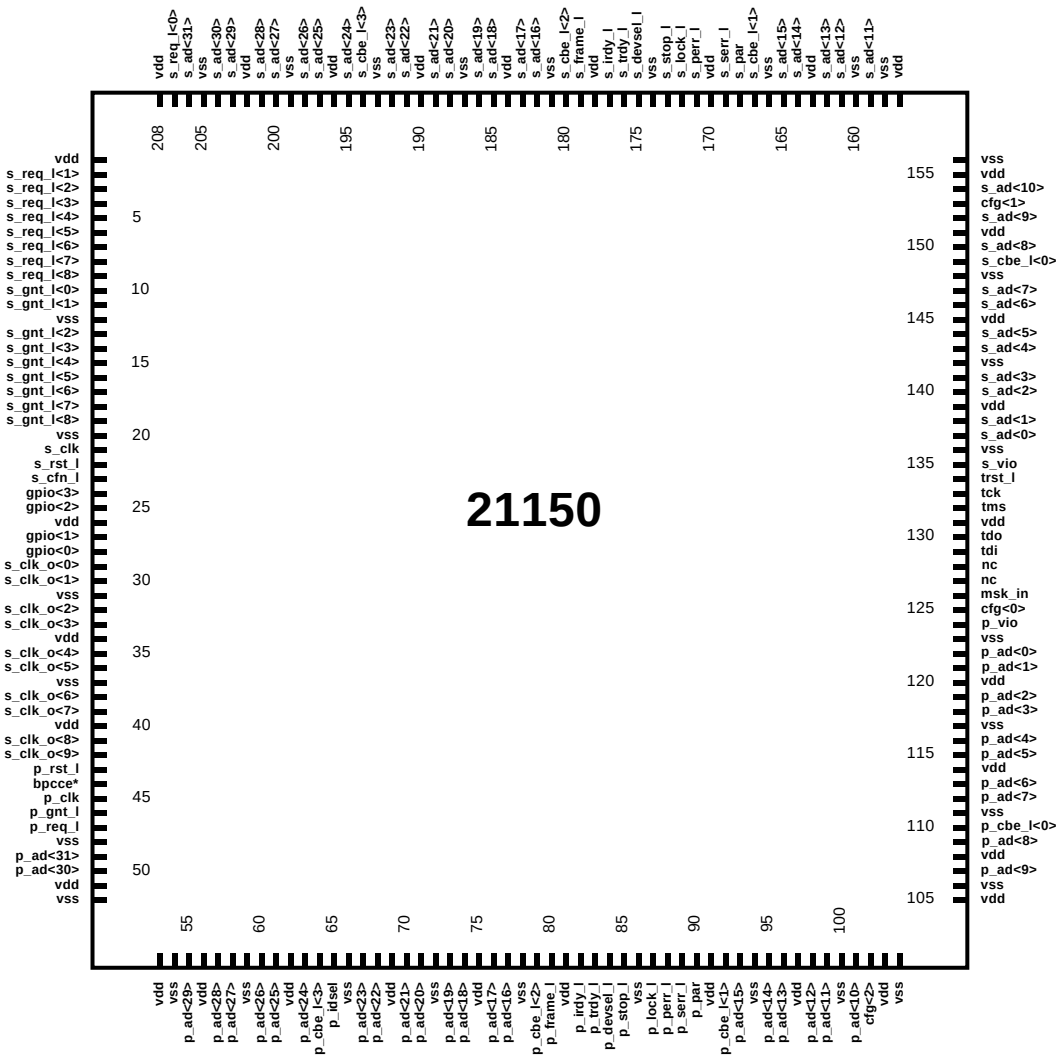
1. Signal trst_l must be driven low to disable JTAG for normal operation

The signal trst_l resets the JTAG circuitry while asserted low. This signal also enables normal JTAG TAP controller operation when high. For normal PCI-to-PCI bridge operation, disable JTAG by pulling trst_l low using a 5K resistor.

Documentation Changes

1. Section 3.0, Figure 5, 21150 Pin Assignment

Pin 44 should be designated bpcce*. The following note should be added to the drawing: *For 21150AB and later revisions only. This is a vss pin for the 21150AA.



* For 21150-AB and later revisions only.
This is a **vss** pin for the 21150-AA.

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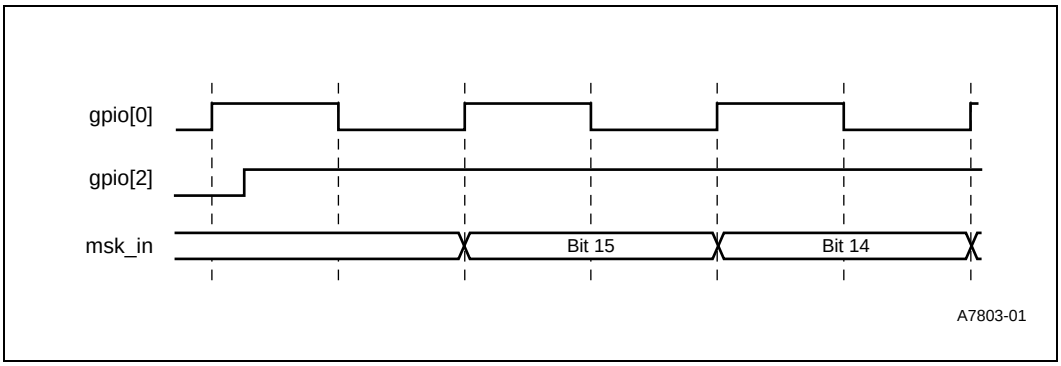
2. Section 10.2, Secondary Clock Control, Figure 20

This figure now appears as follows:

Figure 20. Clock Mask and Load Shift Timing



3. Section 10.2, Secondary Clock Control, Table 33

This table has been re-arranged to indicate the gpio serial data format. It now appears as follows:

Table 33. gpio Serial Data Format

Bit	Description	s_clk_o Output
<15:14>	Reserved	Not applicable
<13>	21150 **s_clk** input	9
<12>	Device 8	8
<11>	Device 7	7
<10>	Device 6	6
<9>	Device 5	5
<8>	Device 4	4
<7:6>	Slot 3 PRSNT#<1:0> or device 3	3
<5:4>	Slot 2 PRSNT#<1:0> or device 2	2
<3:2>	Slot 1 PRSNT#<1:0> or device 1	1
<1:0>	Slot 0 PRSNT#<1:0> or device 0	0

4. Section 16.6.2, Table 38, Boundary-Scan Order, Pages 138 Through 140.

The boundary-scan order pin callouts change from pin 44 through pin 126. The correct pin callout is:

Pin Number	Signal Name	Boundary-Scan Register Number	Group Disable Number	Group Disable Cell
44	bpcce	87	—	—
Note:A new signal, **bpcce**, was added on pin 44 for the 21150AB and later revisions. From pin 45 through pin 126, two values are provided in the xxx/yyy format: the boundary-scan register number in the xxx field is for the 21150AA version only, and the boundary-scan register number in the yyy field is for the 21150AB and later revisions.				
45	p_clk	87/88	—	—

Pin Number	Signal Name	Boundary-Scan Register Number	Group Disable Number	Group Disable Cell
46	p_gnt_l	88/89	—	—
47	p_req_l	89/90	3	—
		90/91	—	3
49	p_ad<31>	91/92	2	—
50	p_ad<30>	92/93	2	—
55	p_ad<29>	93/94	2	—
57	p_ad<28>	94/95	2	—
58	p_ad<27>	95/96	2	—
60	p_ad<26>	96/97	2	—
61	p_ad<25>	97/98	2	—
63	p_ad<24>	98/99	2	—
64	p_cbe_l<3>	99/100	2	—
65	p_isdel	100/101	—	—
67	p_ad<23>	101/102	2	—
68	p_ad<22>	102/103	2	—
70	p_ad<21>	103/104	2	—
71	p_ad<20>	104/105	2	—
73	p_ad<19>	105/106	2	—
74	p_ad<18>	106/107	2	—
76	p_ad<17>	107/108	2	—
77	p_ad<16>	108/109	2	—
		109/110	—	2
79	p_cbe_l<2>	110/111	2	—
80	p_frame_l	111/112	1	—
82	p_irdy_l	112/113	1	—
83	p_trdy_l	113/114	1	—
84	p_devsel_l	114/115	1	—
85	p_stop_l	115/116	1	—
		116/117	—	1
87	p_lock_l	117/118	—	—
88	p_perr_l	118/119	1	—
89	p_serr_l	119/120	1	—
90	p_par	120/121	0	—
92	p_cbe_l<1>	121/122	0	—
93	p_ad<15>	122/123	0	—
95	p_ad<14>	123/124	0	—
96	p_ad<13>	124/125	0	—
98	p_ad<12>	125/126	0	—

Pin Number	Signal Name	Boundary-Scan Register Number	Group Disable Number	Group Disable Cell
46	p_gnt_l	88/89	—	—
47	p_req_l	89/90	3	—
		90/91	—	3
49	p_ad<31>	91/92	2	—
50	p_ad<30>	92/93	2	—
55	p_ad<29>	93/94	2	—
57	p_ad<28>	94/95	2	—
58	p_ad<27>	95/96	2	—
60	p_ad<26>	96/97	2	—
61	p_ad<25>	97/98	2	—
63	p_ad<24>	98/99	2	—
64	p_cbe_l<3>	99/100	2	—
65	p_isdel	100/101	—	—
67	p_ad<23>	101/102	2	—
68	p_ad<22>	102/103	2	—
70	p_ad<21>	103/104	2	—
71	p_ad<20>	104/105	2	—
73	p_ad<19>	105/106	2	—
74	p_ad<18>	106/107	2	—
76	p_ad<17>	107/108	2	—
77	p_ad<16>	108/109	2	—
		109/110	—	2
79	p_cbe_l<2>	110/111	2	—
80	p_frame_l	111/112	1	—
82	p_irdy_l	112/113	1	—
83	p_trdy_l	113/114	1	—
84	p_devsel_l	114/115	1	—
85	p_stop_l	115/116	1	—
		116/117	—	1
87	p_lock_l	117/118	—	—
88	p_perr_l	118/119	1	—
89	p_serr_l	119/120	1	—
90	p_par	120/121	0	—
92	p_cbe_l<1>	121/122	0	—
93	p_ad<15>	122/123	0	—
95	p_ad<14>	123/124	0	—
96	p_ad<13>	124/125	0	—
98	p_ad<12>	125/126	0	—

Pin Number	Signal Name	Boundary-Scan Register Number	Group Disable Number	Group Disable Cell
99	p_ad<11>	126/127	0	—
101	p_ad<10>	127/128	0	—
102	p_m66ena	128/129	—	—
107	p_ad<9>	129/130	0	—
109	p_ad<8>	130/131	0	—
110	p_cbe_l<0>	131/132	0	—
112	p_ad<7>	132/133	0	—
113	p_ad<6>	133/134	0	—
115	p_ad<5>	134/135	0	—
116	p_ad<4>	135/136	0	—
118	p_ad<3>	136/137	0	—
119	p_ad<2>	137/138	0	—
121	p_ad<1>	138/139	0	—
122	p_ad<0>	139/140	0	—
		140/141	—	0
125	config66	141/142	—	—
126	msk_in	142/143	—	—

5. Section 4.3, Page 22, Paragraph 1:

Section 4.3, Paragraph 1is changed to read as follows:

Some versions of the 21150 support 66 MHz operation. Versions marked 21150Ax are not tested to be 66 MHz capable. Versions of the 21150 marked 21150Bx are capable of 66 MHz operation.

6. Section 5.1, Initialization, Description

This section has been changed to:

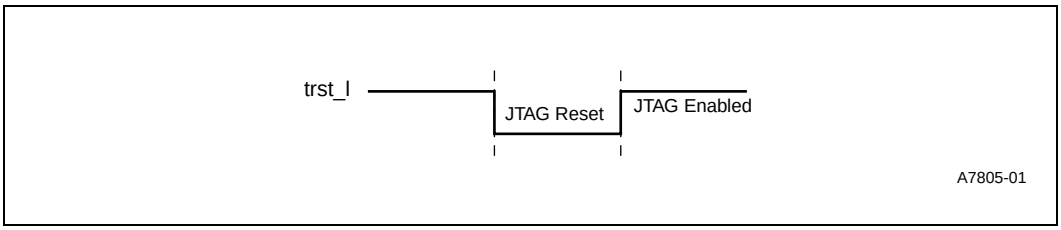
The test access port controller and the instruction register output latches are initialized and JTAG is disabled while the trst_l input is asserted low (see Figure 4). While signal trst_l is low, the test access port controller enters the test-logic reset state. This results in the instruction register being reset which holds the bypass register instruction. During test-logic reset state, all JTAG test logic is disabled, and the device performs normal functions. The test access port controller leaves this state only after trst_l (low) goes high and an appropriate JTAG test operation sequence is sent on the tms and tck pins.

For the 21150 to operate properly, the JTAG logic must be reset. There are two ways to reset this logic:

- The controller will reset asynchronously with the assertion of TRST_L

- The controller will reset synchronously after five TCK clock cycles, with TMS held high.

Figure 4. Signal trst_l States



During normal 21150 operation the JTAG logic must be disabled by pulling trst_l low using a 5K resistor.

7. Serial Clock Mask Shift, Section 4.4.1, Table 4

Table 4, which shows the gpio pin serial data format, has been updated as follows:

Table4. gpio Serial Data Format

Bits	Description	s_clk_o Output
<15:14>	Reserved	Not applicable
<13>	21150 s_clk input	9
<12>	Device 8	8
<11>	Device 7	7
<10>	Device 6	6
<9>	Device 5	5
<8>	Device 4	4
<7:6>	Slot 3 PRSNT#<1:0> or device 3	3
<5:4>	Slot 2 PRSNT#<1:0> or device 2	2
<3:2>	Slot 1 PRSNT#<1:0> or device 1	1
<1:0>	Slot 0 PRSNT#<1:0> or device 0	0

8. Introduction: Section 1.0

The note below figure 1 has been modified and now appears as follows:

Note: While some customers may choose to use the Intel® 21150 PCI-to-PCI bridge as an AGP-PCI bridge, Intel® has not validated nor can it guarantee its use in this type of application. As a result, the information described in this application note is for reference only and any customer that uses Intel® bridges in the manner described does so at their own risk.

9. Mechanical Specifications: Section 18

Figure 26 and Table 51 have been added to show that the 21150 also supports the 256 pin plastic ball grid array.

Figure 26. 21150 256 PBGA Mechanical Drawing

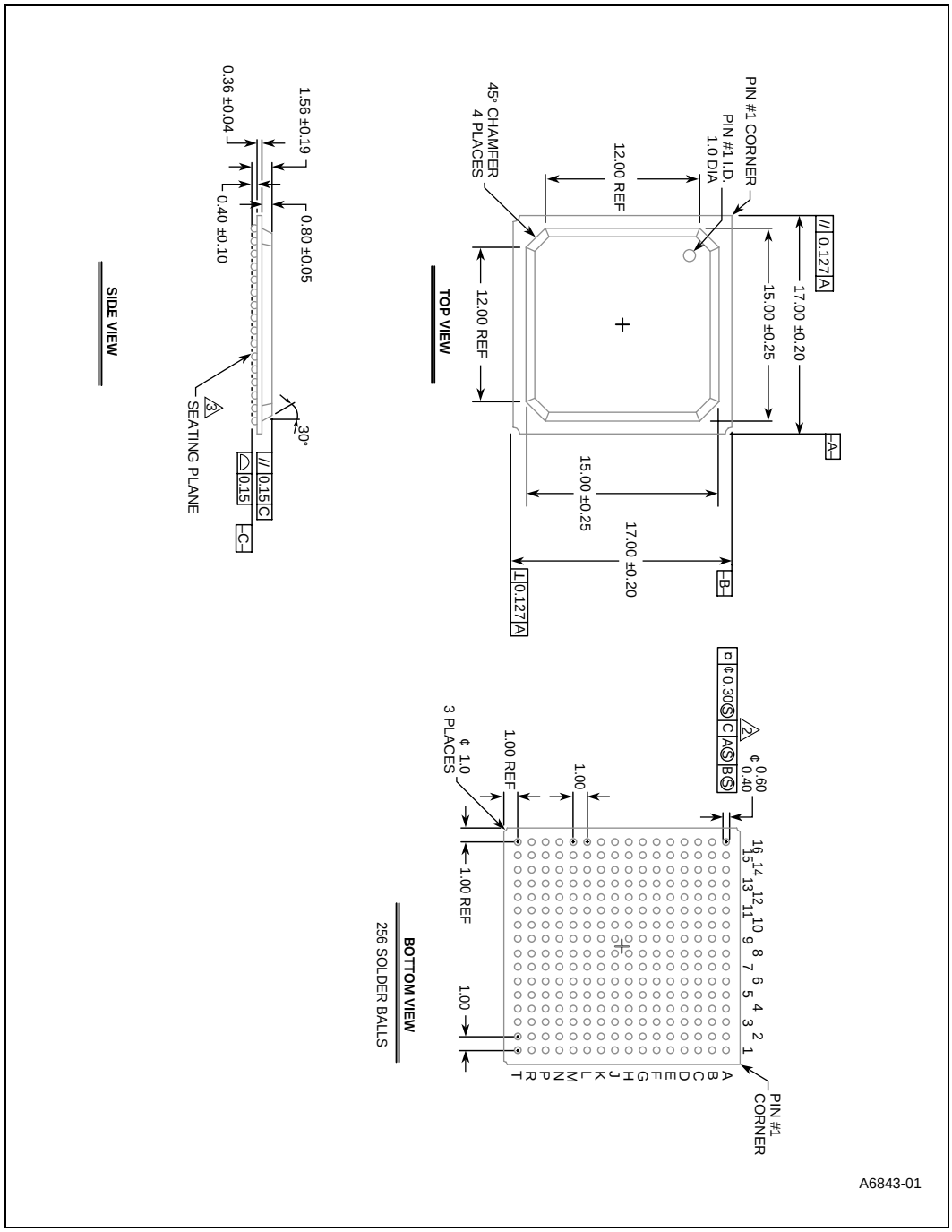


Table 51. Pinout — 256 Plastic Ball Grid Array

Signal	BGA Pad	Signal	BGA Pad	Signal	BGA Pad	Signal	BGA Pad	Signal	BGA Pad
VSSX	A1	s_ad<30>	D5	VSSX	G9	VDDX	K13	p_rst_l	P1
s_req_l<2>	A2	s_ad<26>	D6	VSSX	G10	p_vio	K14	p_req_l	P2
vddi	A3	VDDX	D7	VSSX	G11	msk_in	K15	VSSX	P3
s_ad<31>	A4	VDDX	D8	VDDX	G12	config	K16	vssi	P4
s_ad<28>	A5	VDDX	D9	VDDX	G13	s_clk_o<2>	L1	p_ad<27>	P5
s_ad<25>	A6	VDDX	D10	s_vio	G14	s_clk_o<3>	L2	p_idsel	P6
s_ad<22>	A7	s_serr_l	D11	TRST_L	G15	s_clk_o<5>	L3	p_ad<22>	P7
s_ad<19>	A8	s_ad<14>	D12	s_ad<0>	G16	s_clk_o<6>	L4	p_ad<18>	P8
s_ad<17>	A9	VSSX	D13	s_rst_l	H1	VDDX	L5	p_frame_l	P9
s_frame_l	A10	vssi	D14	s_cfn_l	H2	VSSX	L6	p_devsel_l	P10
s_devsel_l	A11	s_m66ena	D15	s_clk	H3	VSSX	L7	p_serr_l	P11
s_perr_l	A12	s_ad<6>	D16	VDDX	H4	VSSX	L8	p_ad<14>	P12
s_par	A13	s_gnt_l<3>	E1	VDDX	H5	VSSX	L9	vddi	P13
s_ad<13>	A14	s_gnt_l<2>	E2	VSSX	H6	VSSX	L10	VSSX	P14
s_ad<11>	A15	s_req_l<7>	E3	VSSX	H7	VSSX	L11	vddi	P15
VSSX	A16	s_req_l<8>	E4	VSSX	H8	VDDX	L12	p_ad<9>	P16
VSSX	B1	VSSX	E5	VSSX	H9	p_ad<4>	L13	p_gnt_l	R1
VSSX	B2	VDDX	E6	VSSX	H10	p_ad<2>	L14	VSSX	R2
s_req_l<1>	B3	VDDX	E7	VSSX	H11	p_ad<1>	L15	vddi	R3
s_req_l<0>	B4	VDDX	E8	VDDX	H12	p_ad<0>	L16	vssi	R4
s_ad<27>	B5	VDDX	E9	VDDX	H13	s_clk_o<4>	M1	p_ad<24>	R5
s_cbe_l<3>	B6	VDDX	E10	TMS	H14	s_clk_o<8>	M2	p_cbe_l<3>	R6
s_ad<21>	B7	VDDX	E11	TCK	H15	s_clk_o<9>	M3	p_ad<20>	R7
s_ad<18>	B8	VSSX	E12	TDO	H16	p_clk	M4	p_ad<17>	R8
s_cbe_l<2>	B9	s_ad<9>	E13	gpio<1>	J1	VSSX	M5	p_cbe_l<2>	R9
s_irdy_l	B10	s_ad<7>	E14	gpio<2>	J2	VDDX	M6	p_trdy_l	R10
s_stop_l	B11	s_cbe_l<0>	E15	gpio<3>	J3	VDDX	M7	p_lock_l	R11
s_cbe_l<1>	B12	s_ad<4>	E16	VDDX	J4	VDDX	M8	p_ad<15>	R12
s_ad<12>	B13	s_gnt_l<7>	F1	VDDX	J5	VDDX	M9	p_ad<12>	R13
vddi	B14	s_gnt_l<6>	F2	VSSX	J6	VDDX	M10	p_m66ena	R14
VSSX	B15	s_gnt_l<1>	F3	VSSX	J7	VDDX	M11	VSSX	R15
s_ad<10>	B16	s_gnt_l<4>	F4	VSSX	J8	VSSX	M12	vssi	R16
s_req_l<5>	C1	VDDX	F5	VSSX	J9	p_ad<6>	M13	VSSX	T1
s_req_l<4>	C2	VSSX	F6	VSSX	J10	p_ad<7>	M14	p_ad<30>	T2
VSSX	C3	VSSX	F7	VSSX	J11	p_ad<5>	M15	vddi	T3
vddi	C4	VSSX	F8	VDDX	J12	p_ad<3>	M16	p_ad<29>	T4
s_ad<29>	C5	VSSX	F9	VDDX	J13	s_clk_o<7>	N1	p_ad<26>	T5
s_ad<24>	C6	VSSX	F10	nc	J14	bpcce	N2	p_ad<23>	T6
s_ad<23>	C7	VSSX	F11	TDI	J15	p_ad<31>	N3	p_ad<21>	T7
s_ad<20>	C8	VDDX	F12	nc	J16	VSSX	N4	p_ad<19>	T8
s_ad<16>	C9	s_ad<5>	F13	gpio<0>	K1	p_ad<28>	N5	p_ad<16>	T9
s_trdy_l	C10	s_ad<3>	F14	s_clk_o<0>	K2	p_ad<25>	N6	p_irdy_l	T10
s_lock_l	C11	s_ad<2>	F15	s_clk_o<1>	K3	VDDX	N7	p_stop_l	T11
s_ad<15>	C12	s_ad<1>	F16	VDDX	K4	VDDX	N8	p_perr_l	T12
vssi	C13	s_gnt_l<8>	G1	VDDX	K5	VDDX	N9	p_cbe_l<1>	T13
VSSX	C14	vssi	G2	VSSX	K6	VDDX	N10	p_ad<13>	T14
vddi	C15	s_gnt_l<5>	G3	VSSX	K7	p_par	N11	p_ad<10>	T15
s_ad<8>	C16	VDDX	G4	VSSX	K8	p_ad<11>	N12	VSSX	T16
s_gnt_l<0>	D1	VDDX	G5	VSSX	K9	VSSX	N13		
s_req_l<6>	D2	VSSX	G6	VSSX	K10	vssi	N14		
s_req_l<3>	D3	VSSX	G7	VSSX	K11	p_ad<8>	N15		
VSSX	D4	VSSX	G8	VDDX	K12	p_cbe_l<0>	N16		

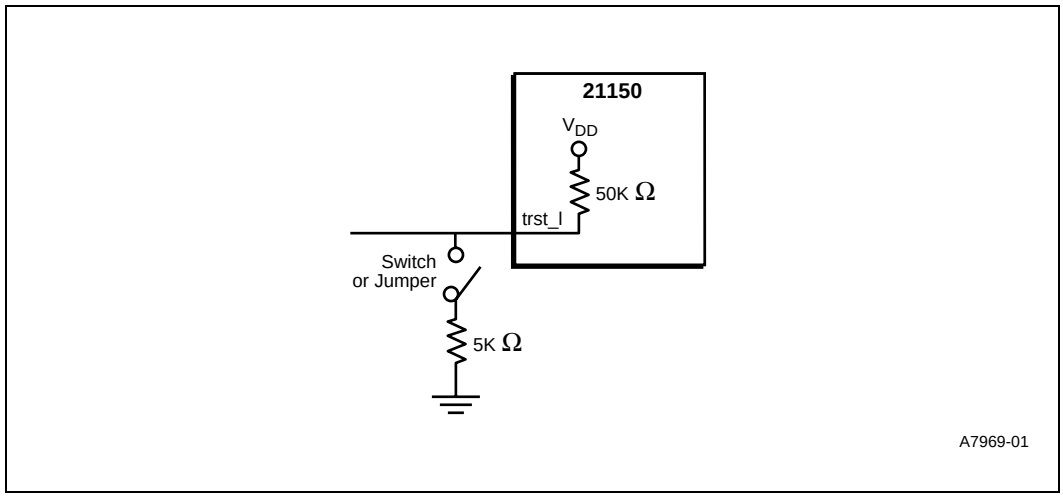
10. Section 6.3.1, Signal trst_l Pull-down Resistor, new section

The following new section has been added:

A 5 K Ω pull-down resistor is required on trst_l for normal PCI-to-PCI bridge operation. However, some JTAG test results may be inconclusive if the 5 K Ω resistor remains in the circuit. To obtain accurate JTAG results, Intel recommends one of the following solutions:

- Verify that the JTAG test equipment, after driving trst_l low to reset the TAP controller, constantly drives trst_l high during JTAG tests. If this signal is not constantly driven high, the 5 K Ω resistor will pull the signal to a low state.
- Remove the 5 K Ω resistor during JTAG tests. This resistor must be installed during normal PCI-to-PCI bridge operation.
- Design external circuits with a switch or jumper to isolate the 5 K Ω resistor during JTAG tests (see Figure 2). This switch must enable the resistor during normal PCI-to-PCI bridge operation.

Figure 2. Removal of pull-down resistor for JTAG testing



11. Section 2.8, JTAG signals, Table 11

The description for tdi, tms, and trst_l have been changed as follows:

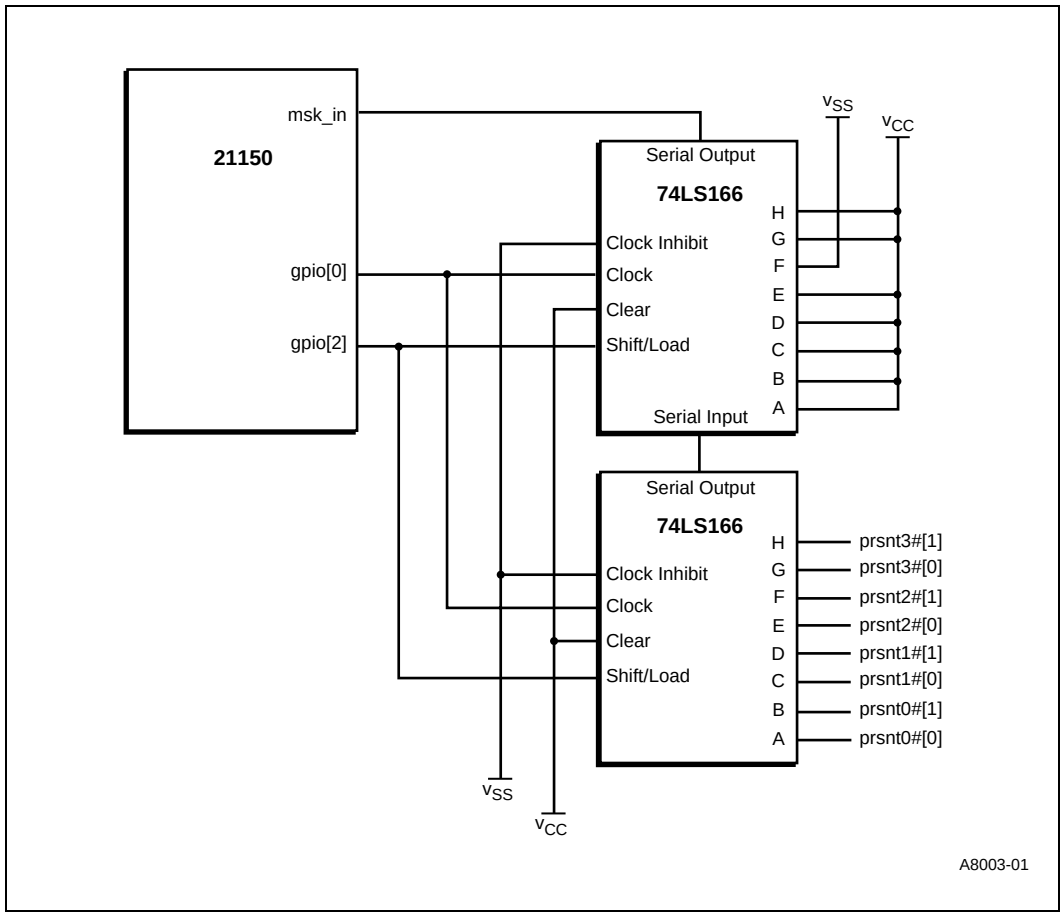
Table 11 JTAG Signals

Signal Name	Type	Description
tdi	I	JTAG serial data in. Signal tdi is the serial input through which JTAG instructions and test data enter the JTAG interface. The new data on tdi is sampled on the rising edge of tck. An unterminated tdi is pulled high by a weak pull-up resistor internal to the device.
tms	I	JTAG test mode select. Signal tms causes state transitions in the test access port (TAP) controller. An unterminated tms is pulled high by a weak pull-up resistor internal to the device.
trst_l	I	JTAG TAP reset and disable. When asserted low, JTAG is disabled and the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic. An unterminated trst_l is pulled high by a weak pull-up resistor internal to the device. The TAP controller must be reset before the JTAG circuits can function. For normal JTAG TAP port operation, this signal must be high. For normal PCI-to-PCI bridge operation of the device, this signal must be pulled low using a 5K resistor.

12. Section 10.2, Secondary Clock Control, Figure 19

This figure now appears as follows:

Figure 19. Example of gpio Clock Mask Implementation on the System Board



13. Section 4.2, 21150 Output Clocks

This note has been added to the end of the section:

Note: Intel recommends that a 22K-ohm pull-up resistor be placed on s_clk to better insure proper initialization on power-up.

14. Section 2.7, Miscellaneous Signals, Table 10

This sentence is added at the end of the description for S_m66ena:

When the secondary bus is set to operate at 66 MHz, s_req_l <8:5> and s_gnt_1<8:5> are disabled.

15. Section 2.3, Secondary Bus Arbitration Signals, Table 6

This sentence is added at the end of the description for s_req_l <8:0>:

When the secondary bus is set to operate at 66 MHz, s_req_l <8:5> is disabled.

This sentence is added at the end of the description for s_gnt_l<8:0>:

When the secondary bus is set to operate at 66 MHz, s_gnt_1 <8:5> is disabled.