

DM54S174/DM74S174, DM54S175/DM74S175 Hex/Quad D Flip-Flops with Clear

General Description

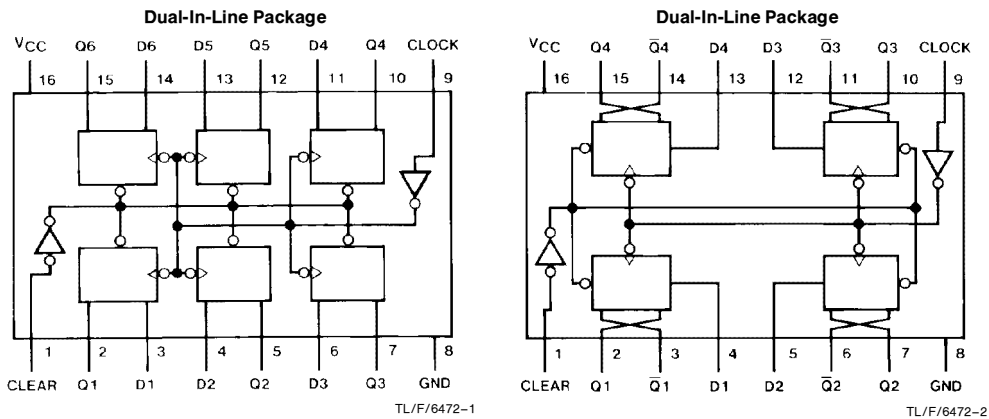
These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- S174 contain six flip-flops with single-rail outputs.
- S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
 - Buffer/storage registers
 - Shift registers
 - Pattern generators
- Typical clock frequency 110 MHz
- Typical power dissipation per flip-flop 75mW

Connection Diagrams



Order Number DM54S174J, DM54S175J, DM54S175W, DM74S174N or DM74S175N
See NS Package Number J16A, N16E or W16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	Q [†]
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q ₀	Q ₀

H = High Level (steady state)

L = Low Level (steady state)

X = Don't Care

↑ = Transition from low to high level

Q₀ = The level of Q before the indicated steady-state input conditions were established.

† = S175 only

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions See Section 1 for Test Waveforms and Output Load

Symbol	Parameter	DM54S174			DM74S175			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			−1			−1	mA
I _{OL}	Low Level Output Current			20			20	mA
f _{CLK}	Clock Frequency (Note 1)	0	110	75	0	110	75	MHz
f _{CLK}	Clock Frequency (Note 2)	0	90	65	0	90	65	MHz
t _w	Pulse Width (Note 1)	Clock	7			7		ns
		Clear	10			10		
	Pulse Width (Note 2)	Clock	9			9		
		Clear	12			12		
t _{SU}	Data Setup Time (Note 1)	5			5		ns	
	Data Setup Time (Note 2)	7			7			
t _H	Data Hold Time (Note 1)	3			3		ns	
	Data Hold Time (Note 2)	5			5			
t _{REL}	Clear Release Time (Note 1)	5			5		ns	
	Clear Release Time (Note 2)	7			7			
T _A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54 DM74	2.5 2.7	3.4 3.4	V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7 \text{ V}$			50	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.5 \text{ V}$			-2	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM54 DM74	-40 -40	-100 -100	mA
I_{CC}	Supply Current (S174)	$V_{CC} = \text{Max}$ (Note 3)		90	144	mA
I_{CC}	Supply Current (S175)	$V_{CC} = \text{Max}$ (Note 3)		60	96	mA

Switching Characteristics at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$ (See Section 1 for Test Waveforms and Output Load)

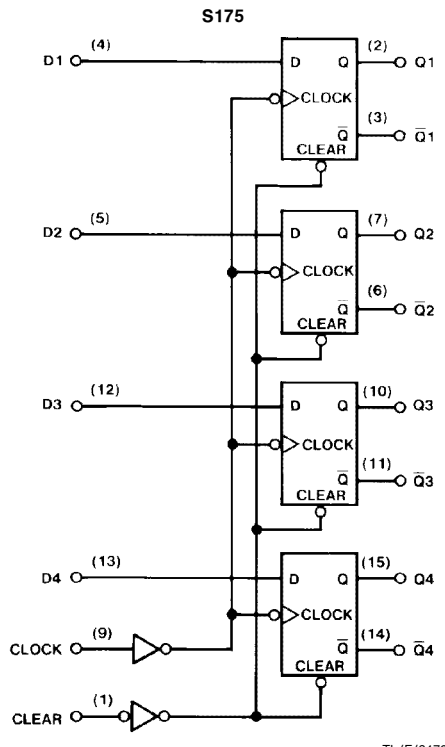
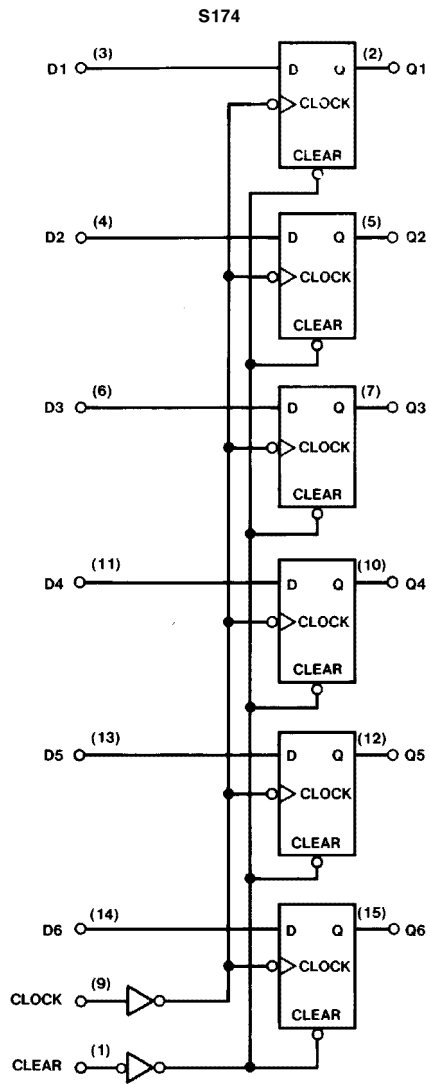
Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		75		65		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		17		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (S175 Only)	Clear to \bar{Q}		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		22		23	ns

Note 1: All typicals are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

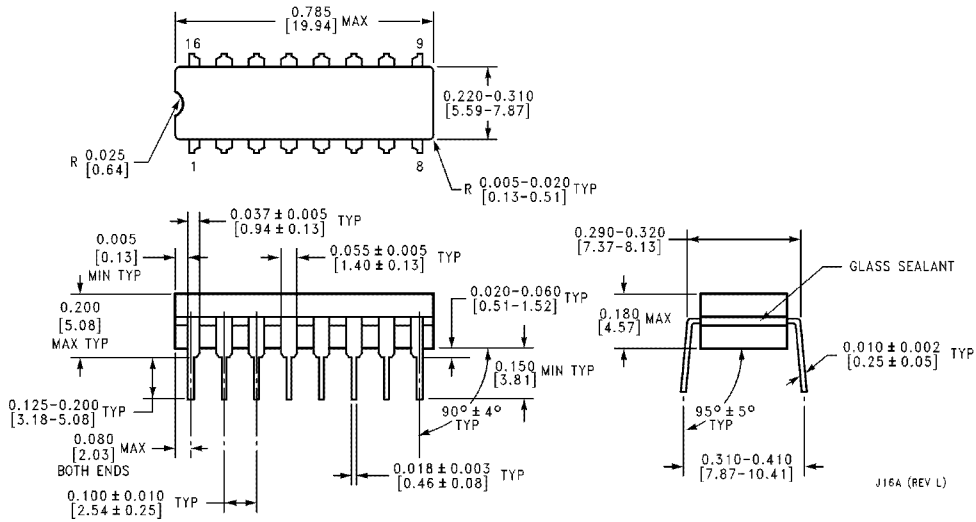
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

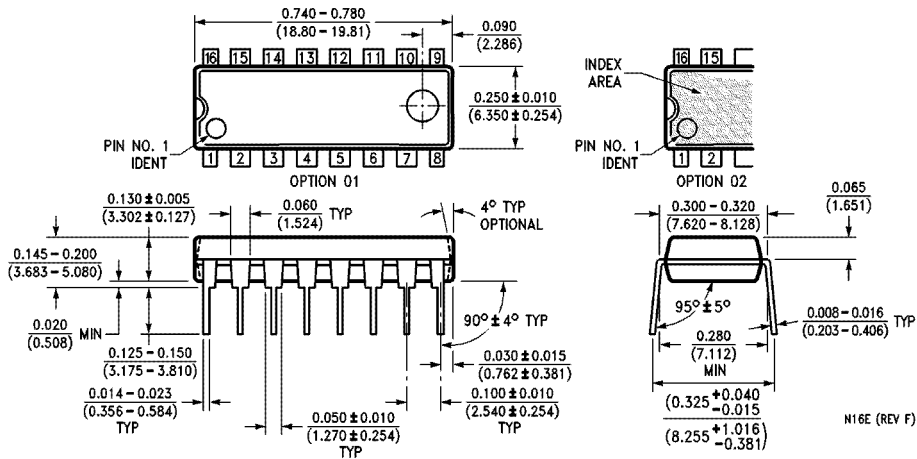
Logic Diagrams



Physical Dimensions inches (millimeters)

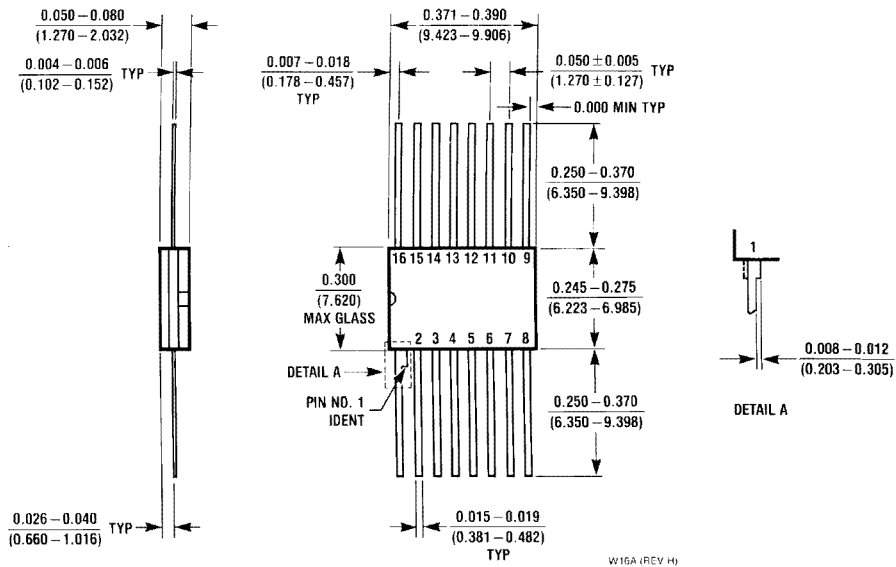


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54S174J or DM54S175J
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74S174N or DM74S175N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number DM54S175W
NS Package Number W16A

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