

## High-Speed, Low-Glitch D/CMOS Analog Switches

### Features

- Fast Switching— $t_{ON}$ : 12 ns
- Low Charge Injection:  $\pm 2$  pC
- Wide Bandwidth: 500 MHz
- 5-V CMOS Logic Compatible
- Low  $r_{DS(on)}$ : 18  $\Omega$
- Low Quiescent Power: 1.2 nW
- Single Supply Operation

### Benefits

- Improved Data Throughput
- Minimal Switching Transients
- Improved System Performance
- Easily Interfaced
- Low Insertion Loss
- Minimal Power Consumption

### Applications

- Fast Sample-and-Holds
- Synchronous Demodulators
- Pixel-Rate Video Switching
- Disk/Tape Drives
- DAC Deglitching
- Switched Capacitor Filters
- GaAs FET Drivers
- Satellite Receivers

### Description

The DG611/612/613 feature high-speed low-capacitance lateral DMOS switches. Charge injection has been minimized to optimize performance in fast sample-and-hold applications.

Each switch conducts equally well in both directions when on and blocks up to 16  $V_{p-p}$  when off. Capacitances have been minimized to ensure fast switching and low-glitch energy. To achieve such fast and clean switching performance, the DG611/612/613 are built on the Siliconix proprietary

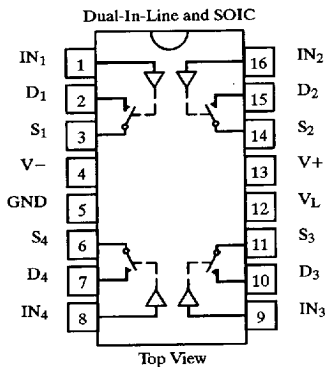
D/CMOS process. This process combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. An epitaxial layer prevents latchup.

The DG611 and DG612 differ only in that they respond to opposite logic levels. The versatile DG613 has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, one DPDT.

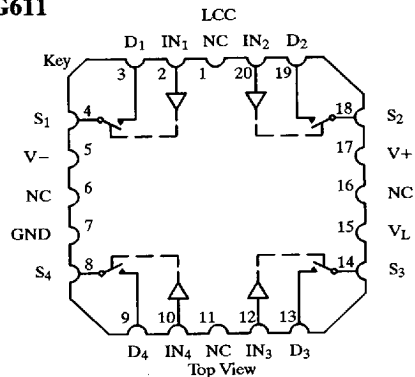
For additional information see Applications Note AN207.

### Functional Block Diagram and Pin Configuration

#### DG611



#### DG611



#### Ordering Information – DG611/612

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG611DJ
		DG612DJ
	16-Pin Narrow SOIC	DG611DY
		DG612DY
-55 to 125°C	16-Pin CerDIP	DG611AK/883
		DG612AK/883
	LCC-20	DG611AZ/883
		DG612AZ/883

#### Four SPST Switches per Package

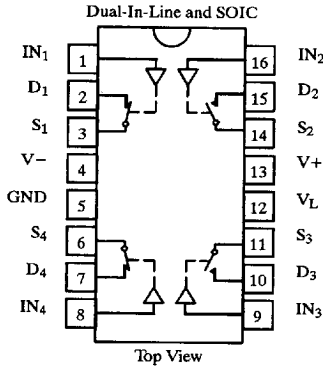
Logic	DG611	DG612
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 1$  V  
Logic "1"  $\geq 4$  V

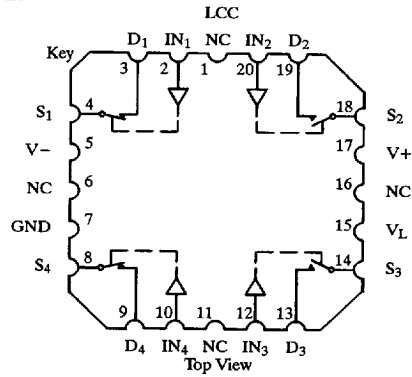
Switches Shown for DG611 Logic "1" Input

**Functional Block Diagram and Pin Configuration (Cont'd)**

**DG613**



**DG613**



**Ordering Information – DG613**

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG613DJ
	16-Pin Narrow SOIC	DG613DY
-55 to 125°C	16-Pin CerDIP	DG613AK/883
	LCC-20	DG613AZ/883

**Four SPST Switches per Package**

**Truth Table**

Logic	SW <sub>1</sub> , SW <sub>4</sub>	SW <sub>2</sub> , SW <sub>3</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 1 V  
Logic "1" ≥ 4 V

Switches Shown for Logic "1" Input

**Absolute Maximum Ratings**

V+ to V-	-0.3 V to 21 V
V+ to GND	-0.3 V to 21 V
V- to GND	-19 V to 0.3 V
VL to GND	-1 V to (V+) + 1 V or 20 mA, whichever occurs first
VIN <sup>a</sup>	(V-) -1 V to (V+) + 1 V or 20 mA, whichever occurs first
Vs, VD <sup>a</sup>	(V-) -0.3 V to (V-) + 16 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal)	±30 mA
Current, S or D (Pulsed at 1 μs, 10% Duty Cycle)	±100 mA
Storage Temperature: CerDIP	-65 to 150°C
Plastic	-65 to 125°C

**Power Dissipation (Package)<sup>b</sup>**

16-Pin Plastic DIP <sup>c</sup>	470 mW
16-Pin Narrow SOIC <sup>d</sup>	600 mW
16-Pin CerDIP <sup>e</sup>	900 mW
20-Pin LCC <sup>e</sup>	900 mW

**Notes:**

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C
- Derate 7.6 mW/°C above 75°C
- Derate 12 mW/°C above 75°C

**CAUTION:** ESD (electrostatic discharge) sensitive. All pins are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Use proper ESD control procedures.

**Recommended Operating Range**

V+	5 V to 21 V
V-	-10 V to 0 V
VL	4 V to V+

VIN	0 V to VL
VANALOG	V- to (V+) - 5 V

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 4\text{ V}, 1\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$	$V_- = -5\text{ V}, V_+ = 12\text{ V}$	Full		-5	7	-5	7	V
Switch On-Resistance	$r_{DS(on)}$	$I_S = -1\text{ mA}, V_D = 0\text{ V}$	Room	18		45		45	$\Omega$
Resistance Match Bet Ch.	$\Delta r_{DS(on)}$		Room	2					
Source Off Leakage	$I_{S(off)}$	$V_S = 0\text{ V}, V_D = 10\text{ V}$	Room Hot	$\pm 0.001$	-0.25 -20	0.25 20	-0.25 -20	0.25 20	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_S = 10\text{ V}, V_D = 0\text{ V}$	Room Hot	$\pm 0.001$	-0.25 -20	0.25 20	-0.25 -20	0.25 20	
Switch On Leakage Current	$I_{D(on)}$	$V_S = V_D = 0\text{ V}$	Room Hot	$\pm 0.001$	-0.4 -40	0.4 40	-0.4 -40	0.4 40	
<b>Digital Control</b>									
Input Voltage High	$V_{IH}$		Full		4		4		V
Input Voltage Low	$V_{IL}$		Full			1		1	
Input Current	$I_{IN}$		Room Hot	0.005	-1 -20	1 20	-1 -20	1 20	$\mu\text{A}$
Input Capacitance	$C_{IN}$		Room	5					pF
<b>Dynamic Characteristics</b>									
Off State Input Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$	Room	3					pF
Off State Output Capacitance	$C_{D(off)}$	$V_D = 0\text{ V}$	Room	2					
On State Input Capacitance	$C_{S(on)}$	$V_S = V_D = 0\text{ V}$	Room	10					MHz
Bandwidth	BW	$R_L = 50\ \Omega$	Room	500					
Turn-On Time <sup>e</sup>	$t_{ON}$	$R_L = 300\ \Omega, C_L = 3\text{ pF}, V_S = \pm 2\text{ V}$ See Test Circuit, Figure 2	Room	12		25		25	ns
Turn-Off Time <sup>e</sup>	$t_{OFF}$		Room	8		20		20	
Turn-On Time	$t_{ON}$	$R_L = 300\ \Omega, C_L = 75\text{ pF}, V_S = \pm 2\text{ V}$ See Test Circuit, Figure 2	Room Full	19		35 50		35 50	
Turn-Off Time	$t_{OFF}$		Room Full	16		25 35		25 35	
Charge Injection <sup>e</sup>	Q	$C_L = 1\text{ nF}, V_S = 0\text{ V}$	Room	4					pC
Ch. Injection Change <sup>e, 8</sup>	$\Delta Q$	$C_L = 1\text{ nF},  V_S  \leq 3\text{ V}$	Room	3		4		4	
Off Isolation <sup>e</sup>	OIRR	$R_{IN} = 50\ \Omega, R_L = 50\ \Omega, f = 5\text{ MHz}$	Room	74					dB
Crosstalk <sup>e</sup>	XTALK	$R_{IN} = 10\ \Omega, R_L = 50\ \Omega, f = 5\text{ MHz}$	Room	87					
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V or } 5\text{ V}$	Room Full	0.005		1 5		1 5	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	-0.005	-1 -5		-1 -5		
Logic Supply Current	$I_L$		Room Full	0.005		1 5		1 5	
Ground Current	$I_{GND}$		Room Full	-0.005	-1 -5		-1 -5		

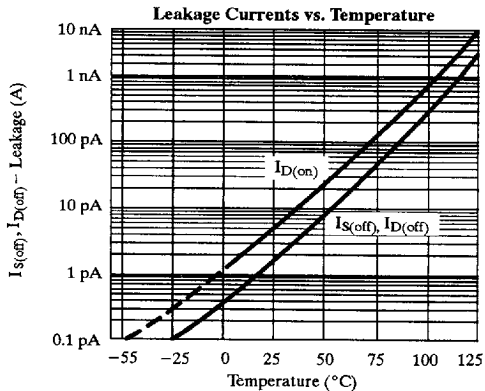
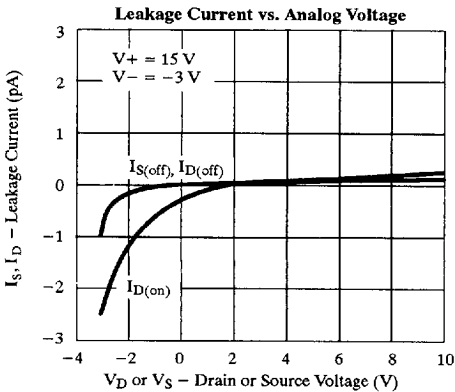
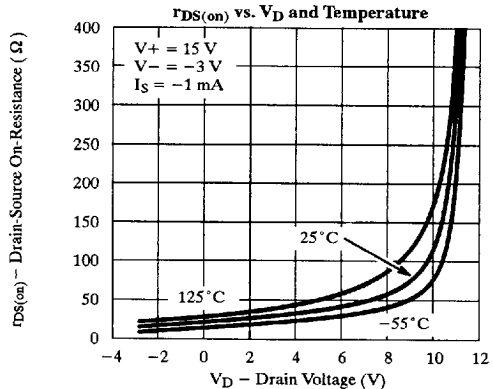
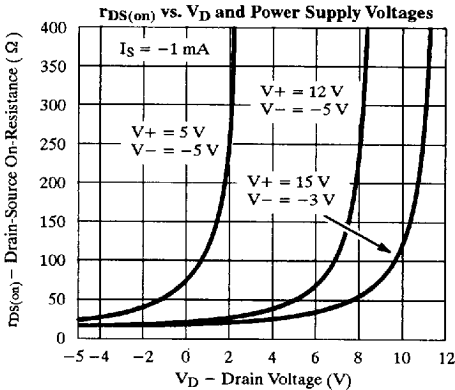
**Specifications<sup>a</sup> for Unipolar Supplies**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 4\text{ V}, 1\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	7	0	7	V
Switch On-Resistance	$r_{DS(on)}$	$I_S = -1\text{ mA}, V_D = 1\text{ V}$	Room	25		60		60	$\Omega$
<b>Dynamic Characteristics</b>									
Turn-On Time <sup>e</sup>	$t_{ON}$	$R_L = 300\ \Omega, C_L = 3\text{ pF}, V_S = 2\text{ V}$ See Test Circuit, Figure 2	Room	15		30		30	ns
Turn-Off Time <sup>e</sup>	$t_{OFF}$		Room	10		25		25	

Notes:

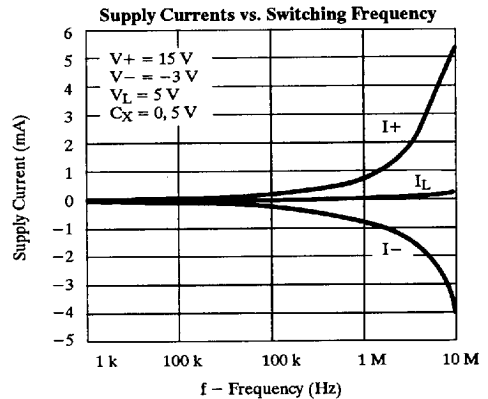
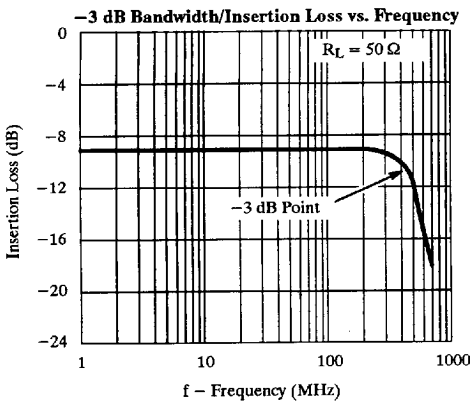
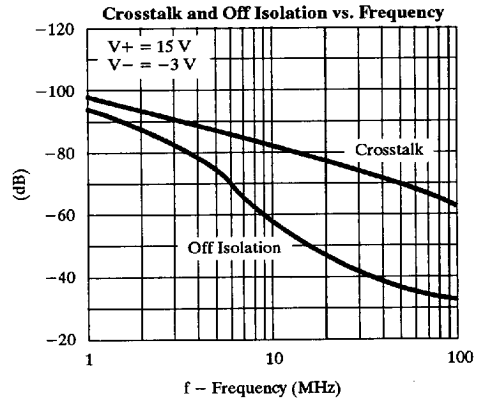
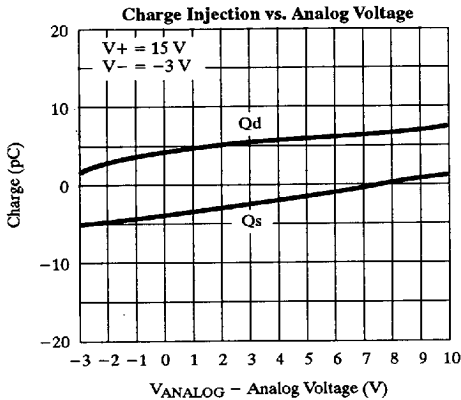
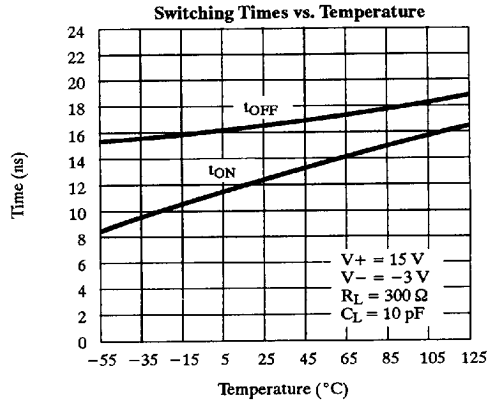
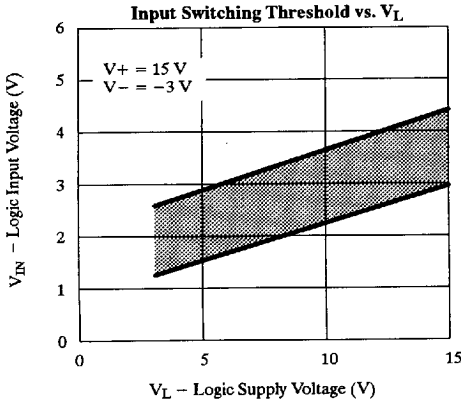
- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.
- g.  $\Delta Q = |Q \text{ at } V_S = 3\text{ V} - Q \text{ at } V_S = -3\text{ V}|$ .

**Typical Characteristics**



**1**

## Typical Characteristics (Cont'd)



**Schematic Diagram (Typical Channel)**

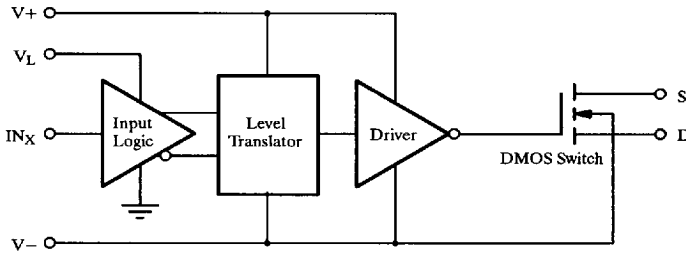
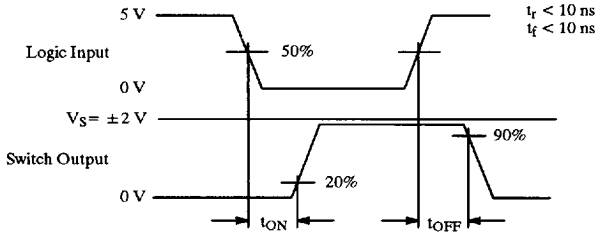
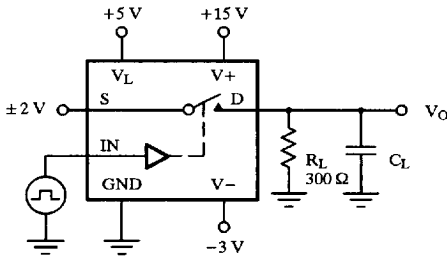


Figure 1.

**Test Circuits**



C<sub>L</sub> (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

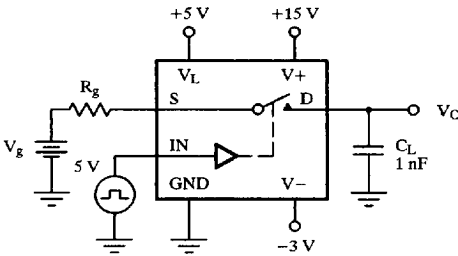
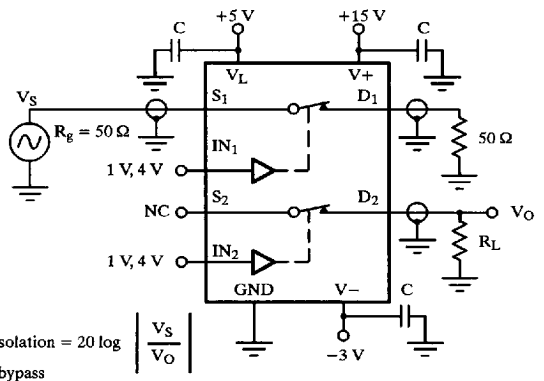


Figure 3. Charge Injection



X<sub>TALK</sub> Isolation = 20 log  $\left| \frac{V_S}{V_O} \right|$   
C = RF bypass

Figure 4. Crosstalk

## Applications

### High-Speed Sample-and-Hold

In a fast sample-and-hold application, the analog switch characteristics are critical. A fast switch reduces aperture uncertainty. A low charge injection eliminates offset (step) errors. A low leakage reduces droop errors. The Si581, a fast input buffer, helps to shorten acquisition and settling

times. A low leakage, low dielectric absorption hold capacitor must be used. Polycarbonate, polystyrene and polypropylene are good choices. The JFET output buffer reduces droop due to its low input bias current. (See Figure 5.)

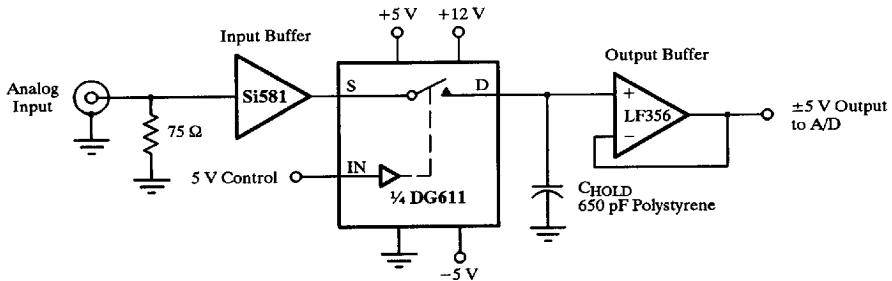


Figure 5. High-Speed Sample-and-Hold

### Pixel-Rate Switch

Windows, picture-in-picture, title overlays are economically generated using a high-speed analog switch such as the DG613. For this application the two video

sources must be synclocked. The glitch-less analog switch eliminates halos. (See Figure 6.)

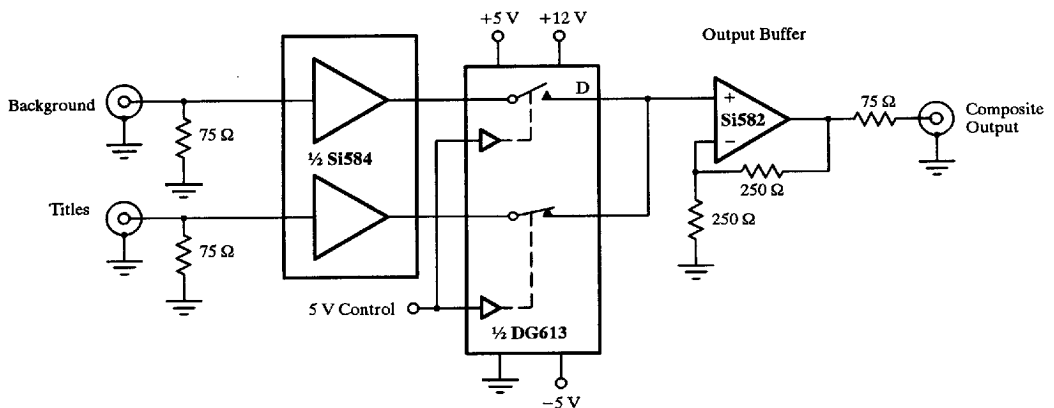


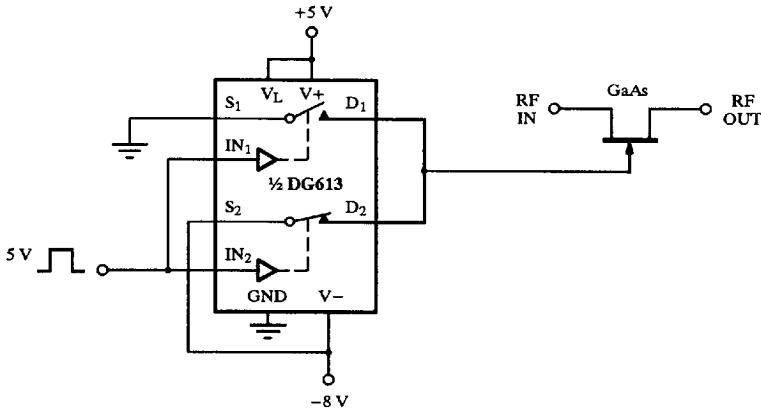
Figure 6. A Pixel-Rate Switch Creates Title Overlays

**Applications (Cont'd)**

**GaAs FET Drivers**

Figure 7 illustrates a high-speed GaAs FET driver. To turn the GaAs FET on 0 V are applied to its gate via S<sub>1</sub>, whereas to turn it off, -8 V are applied via S<sub>2</sub>. This high-speed,

low-power driver is especially suited for applications that require a large number of RF switches, such as phased array radars.



**Figure 7. A High-Speed GaAs FET Driver that Saves Power**