M27210
1M (64K x 16) WORD-WIDE EPROM
MILITARY

- **Military Temperature Range**
  - **— −55°C to +125°C (T_C)**
- **High-Performance HMOS* II-E**
  - **— 200 ns Access Time**
  - **— Low 200 mA Active Power**
- **Complete Upgrade Capability**
  - **— PGM "Don't Care" Status Allows Wiring in Higher Order Addresses**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm—8 Seconds Typical**
- **New Word-Wide Pinout**
  - **— Clean, "Flow-Through" Architecture**
- **Standard EPROM Features**
  - **— TTL Compatibility**
  - **— Two Line Control**
- **40-Pin DIP**

The Intel M27210 is a 5V only, 1,048,576-bit, Electrically Programmable Read Only Memory. It is organized as 64K-words of 16 bits each. It defines a new-clean memory architecture, oriented toward high-performance 16-bit and 32-bit CPUs, which simplifies circuit layout and offers a pin-compatible growth path to higher densities.

The M27210's unique circuit design provides for no-hardware-change upgrades to 4M-bits in the future. Since the $\overline{PGM}$ pin is a "don't care" state during read mode, direct connections to higher order addresses, A16 and A17, can be made without affecting the device's read operation. The M27210 will be offered in a DIP with the same 4M-bit upgrade path.

The M27210 provides the highest density and performance available to 16-bit and 32-bit microprocessors. Its by-16 organization makes it an ideal single-chip firmware solution in most microprocessor applications. The M27210's large capacity is sufficient for storage of operating system kernels in addition to standard bootstrap and diagnostic code. Direct execution of operating system software is made possible by the M27210's fast 200 ns access time, which yields no-WAIT-state operation in such high-performance CPUs as the 10 MHz 80286.

The M27210 is part of a two product military megabit EPROM family. Another family member is the M27011. The 8 x 16K x 8 M27011 utilizes page addressing, and continued no-hardware-change upgrades to 32 M-bits in the same JEDEC-compatible 28-pin site.

The M27210 shares several features with standard JEDEC EPROMs, including two-line output control for simplified interfacing. It can be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 8 seconds.

The M27210 is manufactured using a scaled version of Intel's advanced HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

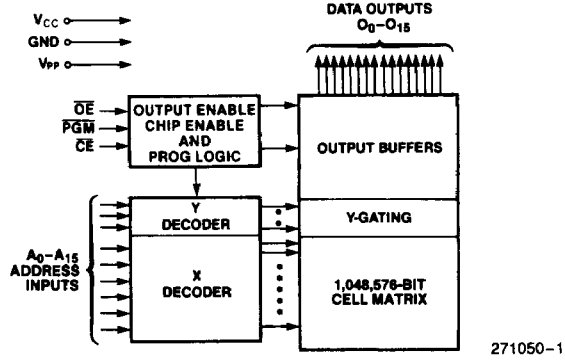
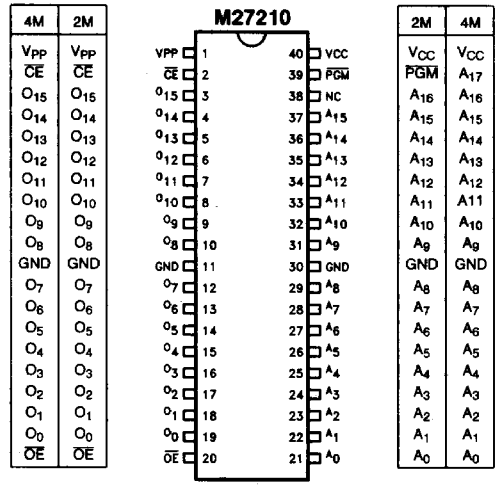


Figure 1. Block Diagram

January 1990
Order Number: 271050-004

Pin Names

A_0–A_{17}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_{15}	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO INTERNAL CONNECT
D.U.	DON'T USE



271050-2

NOTE: Compatible Higher Density Word Wide EPROM Pin Configurations are Shown in the Blocks Adjacent to the M27210 Pins

Figure 2. Cerdip Pin Configurations

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ABSOLUTE MAXIMUM RATINGS*

Case Operating Temperature
Under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +125°C

All Input or Output Voltages with
Respect to Ground ..... −0.6V to +6.25V

Voltage on A_9 with
Respect to Ground ..... −0.6V to +13.0V

V_{PP} Supply Voltage with Respect to
Ground During Programming .... −0.6V to +14V

V_{CC} Supply Voltage
with Respect to Ground ..... −0.6V to +7.0V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{OC}	Digital Supply Voltage	4.50	5.50	V

READ OPERATION

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Limits				Comments
		Min	Typ(3)	Max	Units	
I_{LI}	Input Load Current			1	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			1	μA	$V_{OUT} = 5.5V$
I_{PP1}(2)	V_{PP} Load Current Read			1	μA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby			60	mA	$\overline{CE} = V_{IH}$
I_{CC1}(2)	V_{CC} Current Active			200	mA	$\overline{CE} = OE = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

A.C. CHARACTERISTICS (Over Specified Operating Conditions)

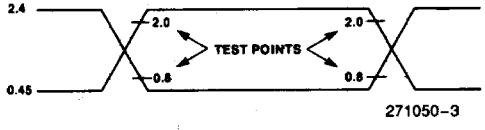
Versions	$V_{CC} \pm 10\%$	M27210-20		M27210-25		Unit
Symbol	Characteristics	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		80		100	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	60	0	60	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		ns

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The maximum current value is with Outputs O_0 to O_{15} unloaded.
3. Typical values are for T_C = 25°C and nominal supply voltages.
4. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE T_C = 25°C, f = 1MHz

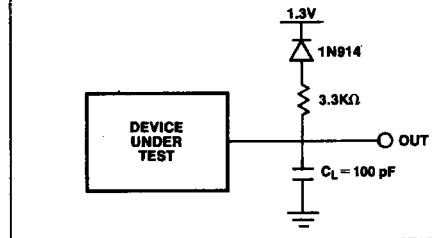
Symbol	Parameter	Typ(1)	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Input Capacitance		25	pF	V_{PP} = 0V

A.C. TESTING INPUT/OUTPUT WAVEFORM



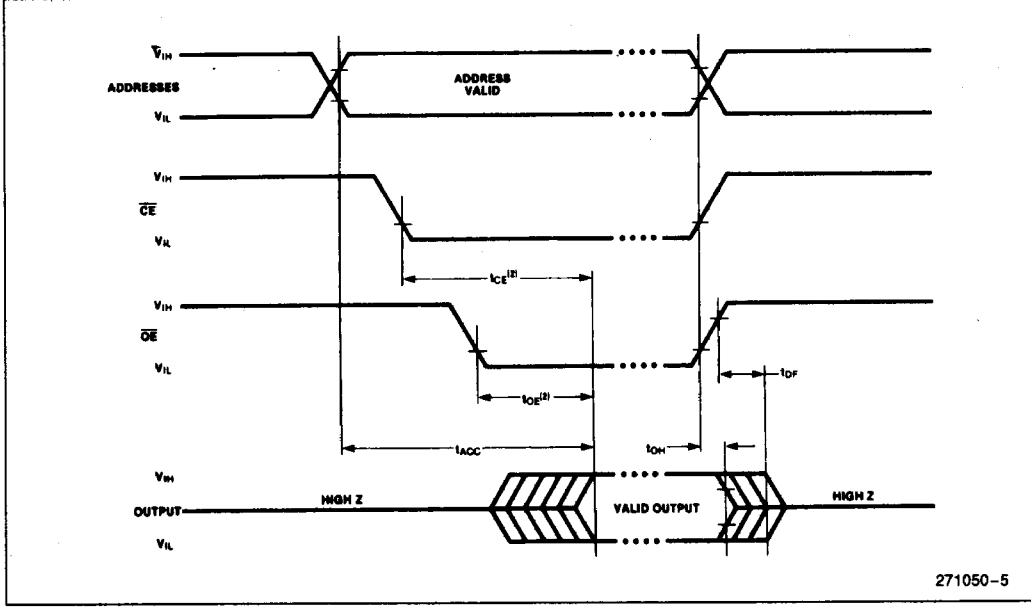
A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



NOTES:
1. Typical values are for T_C = 25°C and nominal supply voltages.
2. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the M27210 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

Table 1. Modes Selection

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	X	X(1)	X	X	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent	Manufacturer(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IL}	V_{CC}	5.0V	0089 H
Identifier	Device(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IH}	V_{CC}	5.0V	00FFH

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1–A_8, A_{10}–$A_{15} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The M27210 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming™ Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week @ 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

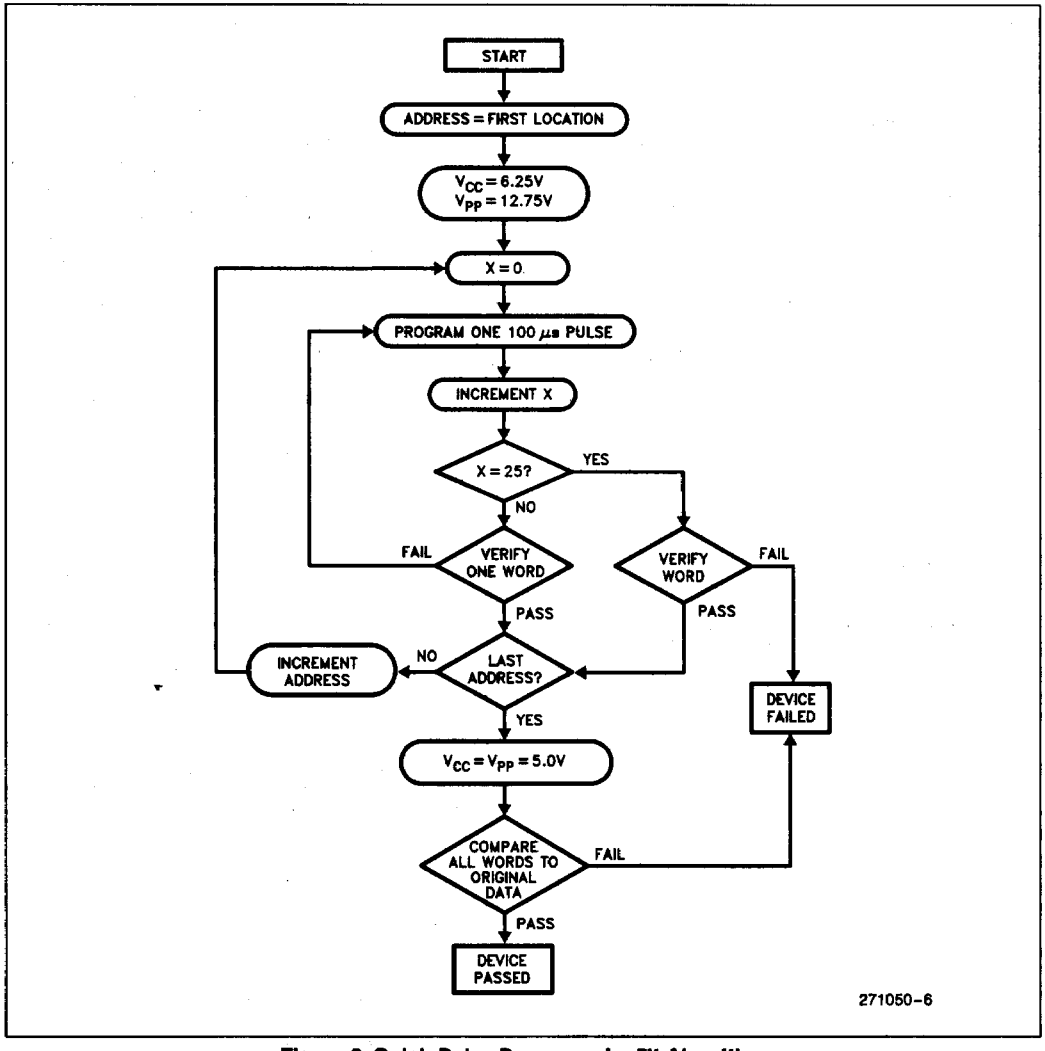


Figure 3. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's M27210 EPROMs can be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed in under eight seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a word verification to determine when the addressed word has been successfully programmed. Up to 25 100 µs pulses per word are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and word verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all data words should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS T_C = 25°C ±5°C

Table 2

Symbol	Parameter	Limits			Comments (Note 1)
		Min	Max	Unit	
I_{LI}	Input Leakage Current (All Inputs)		10	µA	V_{IN} = 6V
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}+1	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH} = −400 µA
I_{CC2}(3)	V_{CC} Supply Current (Program & Verify)		160	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

T_C = 25°C ±5°C (See Table 2 for V_{CC} and V_{PP} voltages.)

Symbol	Parameter	Limits				Comments (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{CES}	$\overline{CE}$ Setup Time	2			µs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	100	105	µs	Quick-Pulse Programming
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_{15} unloaded.

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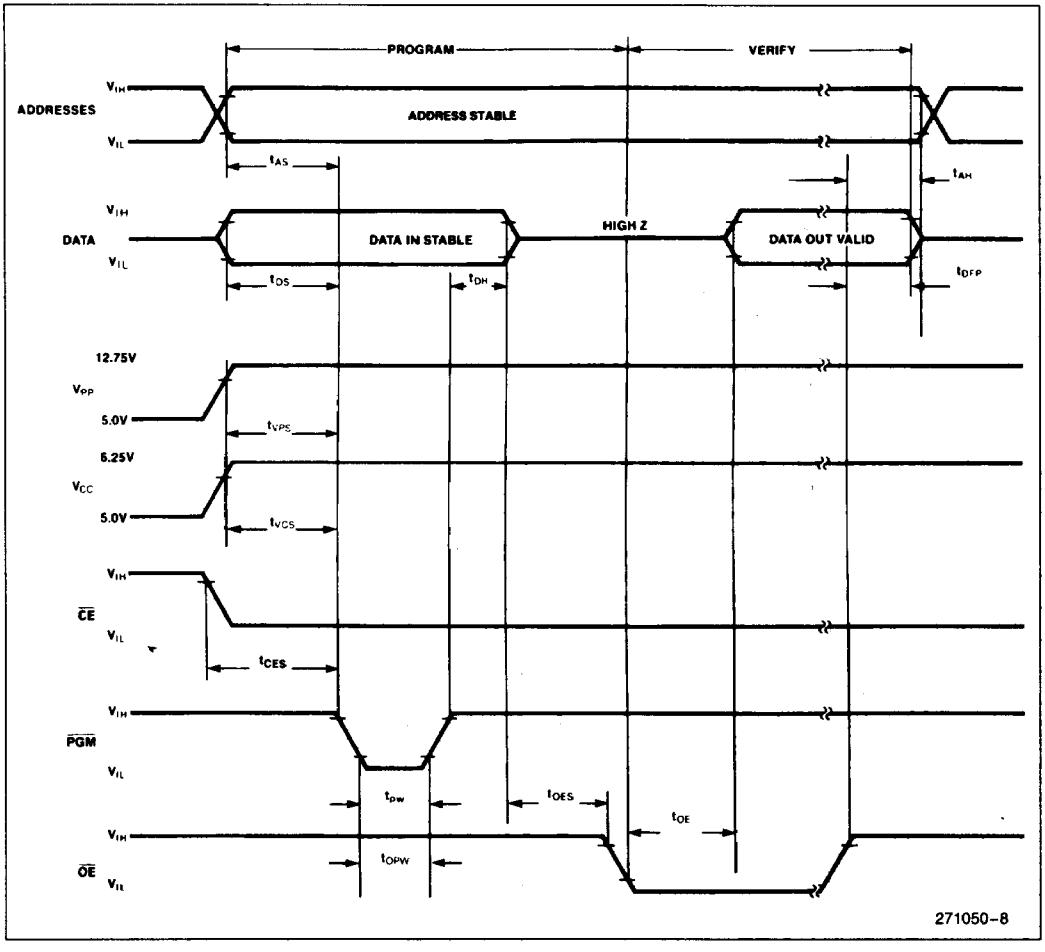
PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27210, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.