SONY

CXK581000ATM/AYM/AM/AP -55LL/70LL/10LL -55SL/70SL/10SL

131072-word × 8-bit High Speed CMOS Static RAM

For the availability of this product, please contact the sales office.

Description

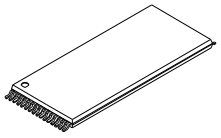
The CXK581000ATM/AYM/AM/AP is a high speed CMOS static RAM organized as 131072-words by 8 bits.

A polysilicon TFT cell technology realized extremely low stand- by current and higher data retention stability.

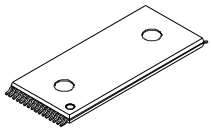
Special feature are low power consumption, high speed and broad package line-up.

The CXK581000ATM/AYM/AM/AP ia a suitable RAM for portable equipment with battery back up.

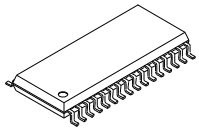
CXK581000ATM
32 pin TSOP (Plastic)



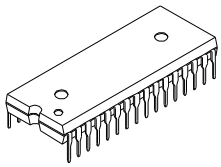
CXK581000AYM
32 pin TSOP (Plastic)



CXK581000AM
32 pin SOP (Plastic)



CXK581000AP
32 pin DIP (Plastic)



Features

- Fast access time:

CXK581000ATM/AYM/AM/AP	(Access time)
-55LL/55SL	55ns (Max.)
-70LL/70SL	70ns (Max.)
-10LL/10SL	100ns (Max.)

- Low standby current:

CXK581000ATM/AYM/AM/AP	
-55LL/70LL/10LL	20µA (Max.)
-55SL/70SL/10SL	12µA (Max.)

- Low data retention current

CXK581000ATM/AYM/AM/AP	
-55LL/70LL/10LL	12µA (Max.)
-55SL/70SL/10SL	4µA (Max.)

- Single +5V supply: +5V ±10%
- Low voltage data retention: 2.0V (Min.)
- Broad package line-up
- CXK581000ATM/AYM
  8mm × 20mm 32 pin TSOP package
- CXK581000AM 525mil 32 pin SOP package
- CXK581000AP 600mil 32 pin DIP package

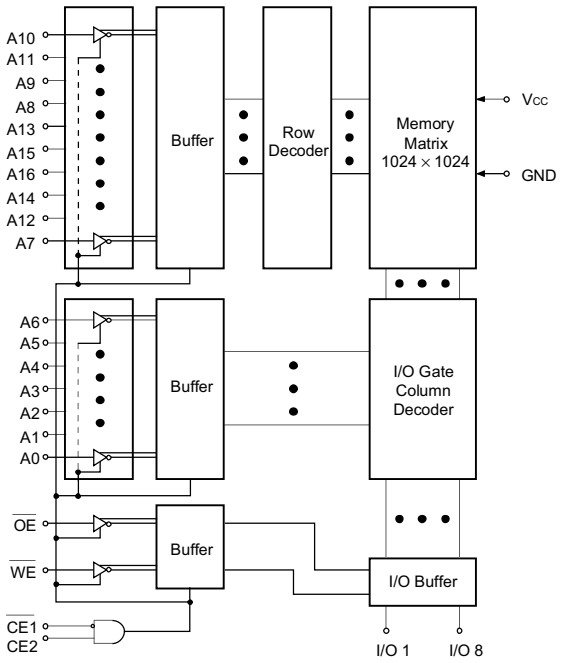
Functions

131072-word × 8-bit static RAM

Structure

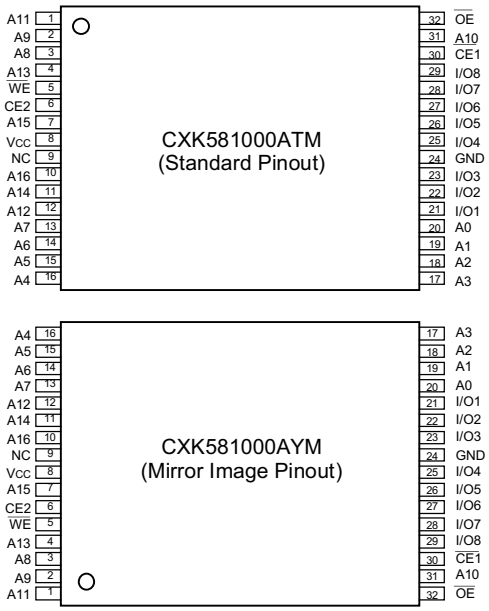
Silicon gate CMOS IC

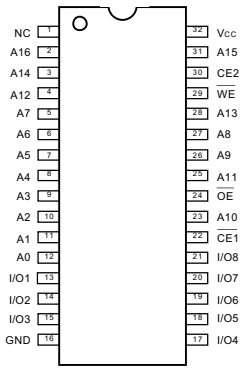
Block Diagram



E92756D53-PP

Pin Configuration (Top View)





CXK581000AM
CXK581000AP

Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		–0.5 to +7.0	V
Input voltage	V_{IN}		–0.5* to V_{CC} +0.5	
Input and output voltage	$V_{I/O}$		–0.5* to V_{CC} +0.5	
Allowable power dissipation	P_D	CXK581000AP	1.0	W
		CXK581000ATM/AYM/AM	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		–55 to +150	
Soldering temperature	Tsolder	CXK581000AP	260 • 10	°C • s
		CXK581000ATM/AYM/AM	235 • 10	

* V_{IN},$V_{I/O}$ = –3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	V_{CC} Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

×: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} +0.3	
Input low voltage	V_{IL}	–0.3*	—	0.8	

* V_{IL} = –3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC Characteristics (V_{CC} = 5V ±10%, GND = 0V, Ta = 0 to = +70°C)

Item	Symbol	Test conditions			Min.	Typ.*1	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}			–1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to V_{CC}			–1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IN} = V_{IH} or V_{IL} I_{OUT} = 0mA			—	7	15	mA
Average operating current	I_{CC2}	Min. cycle Duty = 100% I_{OUT} = 0mA	55LL/55SL		—	45	90	mA
			70LL/70SL		—	40	70	
			10LL/10SL		—	35	60	
	I_{CC3}	Cycle time 1µs duty = 100% I_{OUT} = 0mA $\overline{CE1}$ ≤ 0.2V CE2 ≥ V_{CC} – 0.2V V_{IL} ≤ 0.2V V_{IH} ≥ V_{CC} – 0.2V			—	10	20	
Standby current	I_{SB1}	CE2 ≤ 0.2V or { $\overline{CE1}$ ≥ V_{CC} – 0.2V, CE2 ≥ V_{CC} – 0.2V }	LL*2	0 to +70°C	—	—	20	µA
				0 to +40°C	—	—	4	
				+25°C	—	0.7	2	
			SL*3	0 to +70°C	—	—	12	
				0 to +40°C	—	—	2.4	
				+25°C	—	0.3	1	
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH} = –1.0mA			2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA			—	—	0.4	V

*1 V_{CC} = 5V, Ta = 25°C

*2 For -55LL/70LL/10LL

*3 For -55SL/70SL/10SL

I/O Capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	

Note) This parameter is sampled and is not 100% tested.

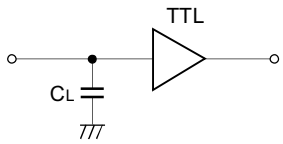
AC Characteristics

• **AC test conditions** (V_{CC} = 5V±10%, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
input rise time		tr = 5ns
input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	-55LL/55SL	C_L* = 30pF, 1TTL
	-70LL/70SL -10LL/10SL	C_L* = 100pF, 1TTL

* C_L includes scope and jig capacitances.

• **Test circuit**



• **Read cycle** ($\overline{WE}$ = "H")

Item	Symbol	-55LL/55SL		-70LL/70SL		-10LL/10SL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	55	—	70	—	100	—	ns
Address access time	t_{AA}	—	55	—	70	—	100	
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	55	—	70	—	100	
Chip enable access time (CE2)	t_{CO2}	—	55	—	70	—	100	
Output enable to output valid	t_{OE}	—	30	—	40	—	50	
Output hold from address change	t_{OH}	15	—	15	—	15	—	
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}, t_{HZ2}*	—	25	—	25	—	35	
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	25	—	25	—	35	

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

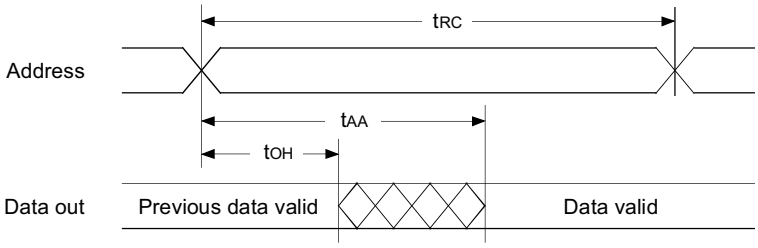
• **Write cycle**

Item	Symbol	-55LL/55SL		-70LL/70SL		-10LL/10SL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	55	—	70	—	100	—	ns
Address valid to end of write	t_{AW}	50	—	60	—	70	—	
Chip enable to end of write	t_{CW}	50	—	60	—	70	—	
Data to write time overlap	t_{DW}	25	—	30	—	40	—	
Data hold from write time	t_{DH}	0	—	0	—	0	—	
Write pulse width	t_{WP}	40	—	50	—	70	—	
Address setup time	t_{AS}	0	—	0	—	0	—	
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	
Output active from end of write	t_{OW}	10	—	10	—	10	—	
Write to output in high Z	t_{WHZ}*	—	25	—	25	—	30	

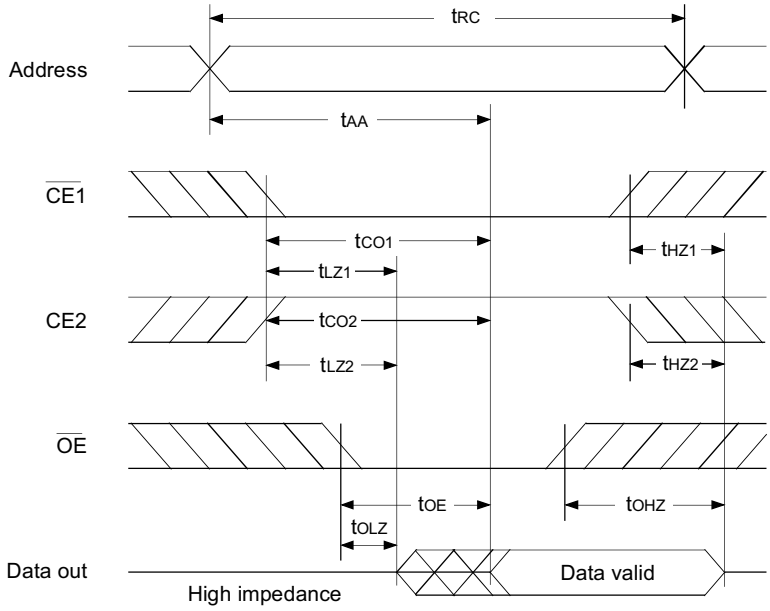
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

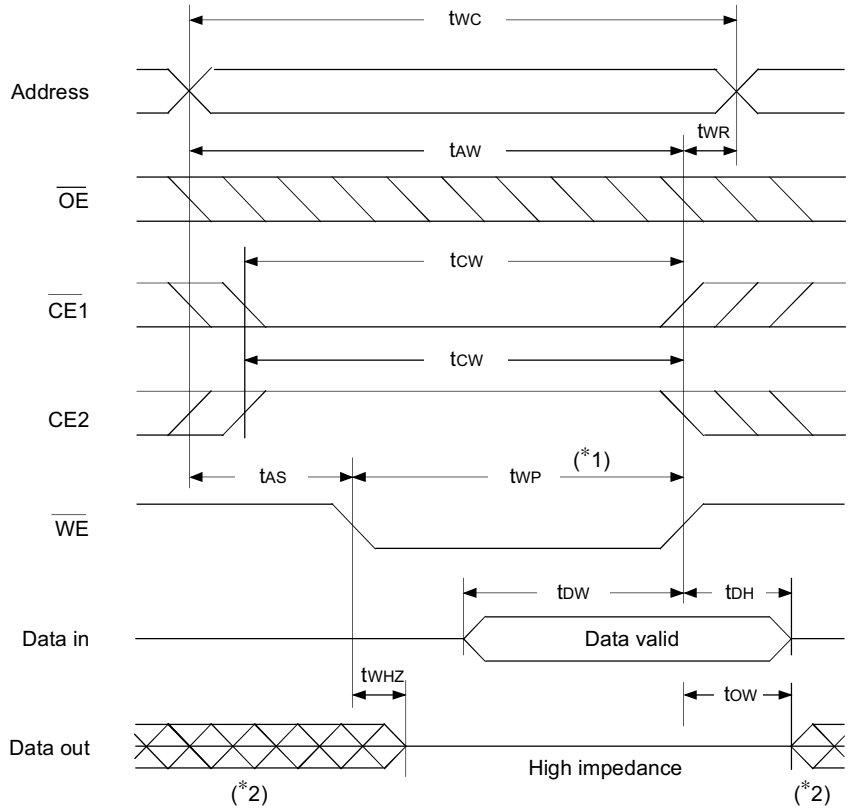
• **Read cycle (1) :** $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}, $\overline{WE}$ = V_{IH}



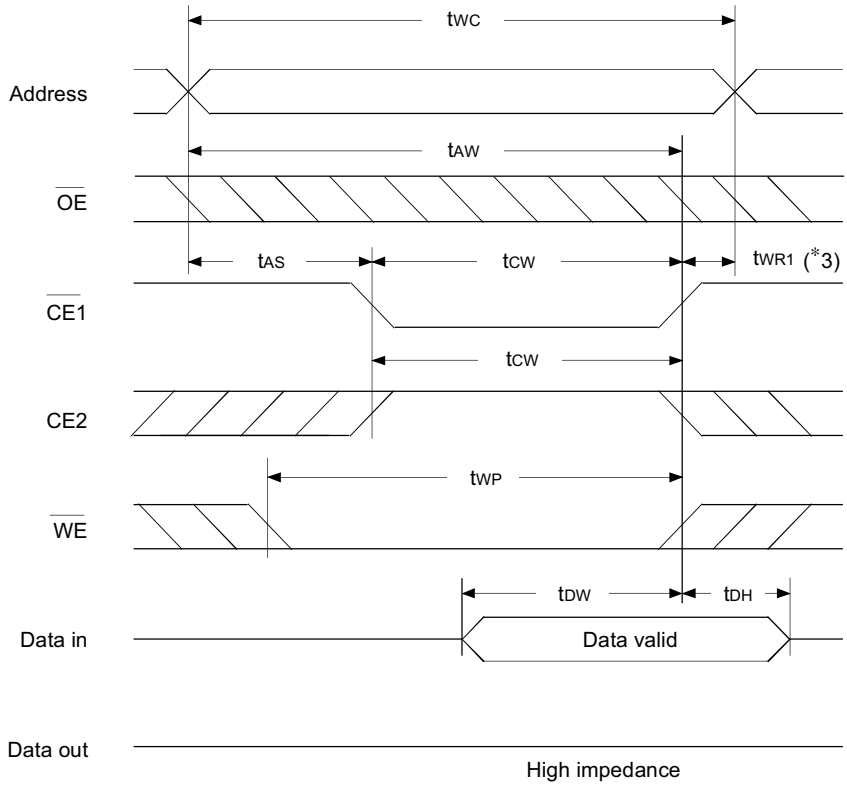
• **Read cycle (2) :** $\overline{WE}$ = V_{IH}



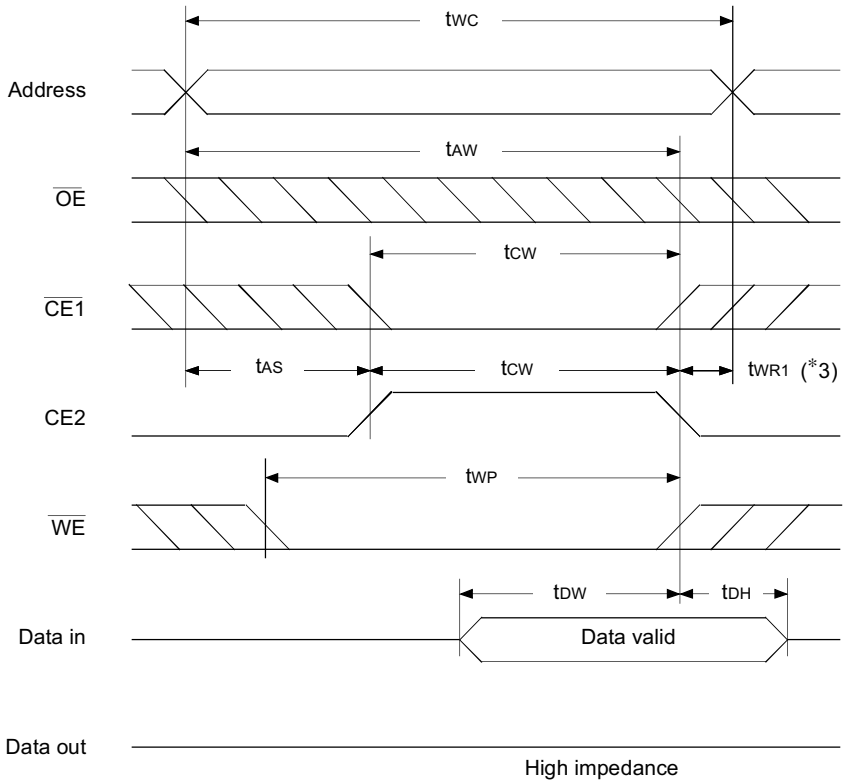
• **Write cycle (1) :** $\overline{WE}$ control



• **Write cycle (2) :** $\overline{CE1}$ control



• **Write cycle (3) :** CE2 control



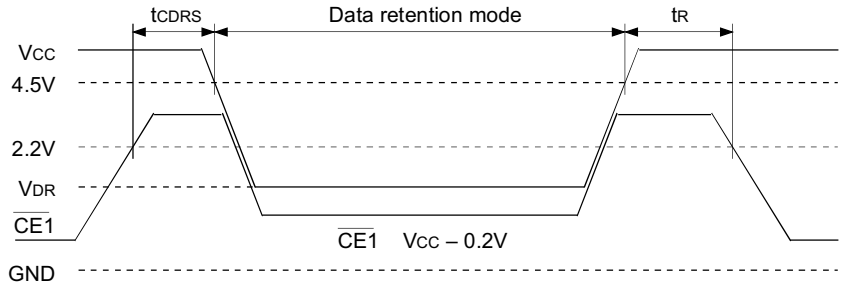
*1 Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

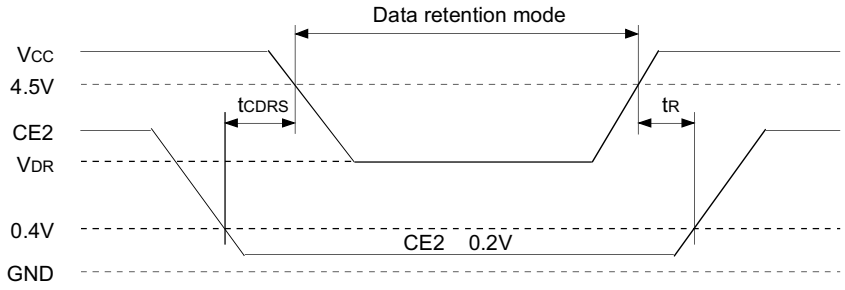
*3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Waveform

• Low supply voltage data retention waveform (1) : $\overline{CE1}$ control



• Low supply voltage data retention waveform (2) : CE2 control



Data Retention Characteristics (Ta = 0 to +70°C)

Item	Symbol	Test conditions			Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*1			2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V*1	LL*2	0 to +70°C	—	—	12	µA
				0 to +40°C	—	—	2.4	
				+25°C	—	0.4	1.2	
			SL*3	0 to +70°C	—	—	4	
				0 to +40°C	—	—	0.8	
				+25°C	—	0.15	0.3	
	I_{CCDR2}	V_{CC} = 2.0V to 5.5V*1	LL*2		—	0.7	20	
			SL*3		—	0.3	12	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode			0	—	—	ns
Recovery time	t_R				5	—	—	ms

Note)

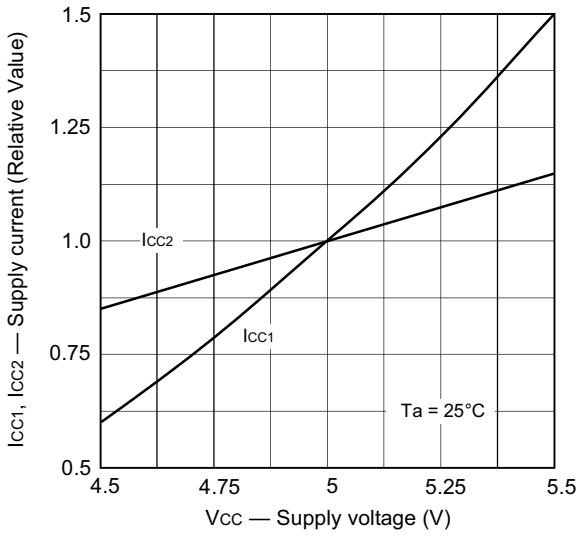
*1 $\overline{CE1} \geq V_{CC} - 0.2V$, CE2 ≥ V_{CC} – 0.2V [$\overline{CE1}$ Control] or CE2 ≤ 0.2V [CE2 Control]

*2 For -55LL/70LL/10LL

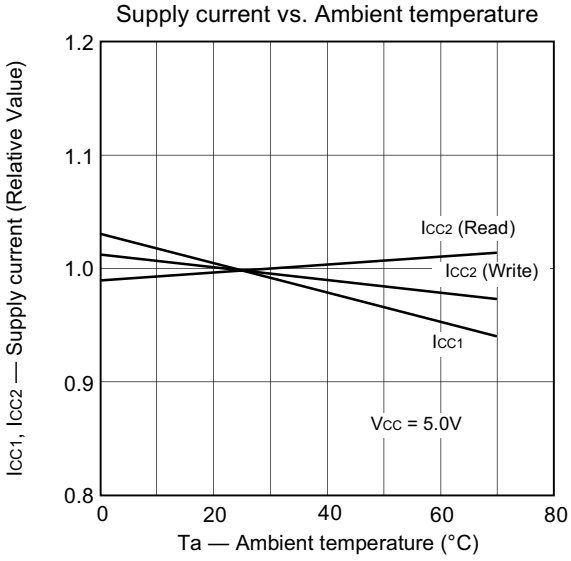
*3 For -55SL/70SL/10SL

Example of Representative Characteristics

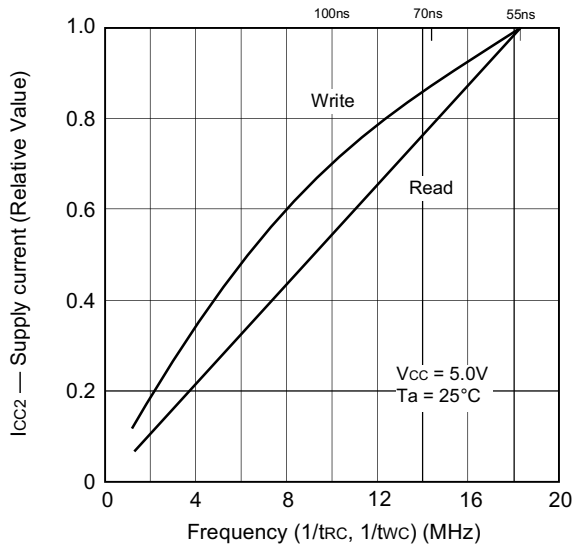
Supply current vs. Supply voltage



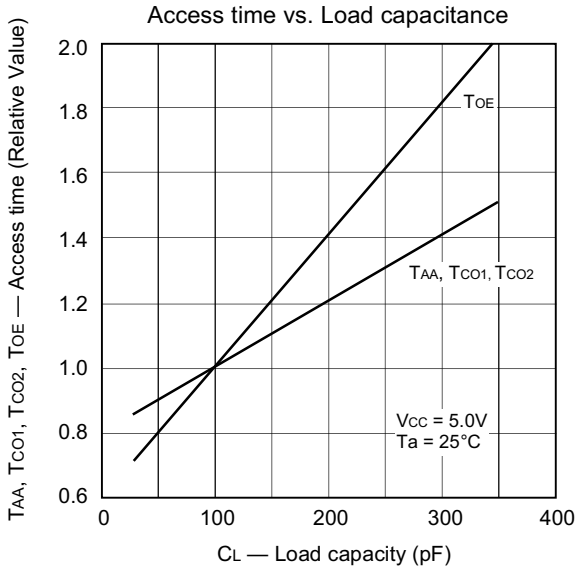
Supply current vs. Ambient temperature



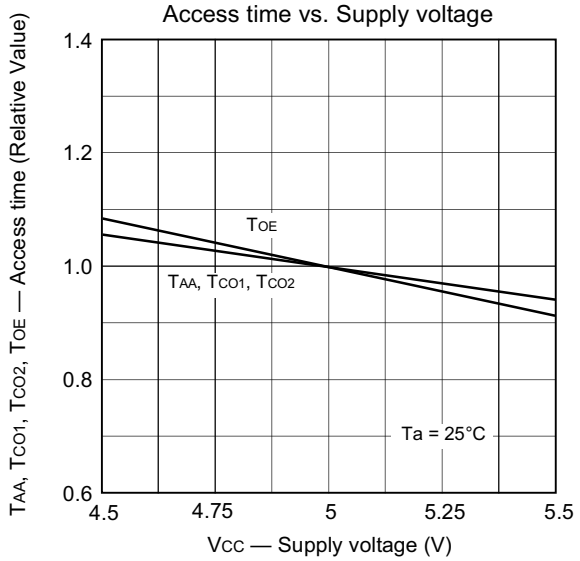
Supply current vs. Frequency



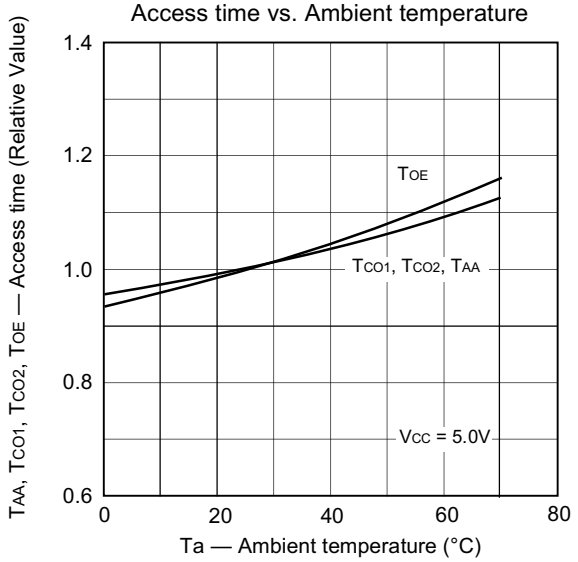
Access time vs. Load capacitance



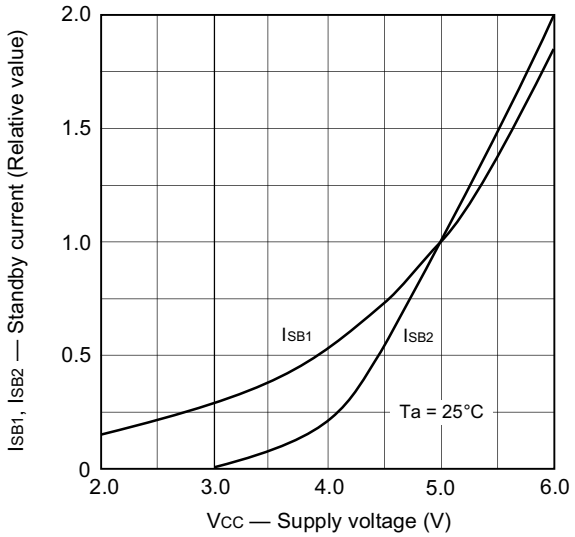
Access time vs. Supply voltage



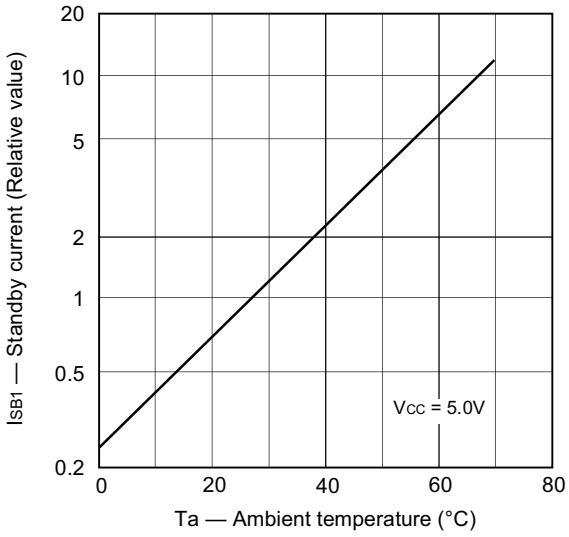
Access time vs. Ambient temperature



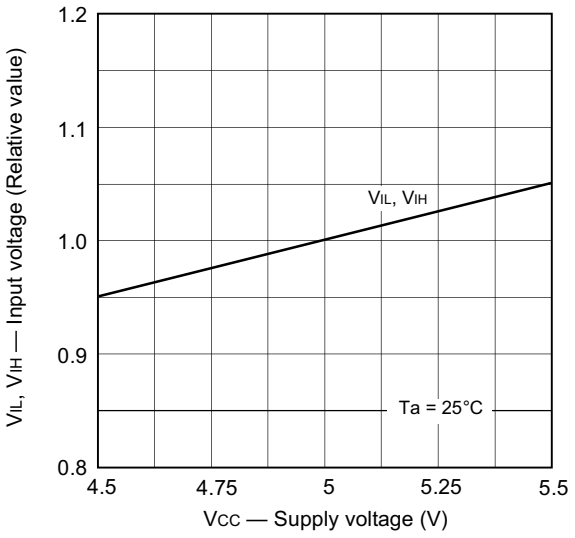
Standby current vs. Supply voltage



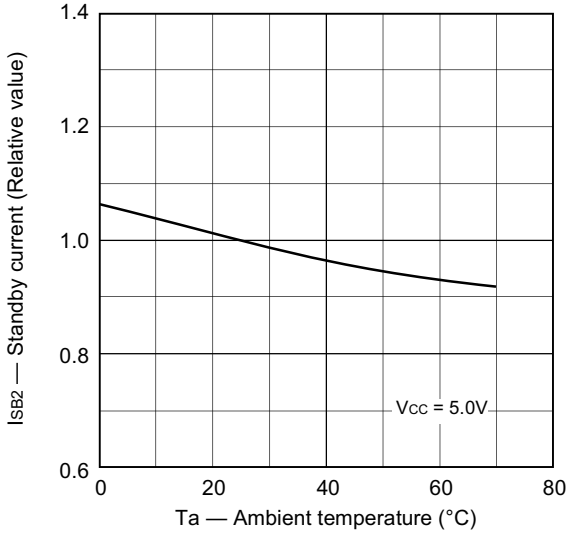
Standby current vs. Ambient temperature



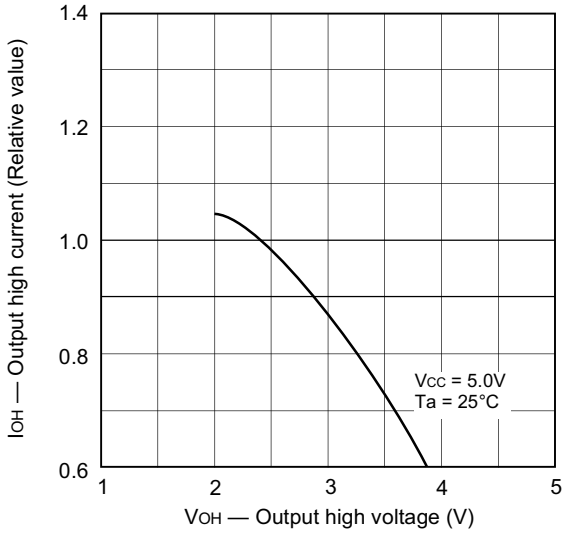
Input voltage level vs. Supply voltage



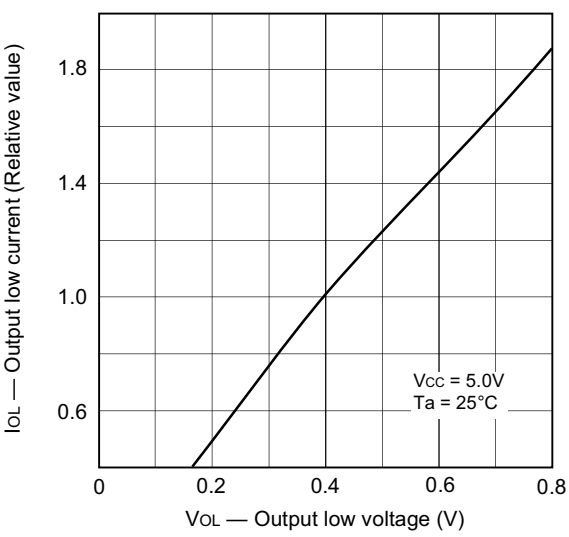
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



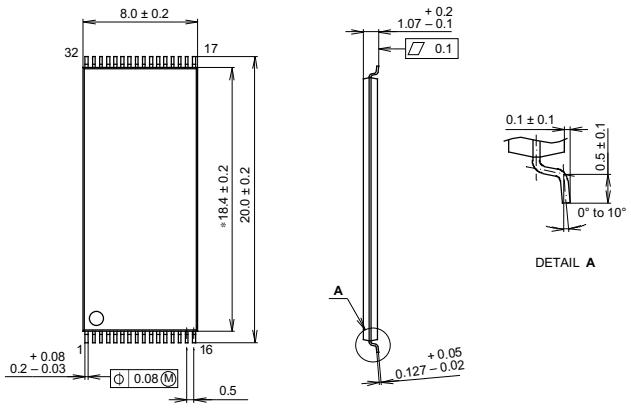
Output low current vs. Output low voltage



Package Outline Unit: mm

CXK581000ATM

32PIN TSOP (I) (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

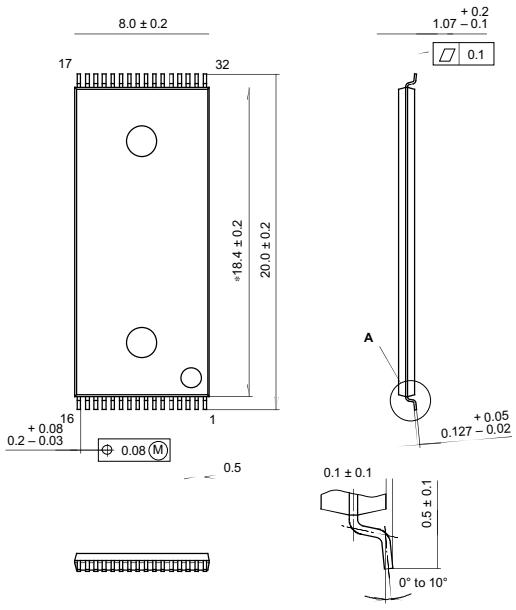
PACKAGE STRUCTURE

SONY CODE	TSOP (I) -32P-L01
EIAJ CODE	TSOP (I) 032-P-0820-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	

CXK581000AYM

32PIN TSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

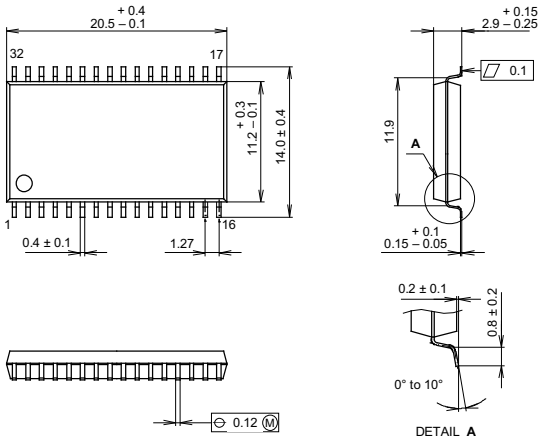
PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01R
EIAJ CODE	TSOP032-P-0820-B
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

CXK581000AM

32PIN SOP (PLASTIC) 525mil



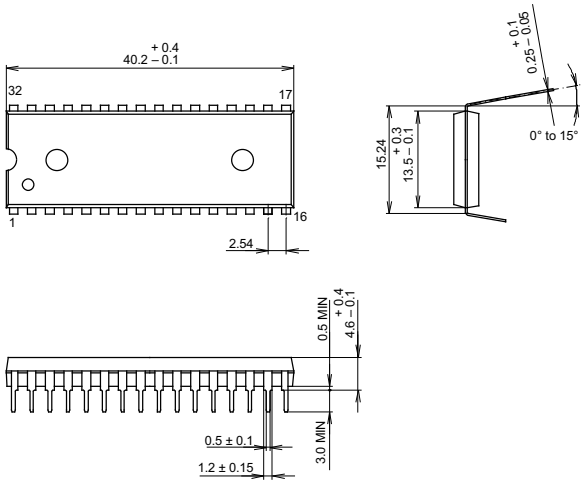
PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	*SOP032-P-0525-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————

CXK581000AP

32PIN DIP (PLASTIC) 600mil



PACKAGE STRUCTURE

SONY CODE	DIP-32P-01
EIAJ CODE	*DIP32-P-0600-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	4.5g