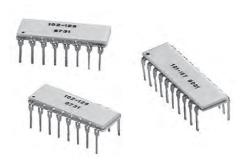


Ceramic Sandwich, Dual-In-Line Thin Film Resistor, Through Hole Network (Custom)



A dual-in-line monolithic ceramic package in a variety of sizes and configurations. A rugged, low cost packaging technique with 4 leads to 20 leads that allows higher resistance integration than chip and wire ceramic packages.

FEATURES

 Gold-to-gold terminations. External leads are attached directly to gold pads on the ceramic substrate by thermo-compression bonding (no internal solder)



RoHS*

HALOGEN

FREE

- Monolithc construction
- Ceramic package with no cavity. 4 pins to 20 pins.
- Flexibility of lead variations to save PC board space
- Compliant to RoHS Directive 2002/95/EC
- Halogen-free according to IEC 61249-2-21 definition

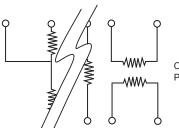
Note

* Pb containing terminations are not RoHS compliant, exemptions may apply

TYPICAL PERFORMANCE

	ABSOLUTE	TRACKING
TCR	10	2
	ABSOLUTE	RATIO
TOL.	0.1	0.02

SCHEMATIC



Custom schematics available. Please consult factory

TEST	SPECIFICATIONS		CONDITIONS
Material	Passivated nichrome	Tantalum nitride (1)	-
Pin/Lead Number	4 to 20		-
Resistance Range	100 Ω to	o 5 MΩ total	-
TCR: Absolute	± 10 ppm/°C	± 25 ppm/°C to ± 100 ppm/°C	- 55 °C to + 125 °C
TCR: Tracking	± 2 ppm/°C	± 5 ppm/°C	- 55 °C to + 125 °C
Tolerance: Absolute	± 0.1 % to ± 1.0 %		+ 25 °C
Tolerance: Ratio	± 0.01 % to ± 0.1 %		+ 25 °C
Power Rating: Resistor	100 mW (per element (typical))		Maximum at + 70 °C
Power Rating: Package	500 mW		Maximum at + 70 °C
Stability: Absolute	1000 ppm		2000 h at + 70 °C
Stability: Ratio	300 ppm		2000 h at + 70 °C
Voltage Coefficient	0.1 ppm/V		-
Working Voltage	100 V		-
Operating Temperature Range	- 55 °C to + 125 °C		-
Storage Temperature Range	- 55 °C to + 125 °C		-
Noise	< - 30 dB		-
Thermal EMF	< 0.1 μV/°C		-
Shelf Life Stability: Absolute	ΔR ± 0.01 %		1 year at + 25 °C
Shelf Life Stability: Ratio	$\Delta R \pm 0.002 \%$		1 year at + 25 °C

Note

(1) Tantalum nitride film is custom



DIMENSIONS AND IMPRINTING in inches and millimeters			
	DIMENSION	INCHES	MILLIMETERS
	Α	0.260 max.	6.61
	В	0.050	1.27
	С	0.160 typical	4.06
Part Number L	D	0.080	2.03
xxxx xx	Е	0.125	3.18
	F	0.125 min.	3.18
Pin 1 0 ,	G	0.01	0.254
Vishay Logo Date Code	Н	0.325	8.25
Vishay Logo Daté Code	I	0.100	2.54
→ ^B ←	J	0.020	0.51
	L (4 Pins)	0.220	5.59
	L (6 Pins)	0.320	8.13
	L (8 Pins)	0.420	10.67
→ G → ← → ←	L (10 Pins)	0.520	13.21
H Non-cumulative	L (12 Pins)	0.620	15.75
non-cumulative	L (14 Pins)	0.720	18.29
	L (16 Pins)	0.820	20.83
	L (18 Pins)	0.920	23.37
	L (20 Pins)	1.020	25.91

MECHANICAL SPECIFICATIONS		
Resistive Element	Passivated nichrome or tantalum nitride	
Substrate Material	Alumina	
Body	Ceramic	
Terminals	Copper alloy	
Plating	Gold	
Tin/Lead Option	Sn63	
Lead (Pb)-free Option	Sn96.5, Ag3.0, Cu0.5	
Tin/Lead and Lead (Pb)-free Finish	Hot solder dip	

Special requirements should be identified in advance, but as a minir	num, you should have the following information ready.
ELECTRICAL	MECHANICAL
Resistors, by value and tolerance Reference resistor(s) and matching of which resistors to which reference resistors Resistance by ratio Absolute temperature coefficient of resistivity Temperature tracking of subordinate resistors to reference resistor(s) Maximum operating voltage Resistor power ratings Operating temperature range	Maximum allowable seated height (from PC board to top of network) Special marking concerns Schematic pin out of package Specify if lead (Pb)-free

All standard products may be ordered directly from Vishay Dale Thin Film.





www.vishay.com

Vishay Dale Thin Film

GLOBAL PART NUMBER INFO	RMATION			
New Global Part Numbering: CSD1xx-xxx	UF			
C S D 1	1 x x - x x x x x x x x x x x x x x x x	X		
GLOBAL MODEL (2 or 3 digits)	CUSTOM PART NUMBER (7 or 9 digits)	PACKAGING		
CSD	1xx-xxx	UF = Tubed		
	or 1xx-xxx-x			
Historical Part Number example: 1xx-xxx (for reference purposes only)				
	1xx-xxx			
	CUSTOM PART NUMBER			





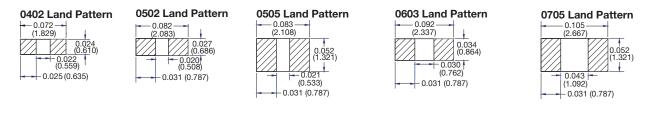
Vishay Dale Thin Film Land Patterns

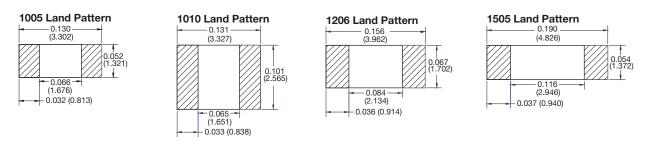
1. Scope

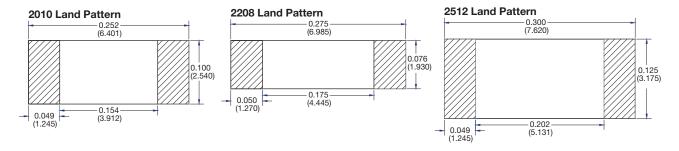
This technical note provides sample land patterns for Vishay Dale Thin Film SMT resistive products. The following drawings are based on IPC-SM-782 Surface Mount Design and Land Pattern Standard. These drawings are for reference only Vishay Thin Film recommends that the user contacts their PC board supplier for actual land patterns required. The pads are intended for lead (Pb)-free and tin / lead solder types.

2. Product Series

Thin Film Surface Mount Chip Resistors (L, P, PTN, PLT, PLTT, PAT, PATT, PNM, M/D55342 QPL Series)



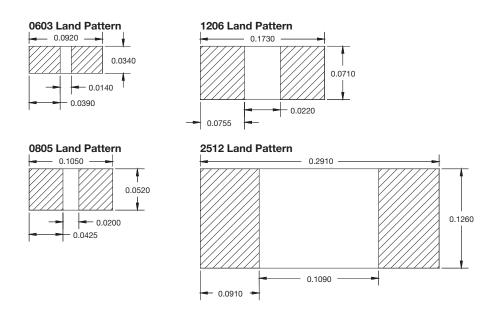




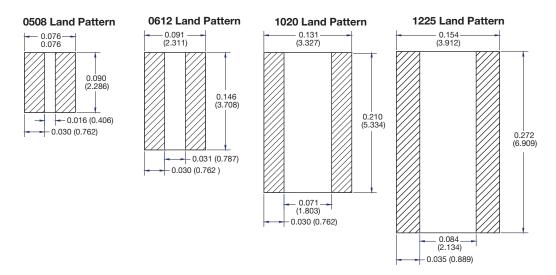




Thin Film Surface Mount Chip Resistors (PHP, PCAN Series)



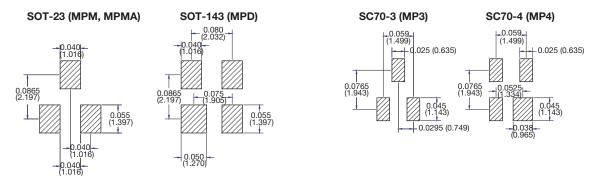
Thin Film Surface Mount Chip Resistors Long Axis Termination (L Series)



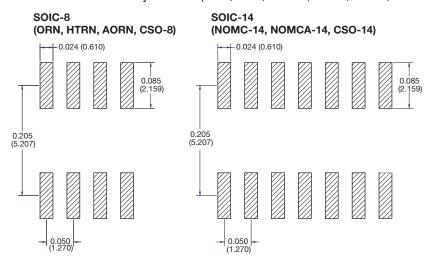


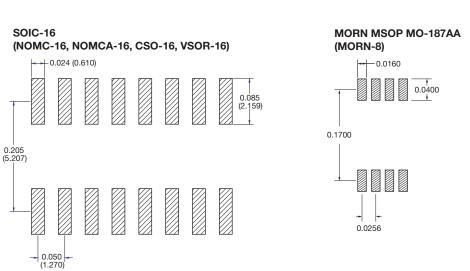


Surface Mount Networks (MPM, MPD, MP3, MP4 Series)



Surface Mount Networks SOIC Narrow Body 150 mils (ORN, CSO, MOMC, HTRN, AORN, MORN Series)



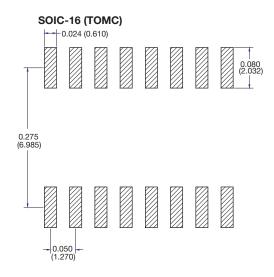


Land Patterns

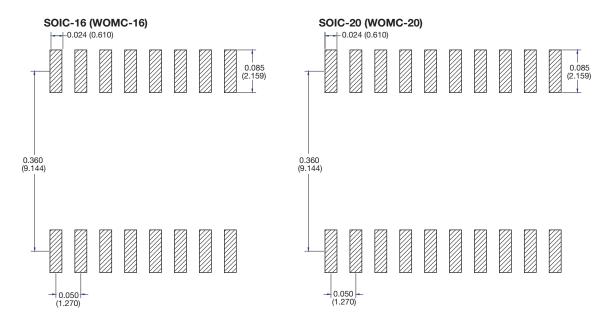


Vishay Dale Thin Film

Surface Mount Networks SOIC Medium Body 220 mils (TOMC Series)



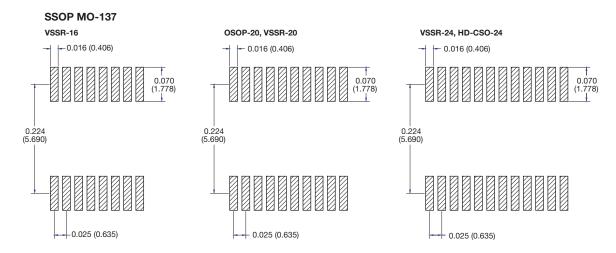
Surface Mount Networks SOIC Wide Body 300 mils (WOMC Series)

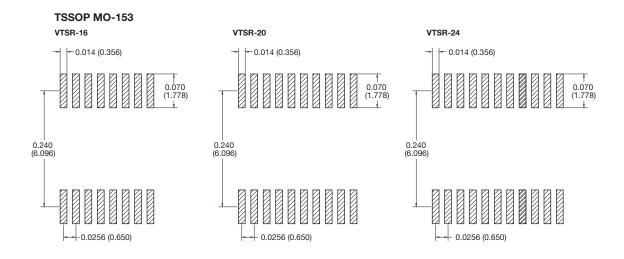






Surface Mount Networks High Density SSOP, TSOP (VSSR, VTSR Series)

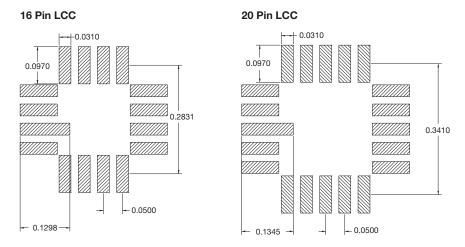




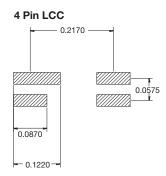




Surface Mount Leadless Networks (LCC Series)

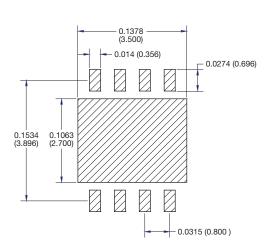


Surface Mount Leadless Networks (MPH Series)

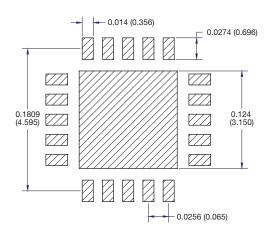


Surface Mount Leadless Packages DUAL/ QUAD Flat No Lead (DFN, QFN Series)

DFN MLP QFN MLP



DFN-8 4 x 5 mm Sq

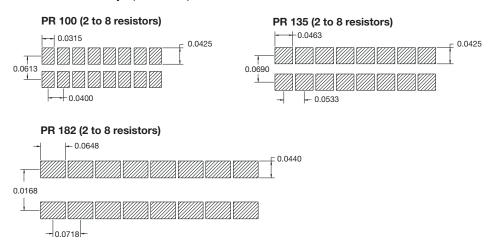


QFN-20 5 x 5 mm Sq





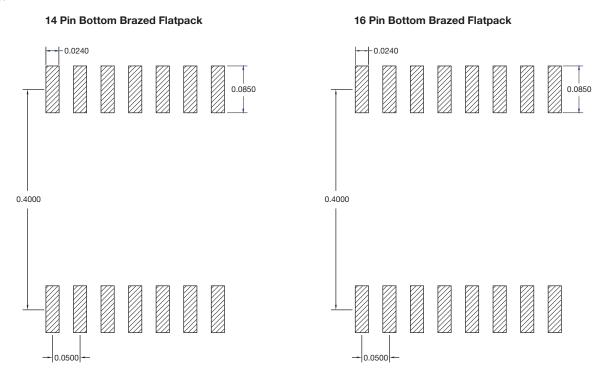
Surface Mount Leadless Resistor Arrays (PR Series)



Note

• All dimensions in inches (mm)

Flatpack





Legal Disclaimer Notice

Vishay

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