

CLC420

High-Speed, Voltage Feedback Op Amp

General Description

The CLC420 is an operational amplifier designed for applications requiring matched inputs, integration or transimpedance amplification. Utilizing voltage feedback architecture, the CLC420 offers a 300MHz bandwidth, a 1100V/ μ s slew rate and a 4mA supply current (power consumption of 40mW, \pm 5V supplies).

Applications such as differential amplifiers will benefit from 70dB common mode rejection ratio and an input offset current of 0.2 μ A. With its unity-gain stability, 2pA/ \sqrt Hz current noise and 3 μ A of input bias current, the CLC420 is designed to meet the needs of filter applications and log amplifiers. The low input offset current and current noise, combined with a settling time of 18ns to 0.01% make the CLC420 ideal for D/A converters, pin diode receivers and photo multiplier amplifiers. All applications will find 70dB power supply rejection ratio attractive.

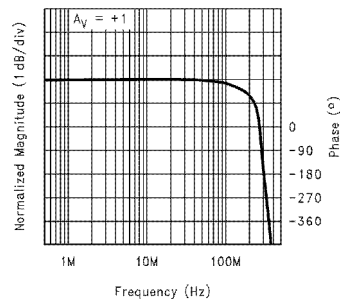
Features

- 300MHz small signal bandwidth
- 1100V/ μ s slew rate
- Unity-gain stability
- Low distortion, -60dBc at 20MHz
- 0.01% settling in 18ns
- 0.2 μ A input offset current
- 2pA/ \sqrt Hz current noise

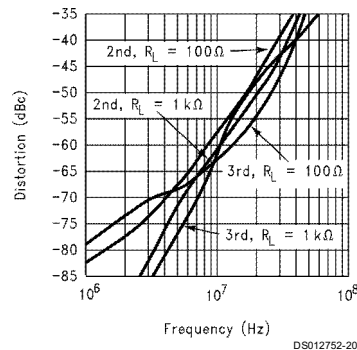
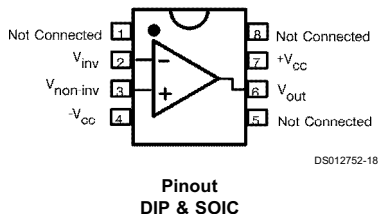
Applications

- Active filters/integrators
- Differential amplifiers
- Pin diode receivers
- Log amplifiers
- D/A converters
- Photo multiplier amplifiers

Non-Inverting Frequency Response



Connection Diagram



CLC420

Ordering Information

Package	Temperature Range Industrial	Packaging Marking	NSC Drawing
8-pin plastic DIP	-40°C to +85°C	CLC420AJP	N08E
8-pin plastic SOIC	-40°C to +85°C	CLC420AJE CLC420AJE-TR13	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) $\pm 7V$

I_{OUT}
(is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed 70mA, except A8D, B8D which should not exceed 35mA over the military temperature range)..

Common Mode Input Voltage	$\pm V_{CC}$
Differential Input Voltage	10V
Junction Temperature	+150°C
Operating Temperature Range AJ:	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Solder Duration (+300°C)	10 sec

Electrical Characteristics

$A_v = +1$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$, $R_f = 0\Omega$; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min (Note 2)			Units
Ambient Temperature		CLC420AJ	+25°C	-40°C	+25°C	+85°C	
Frequency Domain Response							
SSBW	-3dB bandwidth	$V_{OUT} < 0.4V_{PP}$	300	>200	>200	>130	MHz
LSBW		$V_{OUT} < 5V_{PP}$	40	>20	>25	>20	MHz
SSBWI	$A_v = -1$, $R_f = 500\Omega$	$V_{OUT} < 0.4V_{PP}$	100	>65	>65	>45	MHz
LSBWI	$A_v = -1$, $R_f = 500\Omega$	$V_{OUT} < 5V_{PP}$	60	>30	>35	>30	MHz
	gain flatness	$V_{OUT} < 0.4V_{PP}$					
GFPL	peaking	0.1MHz to 100MHz	0	<1	<0.6	<0.6	dB
GFPH	peaking	>100MHz	0	<5	<3	<3	dB
GFR	rolloff	0.1MHz to 100MHz	0.2	<1	<1	<2	dB
GFR1	rolloff, $A_v = -1$, $R_f = 500\Omega$	0.1MHz to 30MHz	0.2	<1.4	<1.4	<1.6	dB
LPD	linear phase deviation	0.1MHz to 100MHz	0.9	<1.8	<1.8	<2.5	°
Time Domain Response							
TRS	rise and fall time	0.4V step	1.2	<2	<2	<3	ns
TRL		5V step	1.4	<25	<20	<20	ns
TRSI	rise and fall time, $A_v = -1$, $R_f = 500\Omega$	0.4V step	3.5	<5.5	<5.5	<7.8	ns
TRLI		5V step	6	<10	<9.5	<10	ns
TSS	settling time to $\pm 0.1\%$	2V step	12	<18	<18	<18	ns
TSP	$\pm 0.01\%$	2V step	18	<25	<25	<25	ns
OS	overshoot	0.4V step	8	<35	<25	<25	%
SR	slew rate, $A_v = +2$	5V step	1100	>600	>750	>600	V/ μ s
SRI	slew rate, $A_v = -1$, $R_f = 500\Omega$	5V step	750	>430	>500	>430	V/ μ s
Distortion And Noise Response							
HD2	2nd harmonic distortion	$2V_{PP}$, 20MHz	-50	<-40	<-40	<-40	dBc
HD3	3rd harmonic distortion	$2V_{PP}$, 20MHz	-53	<-45	<-45	<-40	dBc
HD2	2nd harmonic distortion	$A_v = -1$ $2V_{PP}$, 20MHz, $R_f = 500$	-51	<-40	<-40	<-40	dBc
HD3	3rd harmonic distortion	$A_v = -1$, $R_f = 500\Omega$ $2V_{PP}$, 20MHz, $R_f = 500$	-51	<-40	<-40	<-35	dBc
	input referred noise						
VN	voltage	1MHz to 200MHz	4.2	<5.3	<5.3	<6	nV/ \sqrt{Hz}

Electrical Characteristics (Continued)
 $A_v = +1$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$, $R_f = 0\Omega$; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min (Note 2)			Units
Distortion And Noise Response							
ICN	current	1MHz to 200MHz	2	<2.9	<2.6	<2.3	pA/ $\sqrt{\text{Hz}}$
Static DC Performance							
VIO	input offset voltage (Note 3)		1	<3.2	<2	<3.5	mV
DVIO	average temperature coefficient		8	<15	-	<15	$\mu\text{V}/^\circ\text{C}$
IB	input bias current (Note 3)		3	<20	<10	<10	μA
DIB	average temperature coefficient		45	<120	-	<60	$\text{A}/^\circ\text{C}$
IIO	input offset current (Note 3)		0.2	<2.6	<1	<2	μA
DIIO	average temperature coefficient		2	<20	-	<10	$\text{nA}/^\circ\text{C}$
AOL	open loop gain (Note 3)		65	>52	>56	>56	μA
PSRR	power supply rejection ratio		70	>55	>60	>60	dB
CMRR	common mode rejection ratio		80	>60	>65	>65	dB
ICC	supply current (Note 3)	no load, quiescent	4	<5	<5	<5	mA
Miscellaneous Performance							
RIND	differential mode input	resistance	2	>0.5	>1	>1	$\text{M}\Omega$
CIND		capacitance	1	<2	<2	<2	pF
RINC	common mode input	resistance	1	>0.25	>0.5	>0.5	$\text{M}\Omega$
CINC		capacitance	1	<2	<2	<2	pF
RO	output impedance	at DC	0.02	<0.3	<0.2	<0.2	Ω
VO	output voltage range	no load	± 3.6	± 2.8	± 3	± 3	V
VOL	output voltage range	$R_L = 100\Omega$	± 2.9	± 2.5	± 2.5	± 2.5	V
CMIR	common mode input range	for rated performance	± 3.2	± 2.5	± 2.8	± 2.8	V
IO	output current		± 60	± 30	± 50	± 50	mA
Package Thermal Resistance							
junction to case	CLC420AJP	65°	-	-	-	-	C/W
junction to ambient	CLC420AJP	120°	-	-	-	-	C/W
junction to case	CLC420AJE	60°	-	-	-	-	C/W
junction to ambient	CLC420AJE	140°	-	-	-	-	C/W

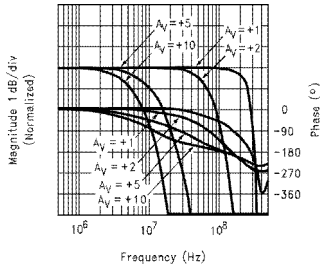
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

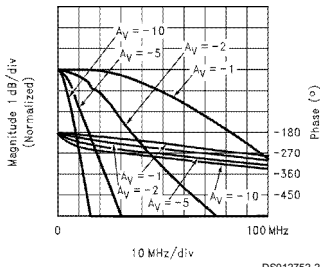
Note 3: AJ-level: spec. is 100% tested at +25°C.

Typical Performance Characteristics

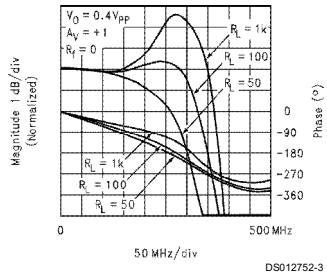
Non-Inverting Frequency Response



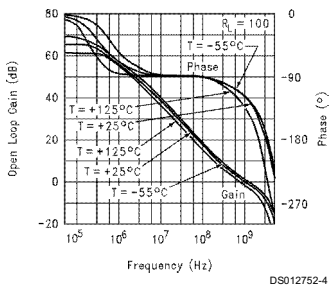
Inverting Frequency Response



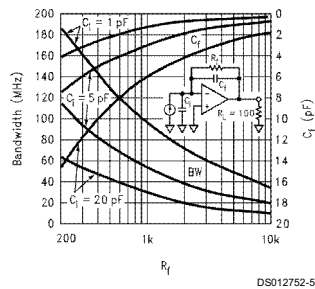
Frequency Response for Various R_L S



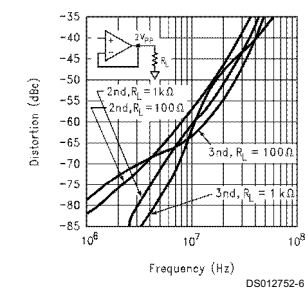
Open Loop Gain and Phase



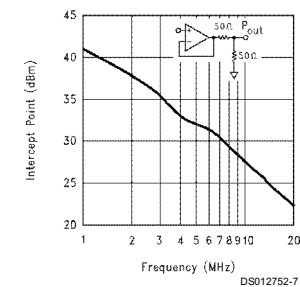
Bandwidth vs. Gain, Transimpedance Configuration



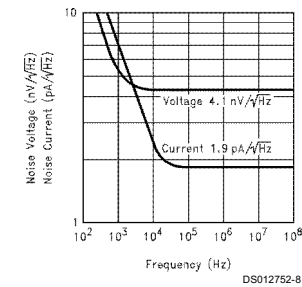
2nd and 3rd Harmonic Distortion



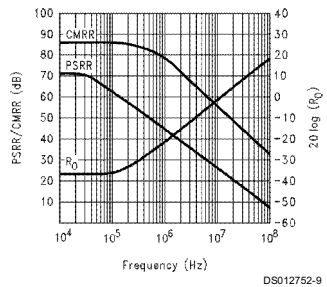
2-Tone, 3rd Order Intermodulation Intercept



Equivalent Input Noise

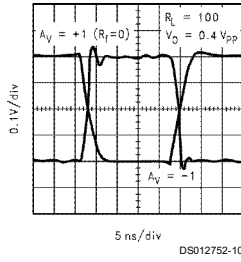


PSRR, CMRR, and Closed Loop R_O

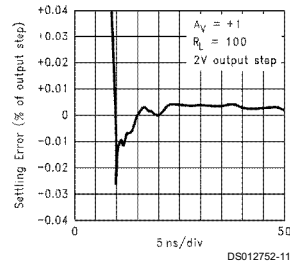


Typical Performance Characteristics (Continued)

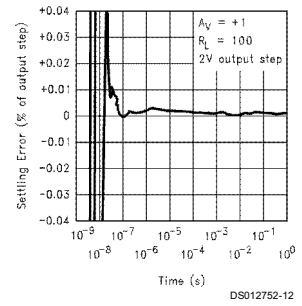
Pulse Response



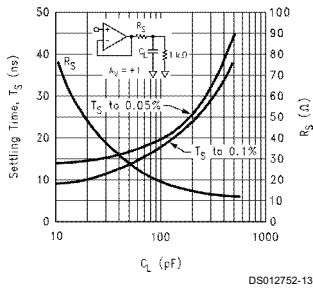
Settling Time



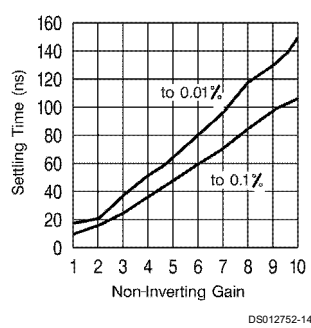
Long-Term Settling Time



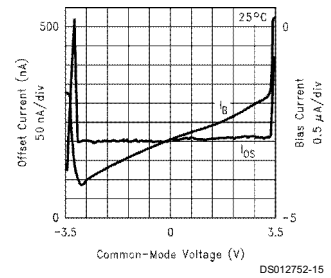
Settling Time vs. Capacitive Load



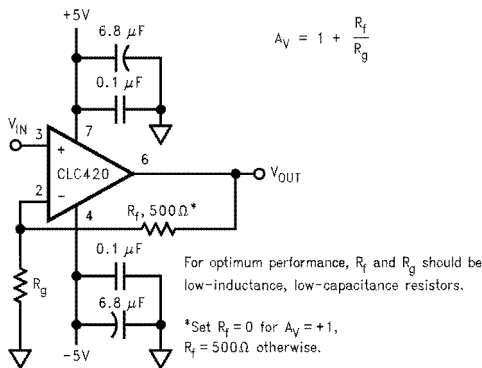
Settling Time vs. Gain



\$I_B\$ and \$I_{OS}\$ vs. Common-Mode Voltage

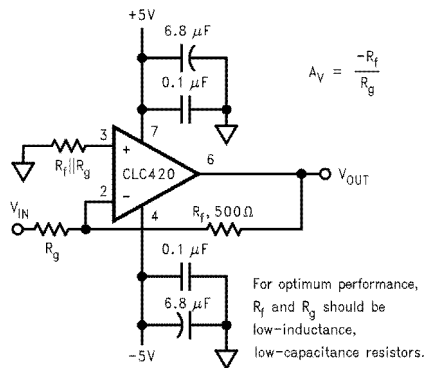


Application Division



DS012752-16

FIGURE 1. Recommended Non-Inverting Gain Circuit



DS012752-17

FIGURE 2. Recommended Inverting Gain Circuit

Description

The CLC420 is a high-speed, slew-booster, voltage feedback amplifier with unity-gain stability. These features along with matched inputs, low input bias and noise currents, and excellent CMRR render the CLC420 very attractive for active filters, differential amplifiers, log amplifiers, and transimpedance amplifiers.

DC accuracy

Unlike current-feedback amplifiers, voltage-feedback amplifiers have matched inputs. This means that the non-inverting and inverting input bias current are well matched and track over temperature, etc. As a result, by matching the resistance looking out of the two inputs, these errors can be reduced to a small offset current term.

Gain bandwidth product

Since the CLC420 is a voltage-feedback op-amp, closed-loop bandwidth is approximately equal to the gain-bandwidth product (typically 100MHz) divided by the noise gain of the circuit (for noise gains greater than 5). At lower noise gains, higher-order amplifier poles contribute to higher closed-loop bandwidth. At low gains use the frequency response performance plots given in the data sheet.

Another point to remember is that the closed-loop bandwidth is determined by the noise gain, not the signal gain of the circuit. Noise gain is the reciprocal of the attenuation in the feedback network enclosing the op amp. For example, a CLC420 setup as a non-inverting amplifier with a closed-loop gain of +1 (a noise gain of 1) has a 300MHz bandwidth. When used as an inverting amplifier with a gain of -1 (a noise gain of 2), the bandwidth is less, typically only 100MHz.

Full-power bandwidth, and slew-rate

The CLC420 combines exceptional full-power bandwidths (40MHz, $V_o=5V_{pp}$, $A_v=+1$) and slew rates (1100V/ μ s, $A_v=+1$) with low (40mW) power consumption. These attractive results are achieved by using slew-boosting circuitry to keep the slew rates high while consuming very little power.

In non-slew boosted amplifiers, full-power bandwidth can be easily determined from slew-rate measurements, but in slew-boosting amplifiers, such as the CLC420, you can't. For this reason we provide data for both.

Slew rate is also different for inverting and non-inverting configurations. This occurs because common-mode signal voltages are present in non-inverting circuits but absent in inverting circuits. Once again data is provided for both.

Application Division (Continued)

Transimpedance amplifier circuits

Low inverting, input current noise ($2pA/\sqrt{Hz}$) makes the CLC420 ideal for high-sensitivity transimpedance amplifier circuits for applications such as pin-diode optical receivers, and detectors in receiver IFs. However, feedback resistors $4k\Omega$ or greater are required if feedback resistor noise current is going to be less than the input current noise contribution of the op-amp.

With feedback resistors this large, shunt capacitance on the inverting input of the op-amp (from the pin-diode, etc.) will unacceptably degrade phase margin causing frequency response peaking or oscillations a small valued capacitor shunting the feedback resistor solves this problem (Note: This approach does not work for a current-feedback op-amp configured for transimpedance applications). To determine the value of this capacitor, refer to the "Transimpedance BW vs. R_f and C_i " plot.

For example, let's assume an optical transimpedance receiver is being developed. Total capacitance from the inverting input to ground, including the photodiode and strays is $5pF$. A $5k\Omega$ feedback resistor value has been determined to provide best dynamic range based on the response of the photodiode and the range of incident optical powers, etc.

From the "Transimpedance BW vs. R_f and C_i " plot, using $C_i=5pF$ it is determined from the two curves labeled $C_i=5pF$, that $C_f=1.5pF$ provides optimal compensation (no more than $0.5dB$ frequency response peaking) and a $-3dB$ bandwidth of approximately $27MHz$.

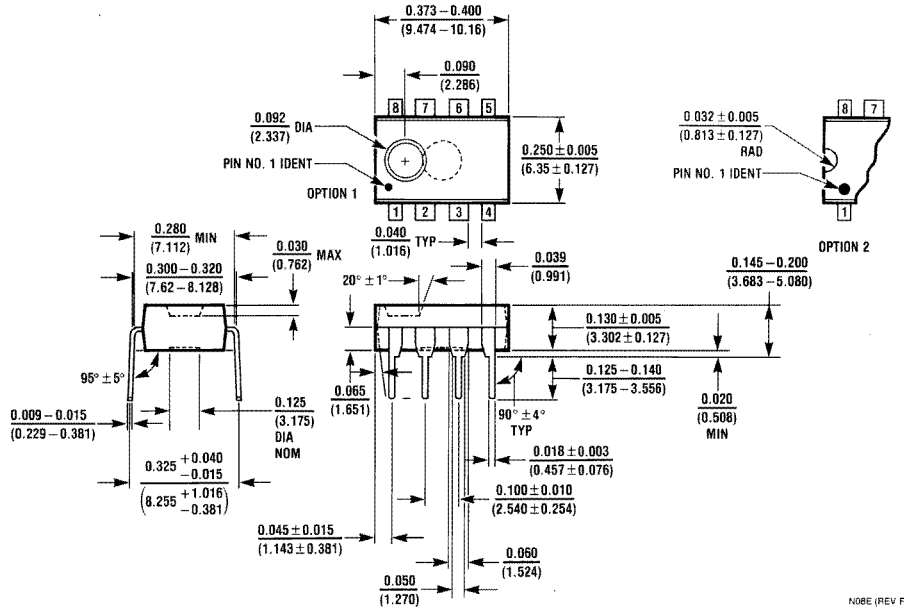
Printed circuit layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the output and inverting input: Node connections should be small with minimal coupling to the ground plane.

Parasitic or load capacitance directly on the output (pin 6) will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before this capacitance, if present, effectively decouples this effect. The graphs on the preceding page, "Settling Time vs. C_L ", illustrates the required resistor value and resulting performance vs. capacitance.

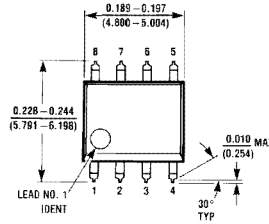
Evaluation PC boards (part no. 730013 for through-hole and CLC730027 for SOIC) are available for the CLC420.

Physical Dimensions inches (millimeters) unless otherwise noted



N08E - CLC420AJP

NOBE (REV F)



M08A - CLC420AJE or CLC420AJE-TR13


MOBA (REV H)

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 <p>National Semiconductor Corporation Americas Tel: 1-800-272-9959 Fax: 1-800-737-7018 Email: support@nsc.com</p> <p>www.national.com</p>	<p>National Semiconductor Europe Fax: +49 (0) 1 80-530 85 86 Email: europe.support@nsc.com Deutsch Tel: +49 (0) 1 80-530 85 85 English Tel: +49 (0) 1 80-532 78 32 Français Tel: +49 (0) 1 80-532 93 58 Italiano Tel: +49 (0) 1 80-534 16 80</p>	<p>National Semiconductor Asia Pacific Customer Response Group Tel: 65-2544466 Fax: 65-2504466 Email: sea.support@nsc.com</p>	<p>National Semiconductor Japan Ltd. Tel: 81-3-5639-7560 Fax: 81-3-5639-7507</p>
--	---	--	---

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.