

CDCV304 200-MHz General-Purpose Clock Buffer, PCI-X Compliant

1 Features

- General-Purpose and PCI-X 1:4 Clock Buffer
- Operating Frequency
 - 0 MHz to 200 MHz General-Purpose
- Low Output Skew: <100 ps
- Distributes One Clock Input to One Bank of Four Outputs
- Output Enable Control that Drives Outputs Low when OE is Low
- Operates from Single 3.3-V Supply or 2.5-V Supply
- PCI-X Compliant
- 8-Pin TSSOP Package

2 Description

The CDCV304 is a high-performance, low-skew, general-purpose PCI-X compliant clock buffer. It distributes one input clock signal (CLKIN) to the output clocks (1Y[0:3]). It is specifically designed for use with PCI-X applications. The CDCV304 operates at 3.3 V and 2.5 V and is therefore compliant to the 3.3-V PCI-X specifications.

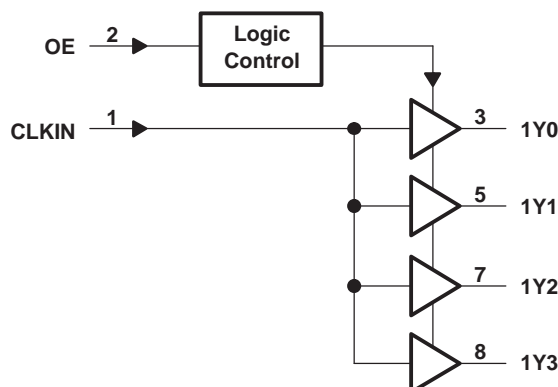
The CDCV304 is characterized for operation from –40°C to 85°C for automotive and industrial applications.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| CDCV304 | TSSOP (8) | 3.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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3 Revision History

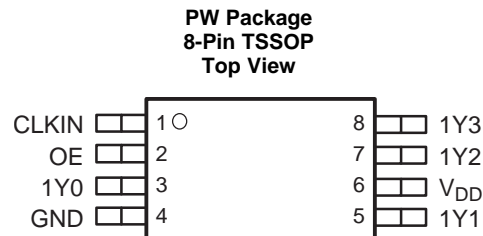
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision H (February 2011) to Revision I | Page |
|---|-------------|
| • Changed datasheet layout | 1 |
| • Added Junction temperature, $T_{j, \max} 125\text{ }^{\circ}\text{C}$ | 3 |

| Changes from Revision G (January 2011) to Revision H | Page |
|---|-------------|
| • Added missing characteristics graphs | 6 |

| Changes from Revision F (April 2009) to Revision G | Page |
|---|-------------|
| • Added ψ_{JT} and ψ_{JB} specs to the Thermal Information Table and changed $R_{\theta JB}$ and $R_{\theta JC}$ specs from 65 and 69 $^{\circ}\text{C/W}$ respectively | 4 |

4 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------|------------|-------|---------------------------|
| NAME | NO. | | |
| 1Y[0:3] | 3, 5, 7, 8 | O | Buffered output clocks |
| CLKIN | 1 | I | Input reference frequency |
| GND | 4 | Power | Ground |
| OE | 2 | I | Output enable control |
| V _{DD} | 6 | Power | Supply |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | MIN | MAX | UNIT |
|---|------|-----------------------|------|
| Supply voltage range, V _{DD} | -0.5 | 4.3 | V |
| Input voltage range, V _I ^{(2) (3)} | -0.5 | V _{DD} + 0.5 | V |
| Output voltage range, V _O ^{(2) (3)} | -0.5 | V _{DD} + 0.5 | V |
| Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}) | -50 | 50 | mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}) | -50 | 50 | mA |
| Continuous total output current, I _O (V _O = 0 to V _{DD}) | -50 | 50 | mA |
| Package thermal impedance, θ_{JA} : PW package | | 230.5 | °C/W |
| Junction temperature, T _{j, max} | | 125 | °C |
| Storage temperature range T _{stg} | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This value is limited to 4.6 V maximum.

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5.2 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------------------------|--------------------------|---------------------|-----|---------------------|------|
| Supply voltage, V_{DD} | | 2.3 | | 3.6 | V |
| Low-level input voltage, V_{IL} | | | | $0.3 \times V_{DD}$ | V |
| High-level input voltage, V_{IH} | | $0.7 \times V_{DD}$ | | | V |
| Input voltage, V_I | | 0 | | V_{DD} | V |
| High-level output current, I_{OH} | $V_{DD} = 2.5 \text{ V}$ | | | -12 | mA |
| | $V_{DD} = 3.3 \text{ V}$ | | | -24 | |
| Low-level output current, I_{OL} | $V_{DD} = 2.5 \text{ V}$ | | | 12 | mA |
| | $V_{DD} = 3.3 \text{ V}$ | | | 24 | |
| Operating free-air temperature, T_A | | -40 | | 85 | °C |

5.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | THERMAL AIR FLOW (CFM) | CDCV304 | | UNIT |
|-------------------------------|--|------------------------|------------|-----|------|
| | | | PW (TSSOP) | | |
| | | | 8 PINS | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | High K | 0 | 149 | °C/W |
| | | | 150 | 142 | |
| | | | 250 | 138 | |
| | | | 500 | 132 | |
| | | Low K | | 230 | |
| | | | | 185 | |
| | | | | 170 | |
| | | | | 150 | |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | | 43.7 | | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | | 102 | | |
| ψ_{JT} | Junction-to-top characterization parameter | | 1.8 | | |
| ψ_{JB} | Junction-to-board characterization parameter | | 100.2 | | |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|---------------------------|--------------------------------|---------------------------|----------------|--------------------|------|------|
| V_{IK} | Input voltage | $V_{DD} = 3 \text{ V}$, | $I_I = -18 \text{ mA}$ | | | -1.2 | V |
| V_{OH} | High-level output voltage | $V_{DD} = 2.3 \text{ V}$, | $I_{OH} = -8 \text{ mA}$ | 1.8 | | | V |
| | | $V_{DD} = 2.3 \text{ V}$, | $I_{OH} = -16 \text{ mA}$ | 1.5 | | | |
| | | $V_{DD} = \text{min to max}$, | $I_{OH} = -1 \text{ mA}$ | $V_{DD} - 0.2$ | | | |
| | | $V_{DD} = 3 \text{ V}$, | $I_{OH} = -24 \text{ mA}$ | 2 | | | |
| | | $V_{DD} = 3 \text{ V}$, | $I_{OH} = -12 \text{ mA}$ | 2.4 | | | |
| V_{OL} | Low-level output voltage | $V_{DD} = 2.3 \text{ V}$, | $I_{OL} = 8 \text{ mA}$ | | | 0.5 | V |
| | | $V_{DD} = 2.3 \text{ V}$, | $I_{OL} = 16 \text{ mA}$ | | | 0.7 | |
| | | $V_{DD} = \text{min to max}$, | $I_{OL} = 1 \text{ mA}$ | | | 0.2 | |
| | | $V_{DD} = 3 \text{ V}$, | $I_{OL} = 24 \text{ mA}$ | | | 0.8 | |
| | | $V_{DD} = 3 \text{ V}$, | $I_{OL} = 12 \text{ mA}$ | | | 0.55 | |
| I_{OH} | High-level output current | $V_{DD} = 3 \text{ V}$, | $V_O = 1 \text{ V}$ | -50 | | | mA |
| | | $V_{DD} = 3.3 \text{ V}$, | $V_O = 1.65 \text{ V}$ | | -55 | | |
| I_{OL} | Low-level output current | $V_{DD} = 3 \text{ V}$, | $V_O = 2 \text{ V}$ | 60 | | | mA |
| | | $V_{DD} = 3.3 \text{ V}$, | $V_O = 1.65 \text{ V}$ | | 70 | | |

(1) All typical values are with respect to nominal V_{DD} and $T_A = 25^\circ\text{C}$.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|---|---|-----|--------------------|-----|------|
| I_I | Input current | $V_I = V_O$ or V_{DD} | | | ±5 | μA |
| I_{DD} | Dynamic current, see Figure 1 | $f = 67$ MHz, $V_{DD} = 2.7$ V | | | 28 | mA |
| | | $f = 67$ MHz, $V_{DD} = 3.6$ V | | | 37 | |
| C_I | Input capacitance | $V_{DD} = 3.3$ V, $V_I = 0$ V or V_{DD} | | 3 | | pF |
| C_O | Output capacitance | $V_{DD} = 3.3$ V, $V_I = 0$ V or V_{DD} | | 3.2 | | pF |

5.5 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-----------------|-----------------|-----|-----|-----|------|
| f_{clk} | Clock frequency | | 0 | | 200 | MHz |

5.6 Switching Characteristics: $V_{DD} = 2.5$ V ± 10%

$V_{DD} = 2.5$ V ± 10%, $C_L = 10$ pF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-------------|-------------------------------|---|-----|--------------------|-----|------|
| t_{PLH} | Low-to-high propagation delay | See Figure 4 and Figure 5 | 2 | 2.9 | 4.5 | ns |
| t_{PHL} | High-to-low propagation delay | | 2 | 3 | 4.5 | |
| $t_{sk(o)}$ | Output skew ⁽²⁾ | See Figure 6 | | 50 | 150 | ps |
| t_r | Output rise slew rate | | 1.5 | 2.2 | 4 | V/ns |
| t_f | Output fall slew rate | | 1.5 | 2.2 | 4 | V/ns |

(1) All typical values are with respect to nominal V_{DD} .

(2) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

5.7 Switching Characteristics: $V_{DD} = 3.3$ V ± 10%

$V_{DD} = 3.3$ V ± 10%, $C_L = 10$ pF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------|--|---|-----|--------------------|-----|--------|
| t_{PLH} | Low-to-high propagation delay | See Figure 4 and Figure 5 | 1.8 | 2.4 | 3 | ns |
| t_{PHL} | High-to-low propagation delay | | 1.8 | 2.5 | 3 | |
| $t_{sk(o)}$ | Output skew ⁽²⁾ | | | 50 | 100 | ps |
| t_{jitter} | Additive phase jitter from input to output 1Y0 | 12 kHz to 5 MHz, $f_{out} = 30.72$ MHz | | 63 | | fs rms |
| | | 12 kHz to 20 MHz, $f_{out} = 125$ MHz | | 56 | | |
| $t_{sk(p)}$ | Pulse skew | $V_{IH} = V_{DD}$, $V_{IL} = 0$ V | | | 150 | ps |
| $t_{sk(pr)}$ | Process skew | | | 0.2 | 0.3 | ns |
| $t_{sk(pp)}$ | Part-to-part skew | | | 0.25 | 0.4 | ns |
| t_{high} | Clock high time, see Figure 7 | 66 MHz | 6 | | | ns |
| | | 140 MHz | 3 | | | |
| t_{low} | Clock low time, see Figure 7 | 66 MHz | 6 | | | ns |
| | | 140 MHz | 3 | | | |
| t_r | Output rise slew rate ⁽³⁾ | $V_O = 0.4$ V to 2 V | 1.5 | 2.7 | 4 | V/ns |
| t_f | Output fall slew rate ⁽³⁾ | $V_O = 2$ V to 0.4 V | 1.5 | 2.7 | 4 | V/ns |

(1) All typical values are with respect to nominal V_{DD} .

(2) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

(3) This symbol is according to PCI-X terminology.

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5.8 Typical Characteristics

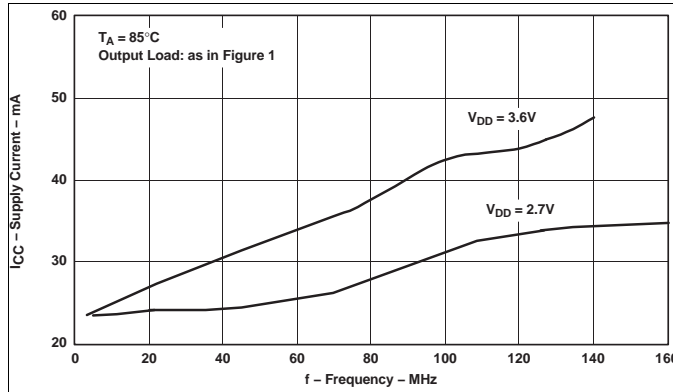


Figure 1. Supply Current vs Frequency

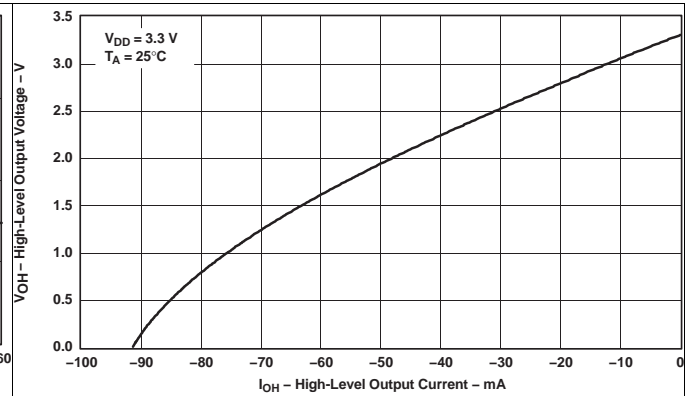


Figure 2. High-Level Output Voltage vs High-Level Output Current

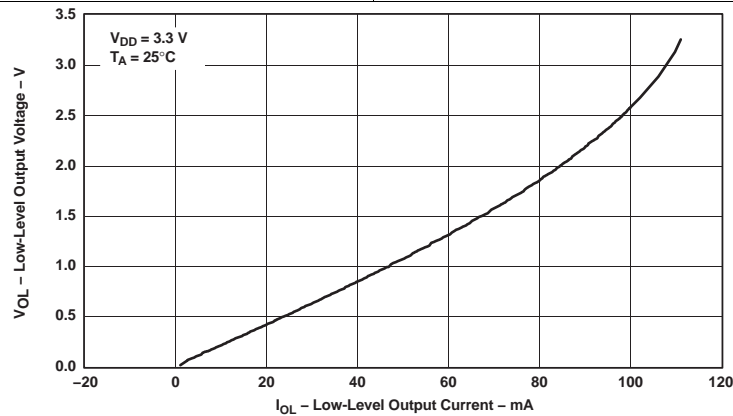


Figure 3. Low-Level Output Voltage vs Low-Level Output Current

6 Parameter Measurement Information

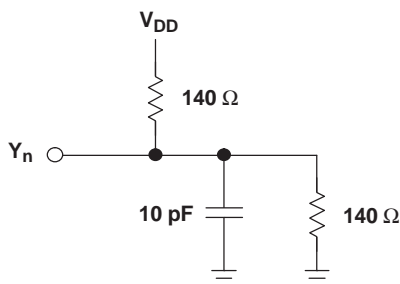


Figure 4. Test Load Circuit

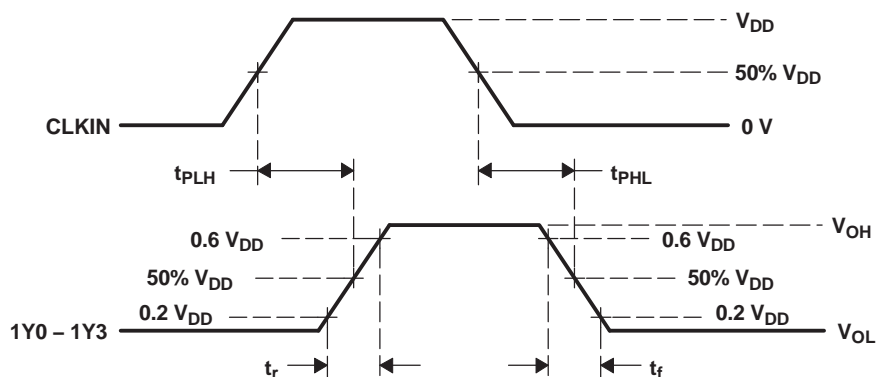


Figure 5. Voltage Waveforms Propagation Delay (t_{pd}) Measurements

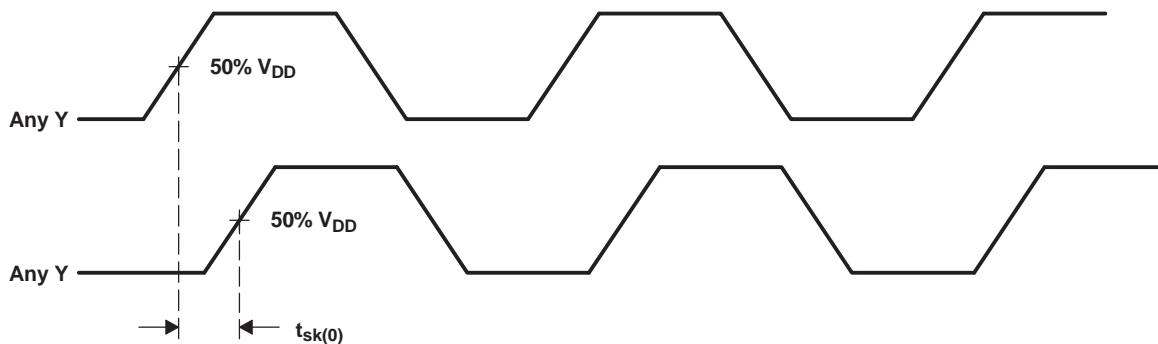
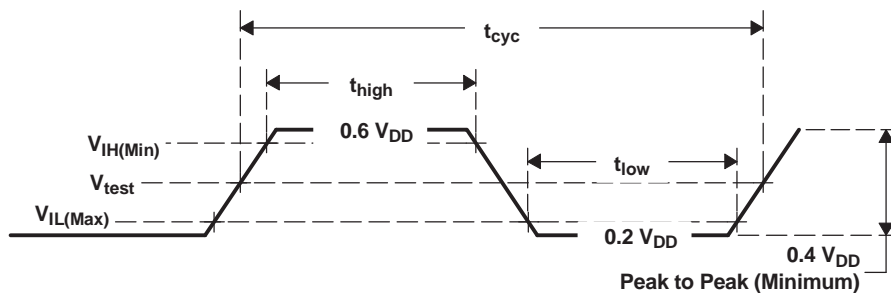


Figure 6. Output Skew

| PARAMETER | VALUE | UNIT |
|----------------------|---------------|------|
| $V_{IH(\text{Min})}$ | $0.5 V_{DD}$ | V |
| $V_{IL(\text{Max})}$ | $0.35 V_{DD}$ | V |
| V_{test} | $0.4 V_{DD}$ | V |



A. All parameters in Figure 7 are according to PCI-X 1.0 specifications.

Figure 7. Clock Waveform

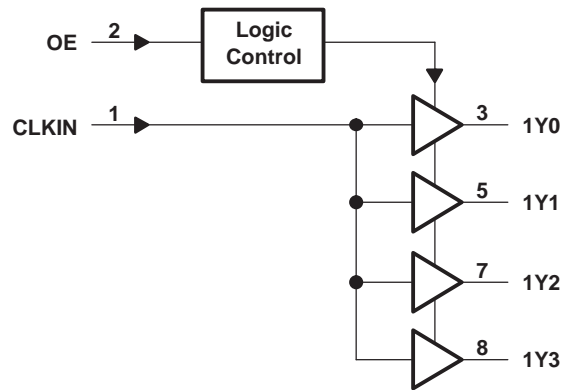
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7 Detailed Description

7.1 Functional Block Diagram



7.2 Device Functional Modes

Table 1. Function Table

| INPUTS | | OUTPUTS |
|--------|----|---------|
| CLKIN | OE | 1Y[0:3] |
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CDCV304PW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CKV304 | Samples |
| CDCV304PWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CKV304 | Samples |
| CDCV304PWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CKV304 | Samples |
| CDCV304PWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CKV304 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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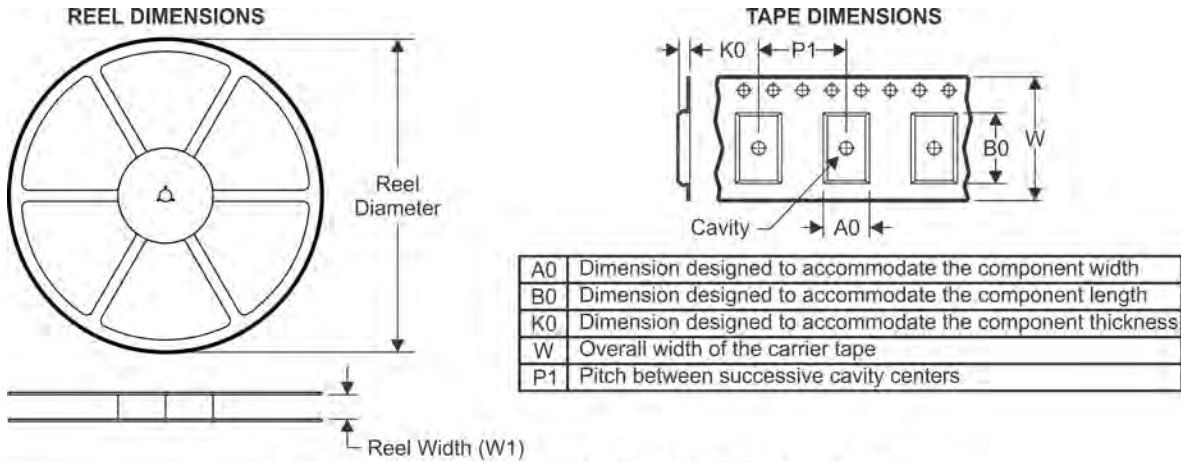
OTHER QUALIFIED VERSIONS OF CDCV304 :

- Enhanced Product: [CDCV304-EP](#)

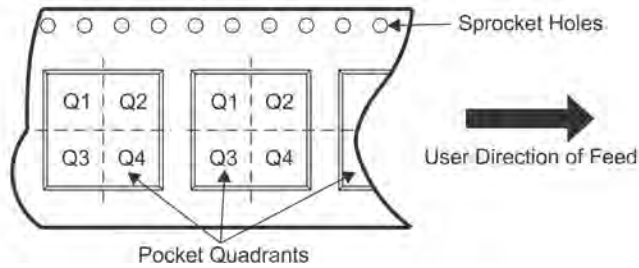
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



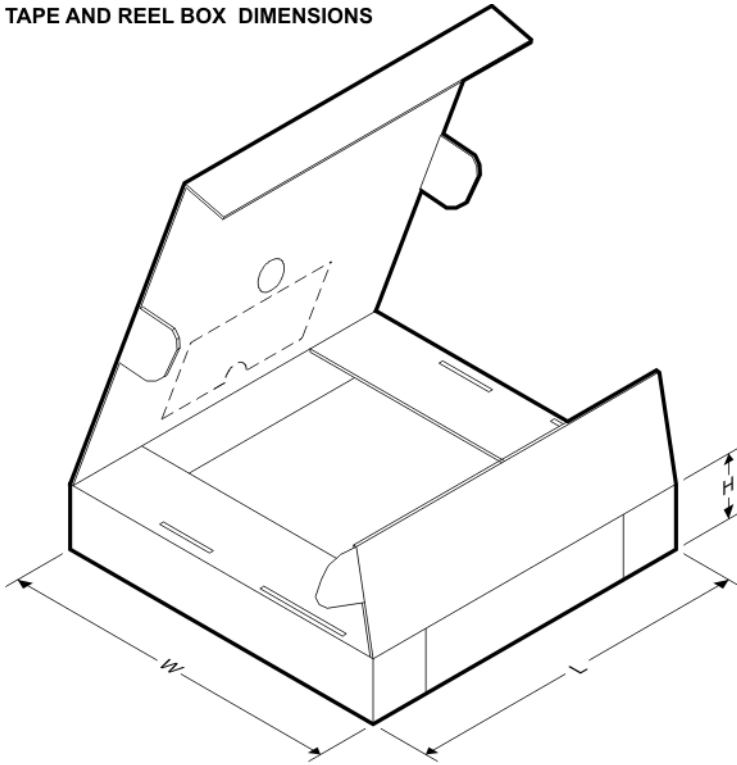
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCV304PWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

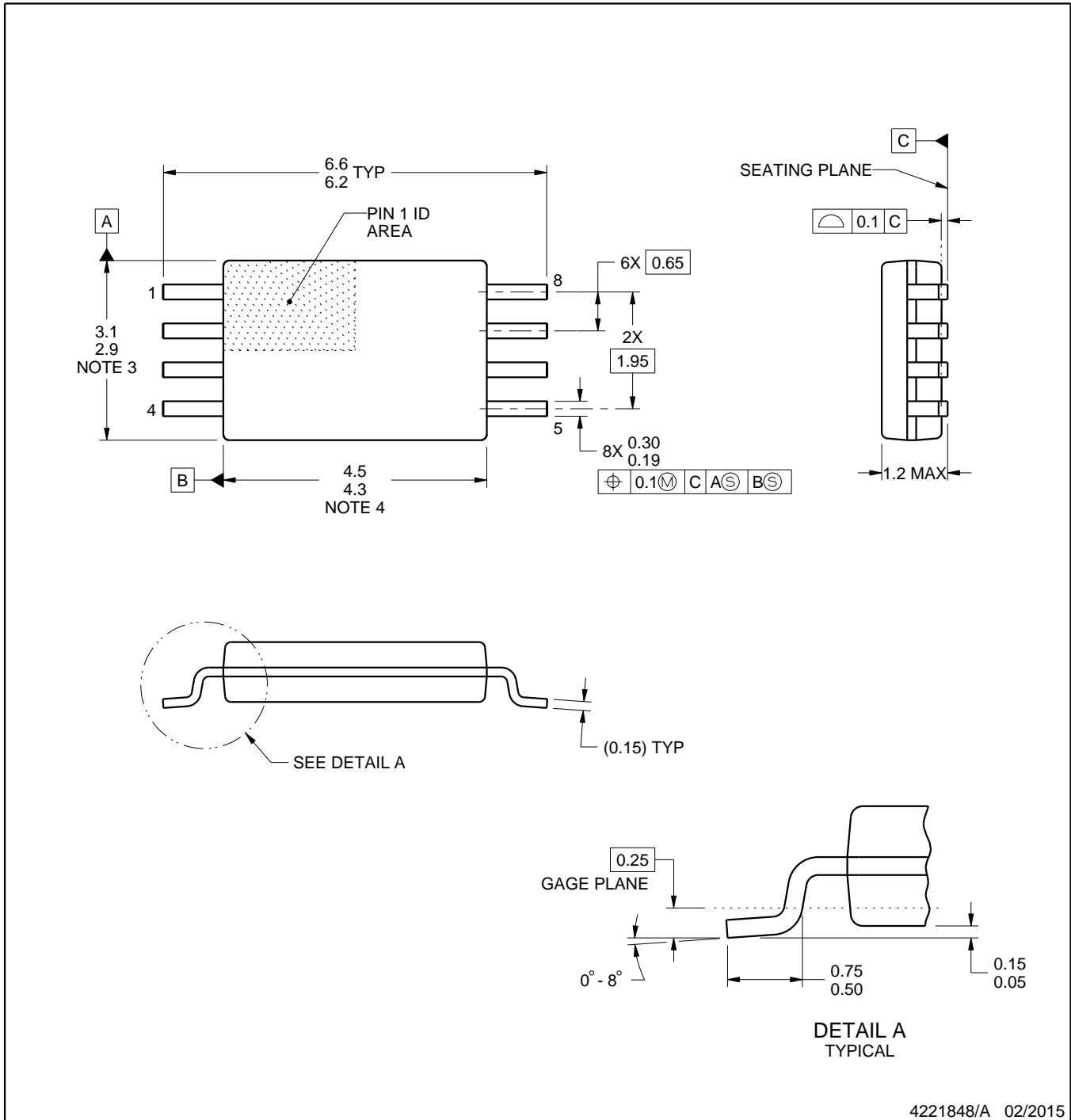
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCV304PWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

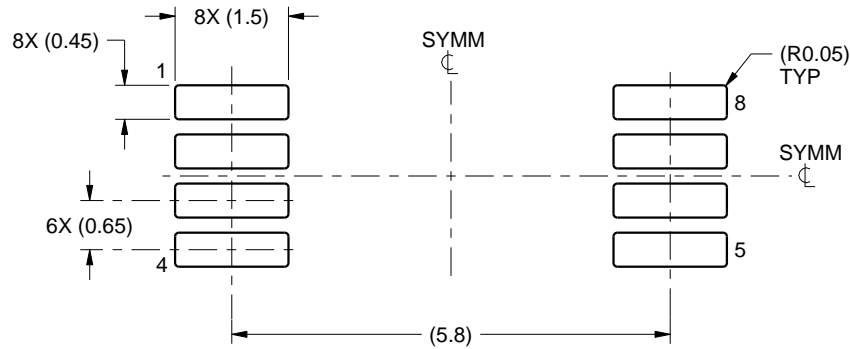
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

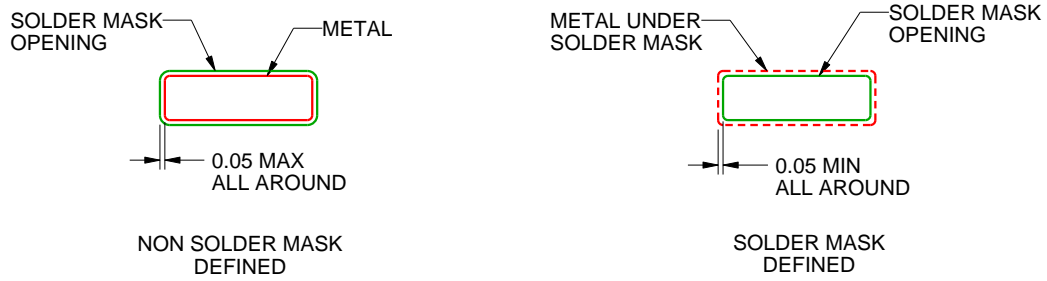
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

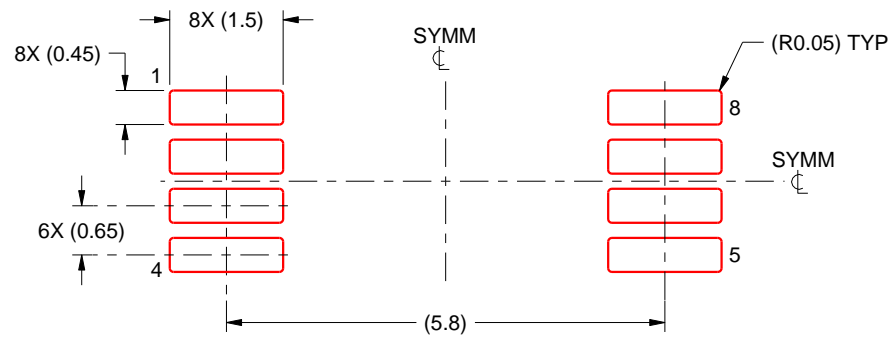
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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN**PW0008A****TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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