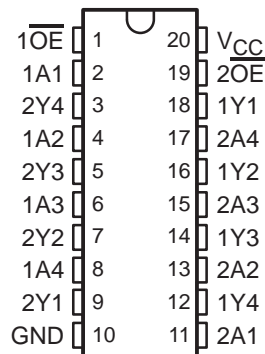


# CD74FCT244, CD74FCT244AT BiCMOS OCTAL BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS722B – JULY 2000 – REVISED AUGUST 2003

- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From  $V_{CC}$
- Controlled Output Edge Rates
- 64-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design

CD74FCT244 . . . E, M, OR SM PACKAGE  
CD74FCT244AT . . . E OR M PACKAGE  
(TOP VIEW)



## description/ordering information

The CD74FCT244 and CD74FCT244AT are octal buffer/line drivers with 3-state outputs using a small-geometry BiCMOS technology. The output stages are a combination of bipolar and CMOS transistors that limit the output high level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0 V to 3.7 V) reduces the power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

These devices are organized as two 4-bit buffers/line drivers with separate active-low output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – E	Tube	CD74FCT244E	CD74FCT244E
	SOIC – M	Tube	CD74FCT244M	74FCT244M
		Tape and reel	CD74FCT244M96	
	SSOP – SM	Tape and reel	CD74FCT244SM96	FCT244SM
	PDIP – E	Tube	CD74FCT244ATE	CD74FCT244ATE
	SOIC – M	Tube	CD74FCT244ATM	74FCT244ATM
Tape and reel		CD74FCT244ATM96		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each buffer/driver)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z



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 **TEXAS  
INSTRUMENTS**

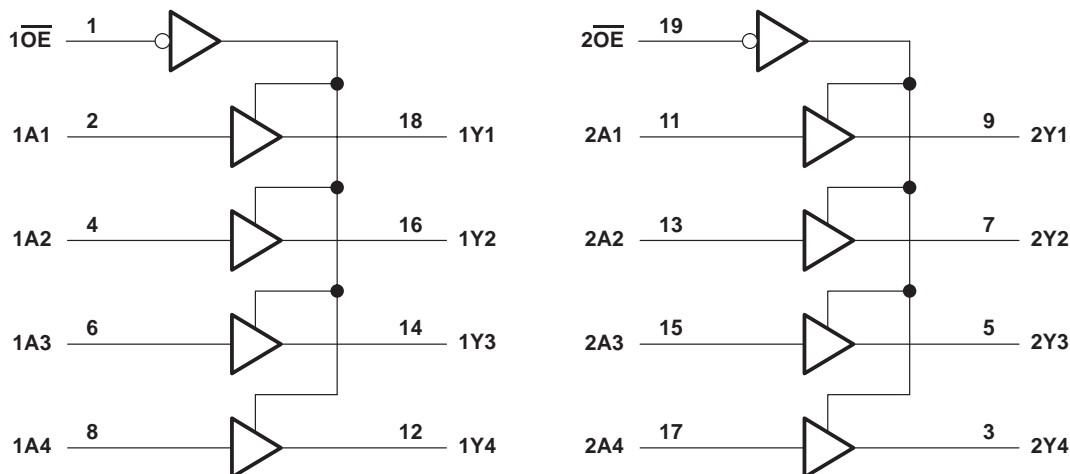
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# CD74FCT244, CD74FCT244AT BiCMOS OCTAL BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

DC supply voltage range, $V_{CC}$ .....	-0.5 V to 6 V
DC input clamp current, $I_{IK}$ ( $V_I < -0.5$ V) .....	-20 mA
DC output clamp current, $I_{OK}$ ( $V_O < -0.5$ V) .....	-50 mA
DC output sink current per output pin, $I_{OL}$ .....	70 mA
DC output source current per output pin, $I_{OH}$ .....	-30 mA
Continuous current through $V_{CC}$ , $I_{CC}$ .....	140 mA
Continuous current through GND .....	528 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): E package .....	69°C/W
M package .....	58°C/W
SM package .....	70°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 2)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5.25	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		-15	mA
$I_{OL}$ Low-level output current		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate (slew rate)		10	ns/V
$T_A$ Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**BiCMOS OCTAL BUFFERS/LINE DRIVERS**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V <sub>IK</sub>	I <sub>I</sub> = -18 mA	4.75 V		-1.2		-1.2	V
V <sub>OH</sub>	I <sub>OH</sub> = -15 mA	4.75 V	2.4		2.4		V
V <sub>OL</sub>	I <sub>OL</sub> = 64 mA	4.75 V		0.55		0.55	V
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.25 V		±0.1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.25 V		±0.5		±10	μA
I <sub>OS</sub> †	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = 0	5.25 V		-60		-60	mA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.25 V		8		80	μA
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.25 V		1.6		1.6	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			10		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND			15		15	pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.25 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CD74FCT244			CD74FCT244AT			UNIT
			T <sub>A</sub> = 25°C		T <sub>A</sub> = 25°C				
			TYP	MIN	MAX	TYP	MIN	MAX	
t <sub>pd</sub>	A	Y	4.5	1.5	6.5	3.8	1.5	5.3	ns
t <sub>en</sub>	$\overline{OE}$	Y	6	1.5	8	4.8	1.5	6.5	ns
t <sub>dis</sub>	$\overline{OE}$	Y	5	1.5	7	4.5	1.5	5.8	ns

**noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C**

PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>		1		V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>		0.5		V
V <sub>IH(D)</sub> High-level dynamic input voltage	2			V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.8	V

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

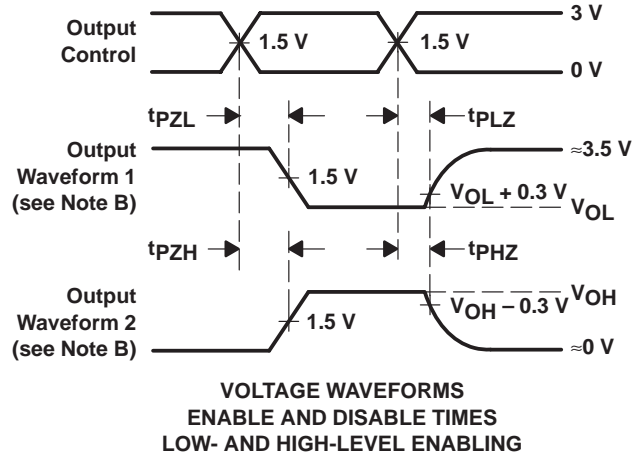
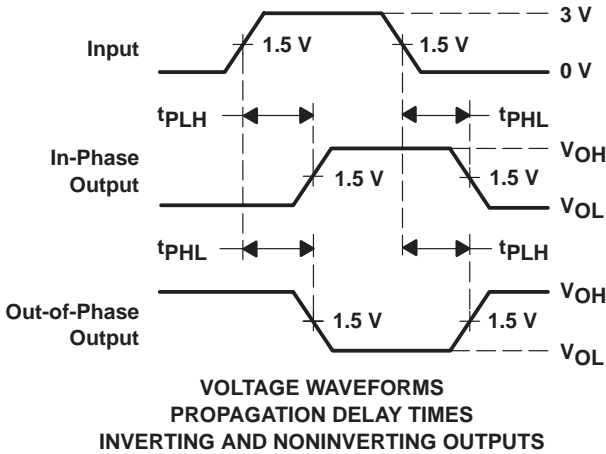
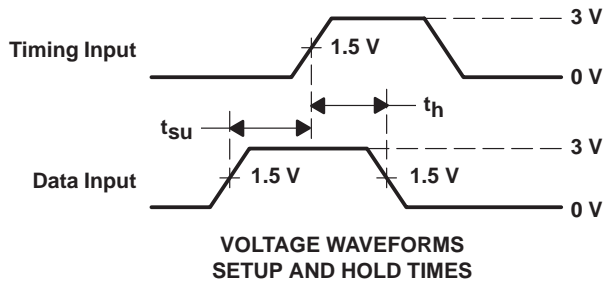
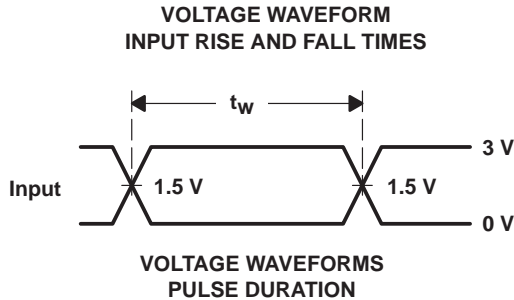
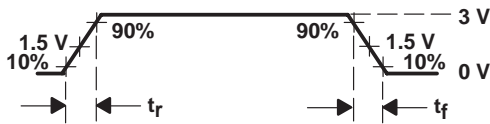
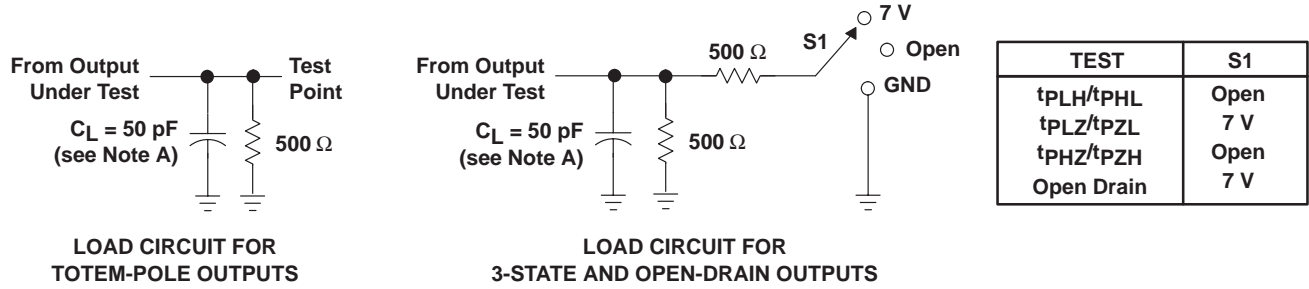
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	35	pF



# CD74FCT244, CD74FCT244AT BiCMOS OCTAL BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r$  and  $t_f = 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD74FCT244ATE	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	<a href="#">Purchase Samples</a>
CD74FCT244ATEE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	<a href="#">Purchase Samples</a>
CD74FCT244ATM	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244ATM96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244ATM96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244ATM96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244ATME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244ATMG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	<a href="#">Purchase Samples</a>
CD74FCT244EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	<a href="#">Purchase Samples</a>
CD74FCT244M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CD74FCT244M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD74FCT244ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
CD74FCT244MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

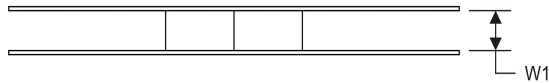
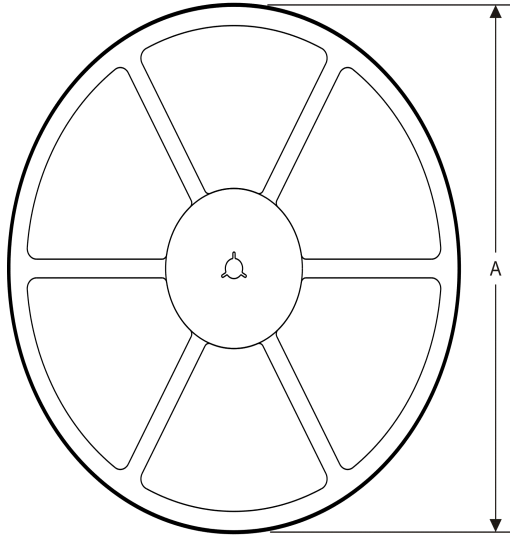
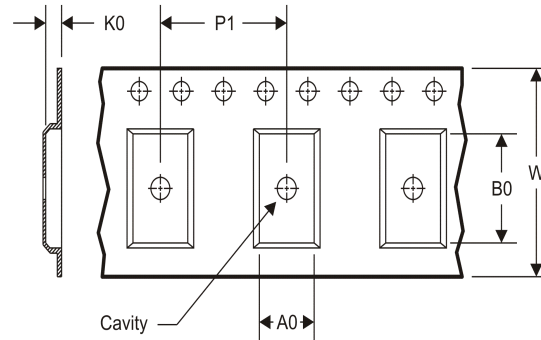
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74FCT244ATM96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74FCT244M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74FCT244ATM96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74FCT244M96	SOIC	DW	20	2000	367.0	367.0	45.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

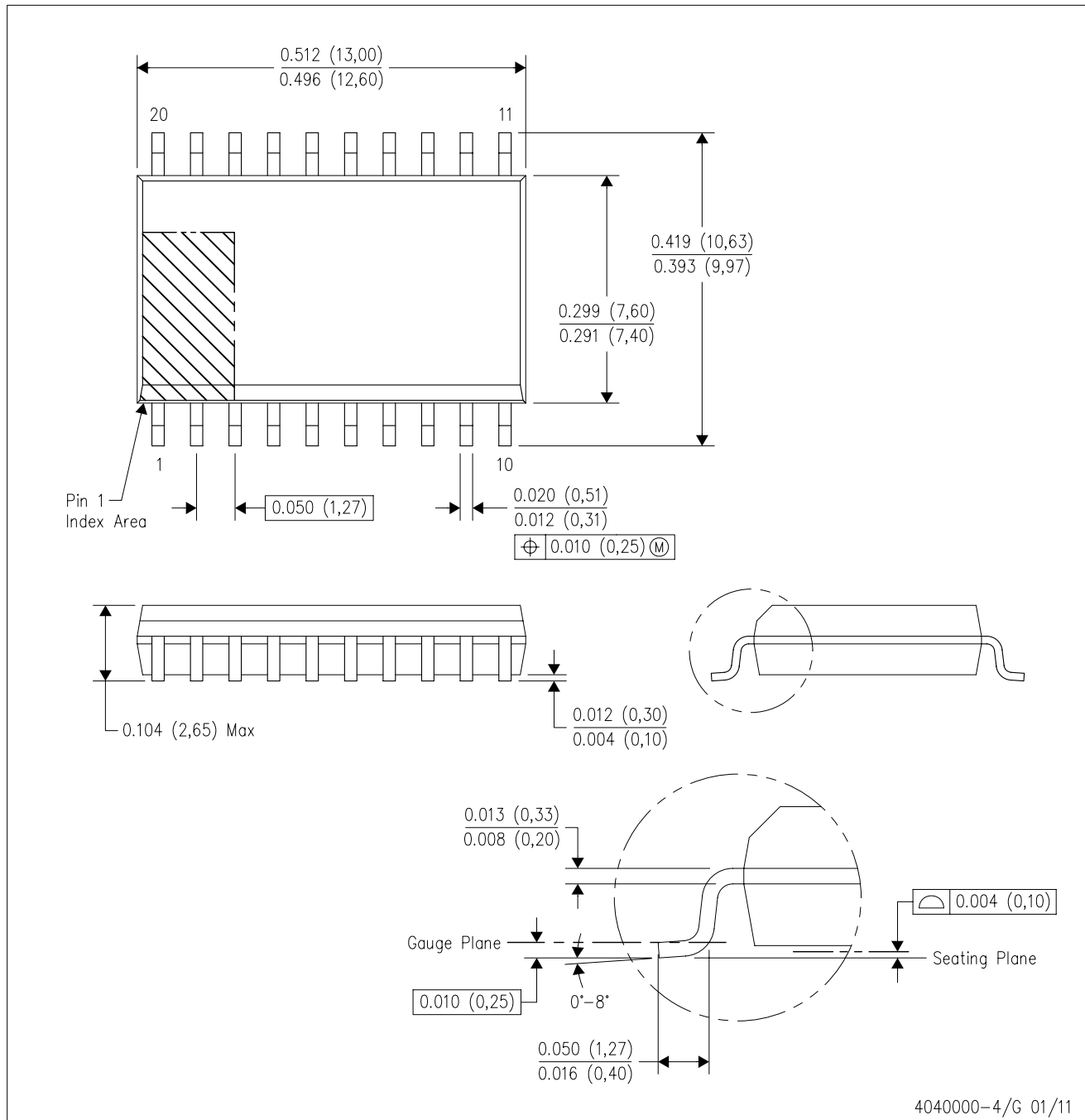
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

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