National Semiconductor Corporation

PRELIMINARY

COP220H/COP221H/COP222H/COP320H/ COP321H/COP322H/COP420H/COP421H/COP422H Single-Chip N-Channel Microcontroller

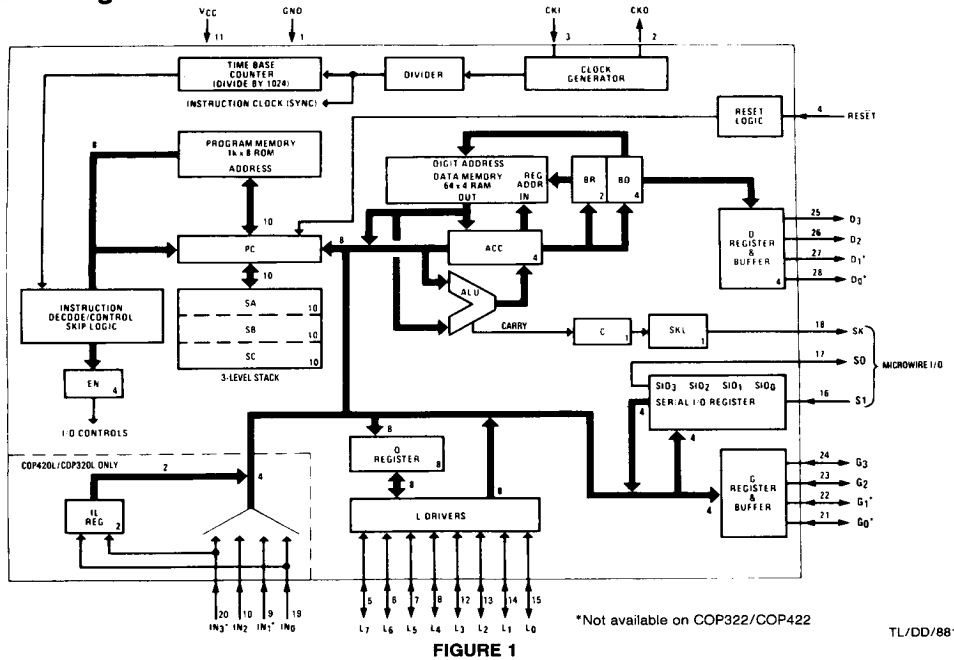
General Description

The COP420H is an enhanced version of the COP420L. It is fabricated in N-channel MOS. It combines the low power consumption of the COP420L and the faster cycle time of the COP420. It has all the software and hardware features of the COP400 series with some added options, and the LED/TRI-STATE® options replaced by an on chip current limiting resistor design. Also it has been designed for late programming of the ROM and hardware options. This allows for a very fast turnaround time for prototype parts. To meet the higher speed requirements the pull-ups and pull-downs had to be made stronger. They have been selected to meet most of the DC specs of the COP420. Therefore some DC parameters will exceed the maximum of the COP420L.

Features

- Low cost
- Low current drain (5 mA max.)
- Powerful instruction set of the COP420L
- 1k x 8 ROM, 64 x 4 RAM
- 4 μs instruction cycle time
- Single supply operation 4.5V–6.3V
- 23 I/O lines (COP420H)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- Internal binary counter register with MICROWIRE™ compatible serial I/O
- Internal time-base counter for real-time processing
- Direct drive of LED digit and segment lines
- General purpose and TRI-STATE outputs
- LSTTL/CMOS compatible in and out
- Software/hardware compatible with COP400 family of devices
- Wider supply range 4.5–9.5V optionally available
- Extended temperature range devices
  COP320H/COP321H/COP322H (−40°C to +85°C)
  COP220H/COP221H/COP222H (−40°C to +110°C)
- Optional internal initialization
- Inputs and open drain outputs able to withstand 15V

Block Diagram



*Not available on COP322/COP422

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FIGURE 1

COP420H/COP421H/COP422H

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage on Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Susceptibility (Note 4)	2000V

Power Dissipation	
COP420H/COP421H	0.75W at 25°C
	0.4W at 70°C
COP422H	0.65W at 25°C
	0.3W at 70°C
Total Source Current	120 mA
Total Sink Current	120 mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 9.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Standard Operating Voltage (V_{CC})	(Note 1)	4.5	6.3	V
Optional Operating Voltage (V_{CC})		4.5	9.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current	All Inputs and Outputs Open		5	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷32, ÷16, ÷8)				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})		−0.3	0.4	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		−0.3	0.6	V
$\overline{\text{RESET}}$ Input Levels	Schmitt Trigger Input			
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.6	V
SO Input Level (Test Mode)	(Note 3)	2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	with TTL Trip Level Options	2.0		V
Logic Low	Selected, V_{CC} = 5V ±5%	−0.3	0.8	V
Logic High	with High Trip Level Options	3.6		V
Logic Low	Selected	−0.3	1.2	V
Input Capacitance			7	pF
Hi-Z Input Leakage	$V_{IN} < 9.5V$	−1	+1	μA
	$9.5 \le V_{IN} \le 15V$	−10	+10	μA
Output Voltage Levels				
LSTTL Operation	V_{CC} = 5V ±10%			
Logic High (V_{OH})	I_{OH} = −25 μA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36 ma		0.4	V
CMOS Operation (Note 2)	V_{CC} = 4.5V			
Logic High	I_{OH} = −10 μA	V_{CC} −1		V
Logic Low	I_{OL} = +10 μA		0.2	V

Note 1: V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 2: TRI-STATE and LED configurations are excluded.

Note 3: SO output "0" level must be less than 0.8V for normal operation.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

DC Electrical Characteristics $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 9.5V$ unless otherwise noted (Continued)

Parameter	Conditions	Min	Max	Units
Output Current Levels				
Output Sink Current				
L_0–L_7 Outputs and Standard	$V_{CC} = 9.5V$, $V_{OL} = 0.4V$	3.2		mA
G_0–G_3, D_0–D_3 Outputs (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 0.4V$	2.3		mA
SO & SK	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	1.7		mA
G_0–G_3 and D_0–D_3 Outputs with	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	15		mA
High Current Options (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	11		mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	7.5		mA
G_0–G_3 and D_0–D_3 Outputs with	$V_{CC} = 9.5V$, $V_{OL} = 1.0V$	30		mA
Very High Current Options (I_{OL})	$V_{CC} = 6.3V$, $V_{OL} = 1.0V$	22		mA
	$V_{CC} = 4.5V$, $V_{OL} = 1.0V$	15		mA
CKI (Single-Pin RC Oscillator)	$V_{CC} = 4.5V$, $V_{IH} = 3.5V$	2.2		mA
CKO	$V_{CC} = 4.5V$, $V_{OL} = 0.4V$	1.8		mA
Output Source Current				
Standard Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−470	−2350	μA
All Outputs (I_{OH})	$V_{CC} = 6.3V$, $V_{OH} = 2.0V$	−250	−1250	μA
	$V_{CC} = 4.5V$, $V_{OH} = 2.0V$	−100	−500	μA
Push-Pull Configuration	$V_{CC} = 9.5V$, $V_{OH} = 4.75V$	−1.4		mA
SO and SK Outputs (I_{OH})	$V_{CC} = 6.3V$, $V_{OH} = 2.4V$	−1.4		mA
	$V_{CC} = 4.5V$, $V_{OH} = 1.0V$	−1.2		mA
LED Configuration, L_0–L_7				
Outputs, Low Current	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−6	−18	mA
Driver Option (I_{OH})	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−1.5	−7	mA
LED Configuration, L_0–L_7				
Outputs, High Current	$V_{CC} = 9.5V$, $V_{OH} = 2.0V$	−12	−36	mA
Driver Option (I_{OH})	$V_{CC} = 6.0V$, $V_{OH} = 2.0V$	−3.0	−14	mA
TRI-STATE Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	−0.75		mA
L_0–L_7 Outputs, Low	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	−0.8		mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−0.9		mA
TRI-STATE Configuration,	$V_{CC} = 9.5V$, $V_{OH} = 5.5V$	−1.5		mA
L_0–L_7 Outputs, High	$V_{CC} = 6.3V$, $V_{OH} = 3.2V$	−1.6		mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V$, $V_{OH} = 1.5V$	−100	−800	mA
Input Load Source Current	$V_{CC} = 5.0V$, $V_{IL} = 0V$	−10	−140	μA
CKO Output				
RAM Power Supply Option	$V_R = 3.3V$		3.0	mA
Power Requirement				
TRI-STATE Output Leakage Current		−2.5	+2.5	μA
Open Drain Output Leakage	$V_{OUT} < 9.5V$	−2.5	+2.5	μA
	$9.5V \le V_{OUT} < 15V$	−2.5	+2.5	μA
Total Sink Current Allowed				
All Outputs Combined			120	mA
D, G Ports			120	mA
L_7–L_4			4	mA
L_3–L_0			4	mA
All Other Pins			1.5	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L_7–L_4			60	mA
L_3–L_0			60	mA
Each L Pin			30	mA
All Other Pins			1.5	mA

COP320H/COP321H/COP322H

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage on Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Susceptibility (Note 4)	3000V

Power Dissipation	
COP320H/COP321H	0.75W at 25°C
COP220H/COP221H	0.4W at 70°C
COP322H/COP222H	0.65W at 25°C
	0.20W at 70°C
Total Source Current	120 mA
Total Sink Current	120 mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics

COP220H/221H/222H $-40°C \le T_A \le +110°C$, $4.5V \le V_{CC} \le 7.5V$; COP320H/321H/322H $-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 7.5V$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Standard Operating Voltage (V_{CC})	(Note 1)	4.5	5.5	V
Optional Operating Voltage (V_{CC})		4.5	7.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current	All Inputs and Outputs Open		8	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH}) V_{CC} = Max		3.0		V
Logic High (V_{IH})				
V_{CC} = 5V ±5%		2.2		V
Logic Low (V_{IL})		−0.3	0.3	V
Schmitt Trigger Input				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		−0.3	0.4	V
$\overline{\text{RESET}}$ Input Levels	Schmitt Trigger Input			
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.4	V
SO Input Level (Test Mode)	(Note 3)	2.2	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	with TTL Trip Level Options	2.2		V
Logic Low	Selected, V_{CC} = 5V ±5%	−0.3	0.6	V
Logic High	with High Trip Level Options	3.6		V
Logic Low	Selected	−0.3	1.2	V
Input Capacitance			7	pF
Hi-Z Input Leakage	$V_{IN} < 7.5$	−2	+2	μA
	$7.5 \le V_{IN} \le 15V$	−20	+20	μA
Output Voltage Levels				
LSTTL Operation	V_{CC} = 5V ±10%			
Logic High (V_{OH})	I_{OH} = −20 μA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36 mA		0.4	V
CMOS Operation (Note 2)	V_{CC} = 4.5V			
Logic High	I_{OH} = −10 μA	V_{CC} −1		V
Logic Low	I_{OL} = +10 μA		0.2	V

Note 1: V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 2: TRI-STATE and LED configurations are excluded.

Note 3: SO output "0" level must be less than 0.6V for normal operation.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

COP320H/COP321H/COP322H

DC Electrical Characteristics

$-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 7.5V$ unless otherwise noted (Continued)

Parameter	Conditions	Min	Max	Units
Output Current Levels				
Output Sink Current				
L_0–L_7 Outputs and Standard	$V_{CC} = 7.5V, V_{OL} = 0.4V$	2.5		mA
G_0–G_3 and D_0–D_3 Outputs (I_{OL})	$V_{CC} = 5.5V, V_{OL} = 0.4V$	1.9		mA
	$V_{CC} = 4.5V, V_{OL} = 0.4V$	1.6		mA
G_0–G_3 and D_0–D_3 Outputs with	$V_{CC} = 7.5V, V_{OL} = 1.0V$	12		mA
High Current Options (I_{OL})	$V_{CC} = 5.5V, V_{OL} = 1.0V$	9		mA
	$V_{CC} = 4.5V, V_{OL} = 1.0V$	7		mA
G_0–G_3 and D_0–D_3 Outputs with	$V_{CC} = 7.5V, V_{OL} = 1.0V$	24		mA
Very High Current Options (I_{OL})	$V_{CC} = 5.5V, V_{OL} = 1.0V$	18		mA
	$V_{CC} = 4.5V, V_{OL} = 1.0V$	14		mA
CKI (Single-Pin RC Oscillator)	$V_{CC} = 4.5V, V_{IH} = 3.5V$	2		mA
CKO	$V_{CC} = 4.5V, V_{OL} = 0.4V$	1.6		mA
Output Source Current				
Standard Configuration,	$V_{CC} = 7.5V, V_{OH} = 2.0V$	−330	−900	μA
All Outputs (I_{OH})	$V_{CC} = 5.5V, V_{OH} = 2.0V$	−110	−600	μA
	$V_{CC} = 4.5V, V_{OH} = 2.0V$	−92	−350	μA
Push-Pull Configuration	$V_{CC} = 7.5V, V_{OH} = 3.75V$	−0.85		mA
SO and SK Outputs (I_{OH})	$V_{CC} = 5.5V, V_{OH} = 2.0V$	−1.1		mA
	$V_{CC} = 4.5V, V_{OH} = 1.0V$	−1.2		mA
LED Configuration, L_0–L_7	$V_{CC} = 7.5V, V_{OH} = 2.0V$	−2.0	−130	mA
Outputs, Low Current	$V_{CC} = 6.0V, V_{OH} = 2.0V$	−1.5	−8.0	mA
Driver Option (I_{OH})				
LED Configuration, L_0–L_7	$V_{CC} = 7.5V, V_{OH} = 2.0V$	−2.7	−30	mA
Outputs, High Current	$V_{CC} = 6.0V, V_{OH} = 2.0V$	−2.7	−18	mA
Driver Option (I_{OH})				
TRI-STATE Configuration,	$V_{CC} = 7.5V, V_{OH} = 4.0V$	−0.7		mA
L_0–L_7 Outputs, Low	$V_{CC} = 5.5V, V_{OH} = 2.7V$	−0.6		mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V, V_{OH} = 1.5V$	−0.9		mA
TRI-STATE Configuration,	$V_{CC} = 7.5V, V_{OH} = 4.0V$	−1.4		mA
L_0–L_7 Outputs, High	$V_{CC} = 5.5V, V_{OH} = 2.7V$	−1.2		mA
Current Driver Option (I_{OH})	$V_{CC} = 4.5V, V_{OH} = 1.5V$	−1.8		mA
Input Load Source Current	$V_{CC} = 5.0V, V_{IL} = 0V$	−100	−1150	μA
CKO Output				
RAM Power Supply Option	$V_R = 3.3V$		4.0	mA
Power Requirement				
TRI-STATE Output Leakage Current		−5	+5	μA
Open Drain Output Leakage	$V_{OUT} < 7.5V$	−5	+5	μA
	$7.5V \le V_{OUT} \le 15V$	−50	+50	μA
Total Sink Current Allowed				
All Outputs Combined			120	mA
D, G Ports			120	mA
L_7–L_4			4	mA
L_3–L_0			4	mA
All Other Pins			1.5	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L_7–L_4			60	mA
L_3–L_0			60	mA
Each L Pin			30	mA
All Other Pins			1.5	mA

AC Electrical Characteristics

COP420H/COP421H/COP422H: $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 9.5V$ unless otherwise noted
COP320H/COP321H/COP322H: $-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 7.5V$ unless otherwise noted
COP220H/COP221H/COP222H: $-40°C \le T_A \le +110°C$, $4.5V \le V_{CC} \le 7.5V$

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time—t_C	(Note 4)	4.0	40	μs
CKI				
Input Frequency—f_I	÷32 Mode (Note 5)	0.8	4.0	MHz
	÷16 Mode	0.4	4.0	MHz
	÷8 Mode	0.2	2.0	MHz
	÷4 Mode	0.1	1.0	MHz
Duty Cycle		40	60	%
Rise Time	f_I = 4 MHz		60	ns
Fall Time			40	ns
CKI Using RC (÷4)	R = 15 kΩ ±5% C = 100 pF ±10%			
Instruction Cycle Time (Note 6)		16	28	μs
INPUTS:				
IN_3–IN_0, G_3–G_0, L_7–L_0				
t_{SETUP}		1.7		μs
t_{HOLD}		0.3		μs
SI				
t_{SETUP}		0.3		μs
t_{HOLD}		0.25		μs
OUTPUT PROPAGATION DELAY	Test Condition: C_L = 50 pF, R_L = 20 kΩ, V_{OUT} = 1.5V			
SO, SK Outputs				
t_{pd1}, t_{pd0}			0.25	μs
All Other Outputs				
t_{pd1}, t_{pd0}			1.4	μs

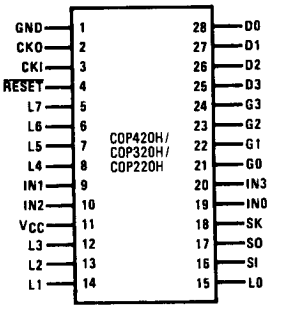
Note 4: COP420H Instruction cycle time is 4 μs ≤ T_{cycle} ≤ 40 μs.

Note 5: T_{cycle} = 4 μs cannot be achieved using CKI % 32.

Note 6: RC tolerances and the variation due to the device included.

Connection Diagrams

Dual-In Line Package



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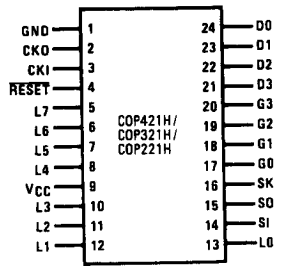
Top View

Order Number COP420H-XXX/N, COP320H-XXX/N or COP220H-XXX/N
See NS Package Number N28B

Dual-In Line Package



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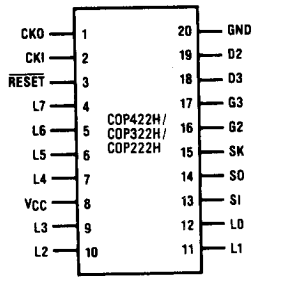
Top View

Order Number COP421H-XXX/M or COP421H-XXX/N COP321H-XXX/M or COP321H-XXX/N, or COP221H-XXX/M or COP221H-XXX/N
See NS Package Number M24B or N24A

Dual-In Line Package



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Top View

Order Number COP422H-XXX/M or COP422H-XXX/N COP322H-XXX/M or COP322H-XXX/N, or COP222H-XXX/M or COP222H-XXX/N
See NS Package Number M20B or N20A

FIGURE 2

Pin Descriptions

Pin	Description
L_7–L_0	8 bidirectional I/O ports with TRI-STATE
G_3–G_0	4 bidirectional I/O ports
D_3–D_0	4 general purpose outputs
IN_3–IN_0	4 general purpose inputs (COP420L only)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System oscillator output (or general purpose input, RAM power supply)
$\overline{RESET}$	System reset input
V_{CC}	Power supply
GND	Ground

Timing Diagrams

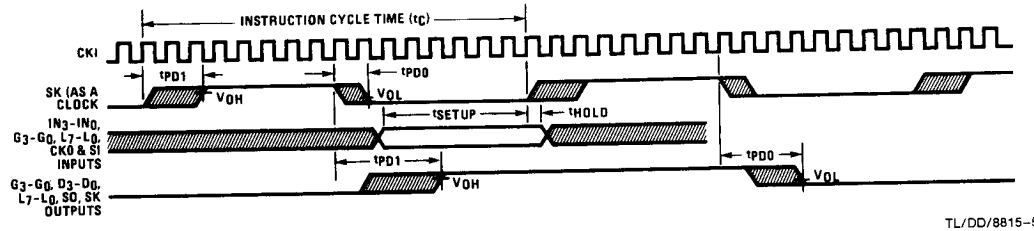

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FIGURE 3. Input/Output Timing Diagrams (Crystal Divide-by-16 Mode)

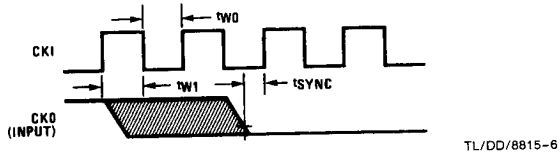

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FIGURE 3a. Synchronization Timing

Functional Description

For ease of reading this description, only COP420H and/or COP421H are referenced; however, all such references apply also to COP220H, COP221H, COP222H, COP320H, COP321H, COP322H, or COP422H.

A block diagram of the COP420H is given in *Figure 1.* Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2V). When a bit is reset, it is a logic "0" (less than 0.8V).

PROGRAM MEMORY

Program Memory consists of a 1,024 byte ROM. As can be seen by an examination of the COP420H/421H instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a 10-bit PC register. Its binary value selects one of the 1,024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are implemented by the 10-bit subroutine save registers, SA, SB and SC, providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

DATA MEMORY

Data memory consists of a 256-bit RAM, organized as 4 data registers of 16 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions is based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions of the COP420H/421H, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunctions with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below.)

Four general-purpose inputs, IN_3–IN_0, are provided.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. The D outputs can be directly connected to the digits of a multiplexed LED display.

The G register contents are outputs to 4 general-purpose bidirectional I/O ports. G I/O ports can be directly connected to the digits of a multiplexed LED display.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa–Sg and decimal point segments of the display.

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3–EN_0).

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediately following an interrupt, EN_1 is reset to disable further interrupts.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables

Functional Description (Continued)

the L drivers, placing the L I/O ports in a high-impedance input state.

4. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". The table below provides a summary of the modes associated with EN_3 and EN_0.

Enable Register Modes—Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

INTERRUPT

The following features are associated with the IN_1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once aknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level (PC + 1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met:
   1. EN_1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time,* the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines and LQID instructions should not be nested within the interrupt servicing routine since their popping the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.

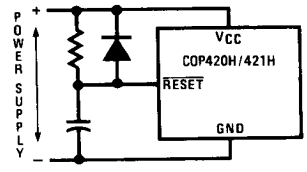
e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

INITIALIZATION

The Reset Logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1 μs. If the power supply rise time is greater than 1 ms, the user must provide an external RC network and diode to the $\overline{\text{RESET}}$ pin as shown below. The $\overline{\text{RESET}}$ pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{\text{RESET}}$ input, provided it stays low for at least three instruction cycle times.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.

Power-Up Clear Circuit



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RC ≥ 5 × Power Supply Rise Time

Functional Description (Continued)

OSCILLATOR

There are three basic clock oscillator configurations available as shown by *Figure 4.*

a. **Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 32 (optional by 16 or 8).

b. **External Oscillator.** CKI is an external clock input signal. The external frequency is divided by 32 (optional by 16 or 8) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R) or as a general purpose input.

c. **RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available as the RAM power supply (V_R) or as a general purpose input.

CKO PIN OPTIONS

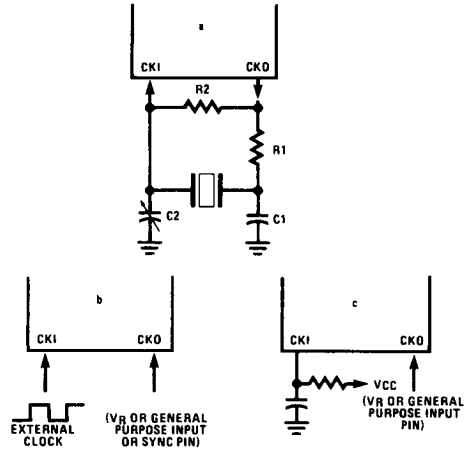
In a crystal controlled oscillator system, CKO is used as an output to the crystal network or it can be a general purpose input read into bit 2 of A (accumulator) upon execution of an INIL Instruction. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the COP420H/421H system timing configuration does not require use of the CKO pin.

RAM KEEP-ALIVE OPTION (Not available on COP422H)

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the RAM. To insure that RAM data integrity is maintained, the following conditions must be met:

1. $\overline{\text{RESET}}$ must go low before V_{CC} goes below spec during power-off; V_{CC} must be within spec before $\overline{\text{RESET}}$ goes high on power-up.
2. During normal operation V_R must be within the operating range of the chip, with $(V_{CC} - 1) \leq V_R \leq V_{CC}$.
3. V_R must be $\leq$ 3.3V with V_{CC} off.

Crystal Oscillator



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Crystal Oscillator

Crystal Value	Component Values		
	R1 (Ω)	R2 (Ω)	C (pF)
455 kHz	4.7k	1M	220
2.097 MHz	1k	1M	56
3.58 MHz	1k	1M	27
4 MHz	1k	1M	27

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time (μs)
51	100	19 ± 15%
82	56	19 ± 13%
12	100	5 ± 20%
6.8	220	5.3 ± 23%
8.2	300	8 ± 29%
22	100	8.6 ± 16%

Note: 200k ≥ R ≥ 5k
360 pF ≥ C ≤ 50 pF

FIGURE 4. COP420H/421H Oscillator

Functional Description (Continued)

I/O OPTIONS

COP420H/421H outputs have the following optional configurations, illustrated in *Figure 5*:

a. **Standard**—an enhancement mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with LSTTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.

b. **Open-Drain**—an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.

c. **Push-Pull**—An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. **Standard L**—same as **a.**, but may be disabled. Available on L outputs only.

e. **Open Drain L**—same as **b.**, but may be disabled. Available on L outputs only.

f. **LED Direct Drive**—an enhancement-mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (see Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display. Available on L outputs only.

g. **TRI-STATE Push-Pull**—an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L outputs only.

COP420H/COP421H inputs have the following optional configurations:

h. An on-chip depletion load device to V_{CC}.

i. A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1–6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 6* for each of these devices to allow the designer to effectively use these I/O configurations in designing a COP420H/421H system.

The SO, SK outputs can be configured as shown in **a.**, **b.**, or **c.** The D and G outputs can be configured as shown in **a.** or **b.** Note that when inputting data to the G ports, the G outputs should be set to "1". The L outputs can be configured as in **d.**, **e.**, **f.** or **g.**

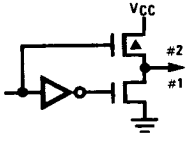
An important point to remember if using configuration **d.** or **f.** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see *Figure 6,* device 2); however, when the L lines are used as inputs, the disabled depletion device *cannot* be relied on to source sufficient current to pull an input to a logic 1.

COP421H

If the COP420H is bonded as a 24-pin device, it becomes the COP421H, illustrated in *Figure 2,* COP420H/421H Connection Diagrams. Note that the COP421H does not contain the four general purpose IN inputs (IN_3–IN_0). Use of this option precludes, of course, use of the IN options and the interrupt feature. All other options are available for the COP421H.

COP422H

If the COP421H is bonded as a 20-pin device, it becomes the COP422H, as illustrated in *Figure 2.* Note that the COP422H contains all the COP421H pins except D_0, D_1, G_0, and G_1. COP422H also does not allow RAM power supply input as a valid CKO pin option.



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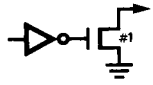
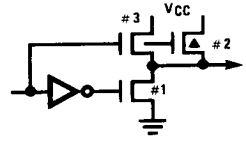
a. Standard Output



TL/DD/8815–10

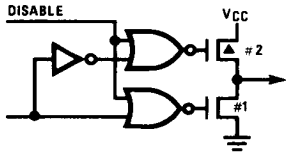
b. Open-Drain Output



TL/DD/8815–11

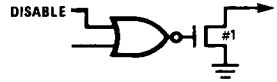
c. Push-Pull Output

Functional Description (Continued)



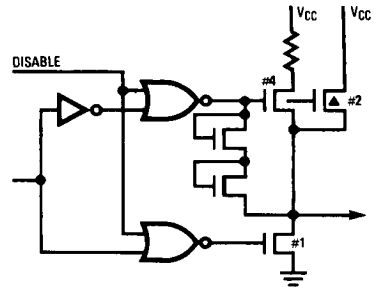
TL/DD/8815-12

d. Standard L Output



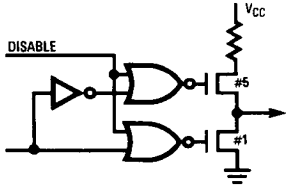
TL/DD/8815-13

e. Open-Drain L Output



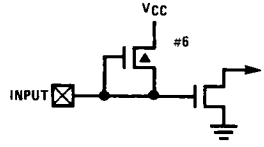
(▲ is Depletion Device) TL/DD/8815-14

f. LED (L Output)



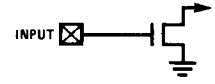
TL/DD/8815-15

g. TRI-STATE Push-Pull (L Output)



TL/DD/8815-16

h. Input with Load



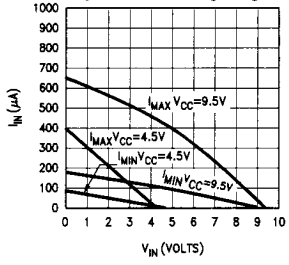
TL/DD/8815-17

i. HI-Z Input

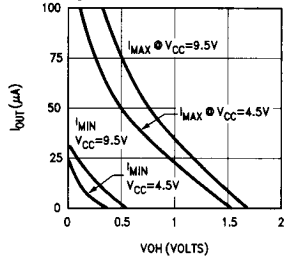
FIGURE 5. Output Configurations

Typical Performance Characteristics

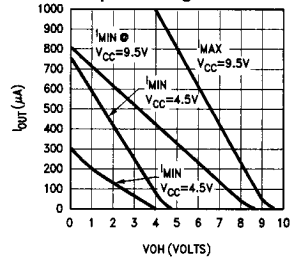
Input Current IN_0–IN_3



Input Current for L_0–L_7 when Output Programmed OFF by Software

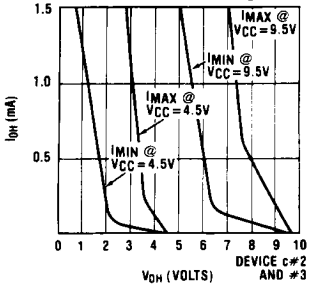


Source Current for Standard Output Configuration



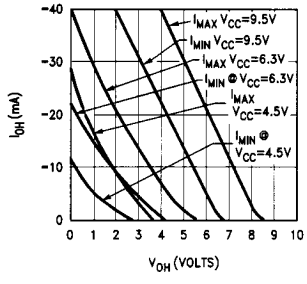
TL/DD/8815-18

Source Current for SO and SK in Push-Pull Configuration

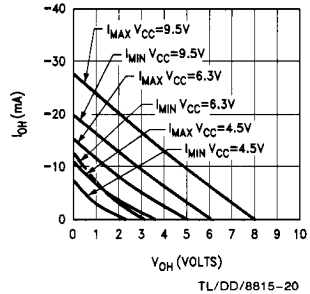


TL/DD/8815-19

Source Current for L_0–L_7 in TRI-STATE Configuration (High Current Option)



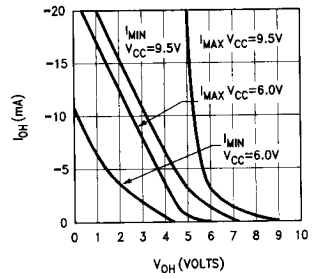
Source Current for L_0–L_7 in TRI-STATE Configuration (Low Current Option)



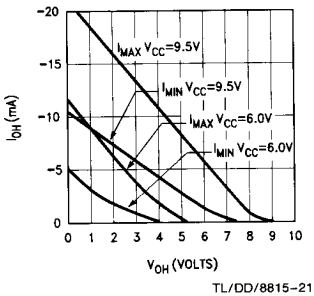
TL/DD/8815-20

Typical Performance Characteristics (Continued)

LED Output Source Current (High Current LED Option)

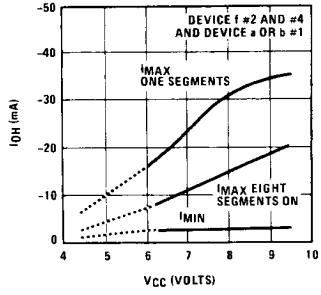


LED Output Source Current (Low Current LED Option)



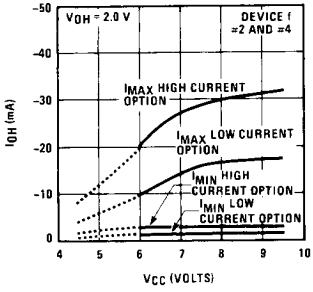
TL/DD/8815-21

LED Output Direct Segment and Digit Drive (High Current Options on L_0–L_7; Very High Current Options on D_0–D_3 or G_0–G_3)



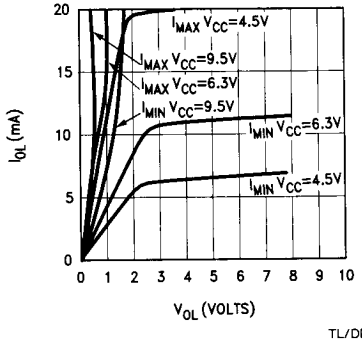
TL/DD/8815-22

LED Output Direct Segment Drive



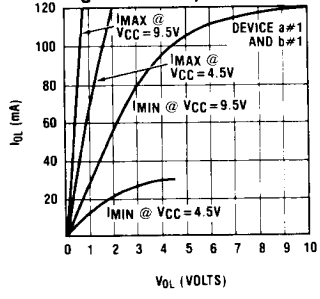
TL/DD/8815-23

Output Sink Current for SO and SK



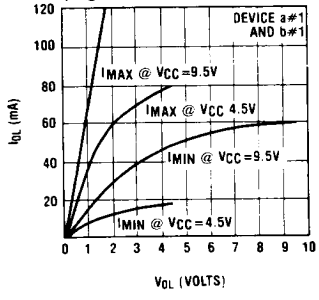
TL/DD/8815-24

Output Sink Current for G_0–G_3 and D_0–D_3 with Very High Current Option



TL/DD/8815-25

Output Sink Current for G_0–G_3 and D_0–D_3 (High Current Option)

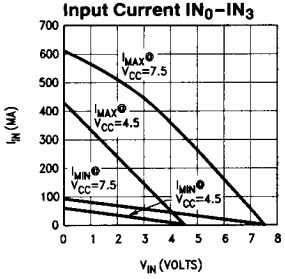


TL/DD/8815-26

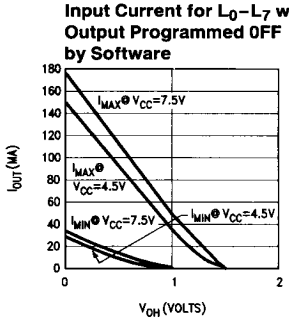
FIGURE 6. COP420H/COP421H/COP422H Input/Output Characteristics

Typical Performance Characteristics (Continued)

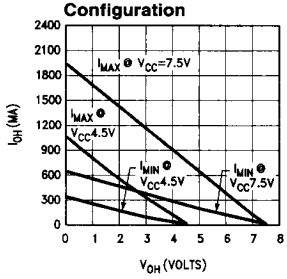
Input Current IN_0–IN_3



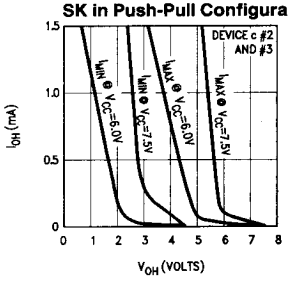
Input Current for L_0–L_7 when Output Programmed OFF by Software



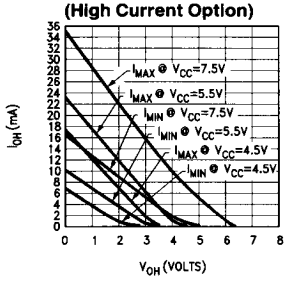
Source Current for Standard Configuration



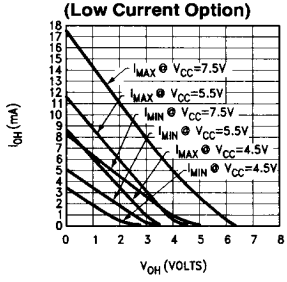
Source Current for SO and SK in Push-Pull Configuration



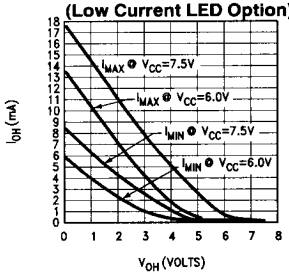
Source Current for L_0–L_7 in TRI-STATE Configuration (High Current Option)



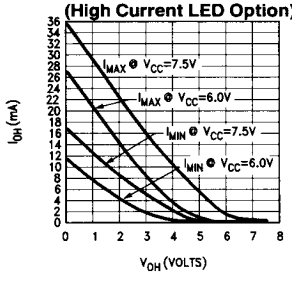
Source Current for L_0–L_7 in TRI-STATE Configuration (Low Current Option)



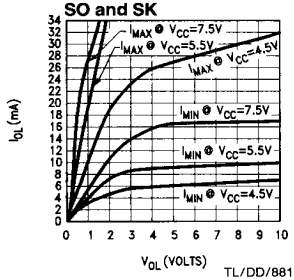
LED Output Source Current (Low Current LED Option)



LED Output Source Current (High Current LED Option)



Output Sink Current for SO and SK



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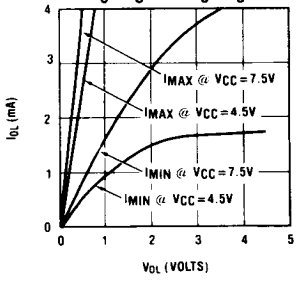
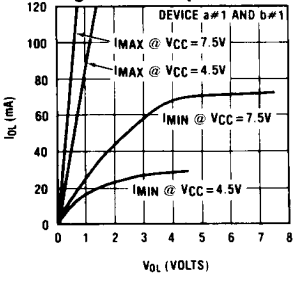
Output Sink Current for L_0–L_7 and Standard Drive Option for D_0–D_3 and G_0–G_3



Output Sink Current for G_0–G_3 and D_0–D_3 with Very High Current Option



Output Sink Current for G_0–G_3 and D_0–D_3 (High Current Option)

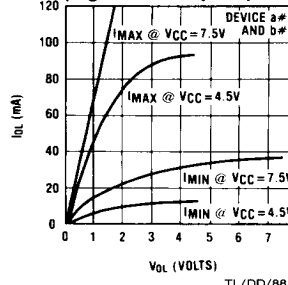


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FIGURE 7. COP320H/COP321H/COP322H Input/Output Characteristics

COP420H/COP421H Instruction Set

Table I is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table II provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the COP420H/421H instruction set.

TABLE I. COP420H/421H Instruction Set Table Symbols

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
IL	Two 1-bit Latches associated with the IN_3 or IN_0 inputs
IN	4-bit Input Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	10-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	10-bit Subroutine Save Register A
SB	10-bit Subroutine Save Register B
SC	10-bit Subroutine Save Register C
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0–15 binary (RAM Digit Select)
r	2-bit Operand Field, 0–3 binary (RAM Register Select)
a	10-bit Operand Field, 0–1023 binary (ROM Address)
y	4-bit Operand Field, 0–15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
–	Minus
→	Replaces
← →	Is exchanged with
=	Is equal to
$\overline{A}$	The ones complement of A
⊕	Exclusive-OR
:	Range of values

Instruction Set (Continued)

TABLE II. COP420H/421H Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011 | 0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011 | 0001	A + RAM(B) → A	None	Add RAM to A
ADTD		4A	0100 | 1010	A + 10_{10} → A	None	Add Ten to A
AISC	y	5–	0101 | y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CASC		5–	0001 | 0000	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Compliment and Add with Carry, Skip on Carry
CLRA		00	0000 | 0000	0 → A	None	Clear A
COMP		40	0100 | 0000	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0100 | 0100	None	None	No Operation
RC		32	0011 | 0010	"0" → C	None	Reset C
SC		22	0010 | 0010	"1" → C	None	Set C
XOR		02	0000 | 0010	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111 | 1111	ROM ($PC_{9:8}$, A,M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6– – –	0110 | 00 | $a_{9:8}$ $a_{7:0}$	a → PC	None	Jump
JP	a	– –	1 | $a_{6:0}$ (pages 2,3 only) or	a → $PC_{6:0}$	None	Jump within Page (Note 4)
		– –	11 | $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	– –	10 | $a_{5:0}$	PC + 1 → SA → SB → SC 0010 → $PC_{9:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6– – –	0110 | 10 | $a_{9:8}$ $a_{7:0}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	0100 | 1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100 | 1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip

Instruction Set (Continued)

TABLE II. COP420H/421H Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33	0011 | 0011	$A \rightarrow Q_{7:4}$	None	Copy A, RAM to Q
		3C	0011 | 1100	$RAM(B) \rightarrow Q_{3:0}$		
CQMA		33	0011 | 0011	$Q_{7:4} \rightarrow RAM(B)$	None	Copy Q to RAM, A
		2C	0010 | 1100	$Q_{3:0} \rightarrow A$		
LD	r	–5	00 | r | 0101	$RAM(B) \rightarrow A$ $Br \oplus r \rightarrow Br$	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23	0010 | 0011	$RAM(r,d) \rightarrow A$	None	Load A with RAM pointed to directly by r,d
		– –	00 | r | d			
LID		33	0011 | 0011			No Skip Condition Load RAM; A Indirect
		19	0001 | 1001	ROM (PC 9:8, A, M) $\rightarrow$ M, A		
LQID		BF	1011 | 1111	$ROM(PC_{9:8},A,M) \rightarrow Q$ $SB \rightarrow SC$	None	Load Q Indirect (Note 3)
RMB	0	4C	0100 | 1100	$0 \rightarrow RAM(B)_0$	None	Reset RAM Bit
	1	45	0100 | 0101	$0 \rightarrow RAM(B)_1$		
	2	42	0100 | 0010	$0 \rightarrow RAM(B)_2$		
	3	43	0100 | 0011	$0 \rightarrow RAM(B)_3$		
SMB	0	4D	0100 | 1101	$1 \rightarrow RAM(B)_0$	None	Set RAM Bit
	1	47	0100 | 1101	$1 \rightarrow RAM(B)_1$		
	2	46	0100 | 0110	$1 \rightarrow RAM(B)_2$		
	3	4B	0100 | 1011	$1 \rightarrow RAM(B)_3$		
STII	y	7–	0111 | y	$y \rightarrow RAM(B)$ $Bd + 1 \rightarrow Bd$	None	Store Memory Immediate and Increment Bd
X	r	–6	00 | r | 0110	$RAM(B) \longleftrightarrow A$ $Br \oplus r \rightarrow Br$	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23	0010 | 0011	$RAM(r,d) \longleftrightarrow A$	None	Exchange A with RAM pointed to directly by (r,d)
		– –	10 | r | d			
XDS	r	–7	00 | r | 0111	$RAM(B) \longleftrightarrow A$ $Bd - 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	–4	00 | r | 0100	$RAM(B) \longleftrightarrow A$ $Bd + 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

OPTION LIST

The COP420H/421H mask-programmable options are assigned numbers which correspond with the COP*420H* pins.

The following is a list of COP420H options. When specifying a COP421H chip, Options 9, 10, 19, and 20 must all be set to zero. When specifying a COP422H chip, options 9, 10, 19, and 20 must all be set to zero; options 21 and 22 may not be set to one, three or five; and option 2 may not be set to one. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Instruction Set (Continued)

TABLE II. COP420H/421H Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 | 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 | 1110	Bd → A	None	Copy Bd to A
LBI	r,d	– –	00 | r | (d−1) (d = 0,9:15) or	r,d → B	Skip until not an LBI	Load B Immediate with r,d (Note 6)
		33	0011 | 0011			
		– –	10 | r | d (any d)			
LEI	y	33	0011 | 0011	y → EN	None	Load EN Immediate (Note 7)
		6–	0110 | y			
XABR		12	0001 | 0010	A ⟷ Br (0,0 → A_3,A_2)	None	Exchange A with Br
TEST INSTRUCTIONS						
SKC		20	0010 | 0000		C = "1"	Skip if C is True
SKE		21	0010 | 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33	0011 | 0011		$G_{3:0}$ = 0	Skip if G is Zero (all 4 bits)
		21	0010 | 0001			
SKGBZ		33	0011 | 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 | 0001	2nd byte	G_0 = 0	
	1	11	0001 | 0001	2nd byte	G_1 = 0	
	2	03	0000 | 0011	2nd byte	G_2 = 0	
	3	13	0001 | 0011	2nd byte	G_3 = 0	
SKMBZ	0	01	0000 | 0001		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0001 | 0001		$RAM(B)_1$ = 0	
	2	03	0000 | 0011		$RAM(B)_2$ = 0	
	3	13	0001 | 0011		$RAM(B)_3$ = 0	
SKT		41	0100 | 0001		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)

Instruction Set (Continued)

TABLE II. COP420H/421H Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33	0011 | 0011	G → A	None	Input G Ports to A
		2A	0010 | 1010			
ININ		33	0011 | 0011	IN → A	None	Input IN Inputs to A (Note 2)
		28	0010 | 1000			
INIL		33	0011 | 0011	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Note 3)
		29	0010 | 1001			
INL		33	0011 | 0011	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
		2E	0010 | 1110			
OBD		33	0011 | 0011	Bd → D	None	Output Bd to D Outputs
		3E	0011 | 1110			
OGI	y	33	0011 | 0011	y → G	None	Output to G Ports Immediate
		5–	0101 | y			
OMG		33	0011 | 0011	RAM(B) → G	None	Output RAM to G Ports
		3A	0011 | 1010			
XAS		4F	0100 | 1111	A ⟷ SIO, C → SKL	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ instruction is only available on the 28-pin COP420L as the other devices do not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d'" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

Description of Selected Instructions

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing COP420H/421H programs.

XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above.) If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 10-bit word, $PC_{9:8}$, A, M. PC_9 and PC_8 are not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

Description of Selected Instructions (Continued)

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL_3 and IL_0 (see *Figure 8*) and CKO into A. The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL_3 and IL_0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN_3 and IN_0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs IN_3–IN_0 are input to A upon execution of an ININ instruction. (See Table II, ININ instruction.) INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction. IL latches are *not cleared* on reset.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word PC_9, PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of PC as follows: A → $PC_{7:4}$, RAM(B) → $PC_{3:0}$, leaving PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note the LQID takes two instruction cycle times to execute.

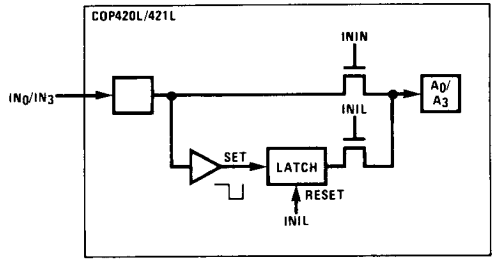

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FIGURE 8. INIL Hardware Implementation

SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the COP420H/421H to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 65 kHz (crystal frequency ÷ 32) and the binary counter output pulse frequency will be 64 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 64 ticks.

INSTRUCTION SET NOTES

a. The first word of a COP420H/421H program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c. The ROM is organized into 16 pages of 64 words each. The Program Counter is a 10-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11, or 15 will access data in the next group of four pages.

Option List

The Option Table should be copied and sent in with your EPROM or disc.

Option 1 = 0: Ground Pin—no options available

Option 2: CKO Output
- = 0: clock generator output to crystal/resonator (0 not allowable value if Option 3 = 3)
- = 1: pin is RAM power supply (V_R) input (not available on the COP422L)
- = 2: general purpose input with load device to V_{CC}
- = 3: general purpose input, Hi-Z

Option 3: CKI Input
- = 0: oscillator input divided by 32 (4 MHz max.)
- = 1: oscillator input divided by 16 (4 MHz max.)
- = 2: oscillator input divided by 8 (2 MHz max.)
- = 3: single-pin RC controlled oscillator (÷4)
- = 4: Schmitt trigger clock input (÷4)

Option 4: RESET Input
- = 0: load device to V_{CC}
- = 1: Hi-Z Input

Option 5: L_7 Driver
- = 0: Standard output
- = 1: Open-drain output
- = 2: High current LED direct segment drive output
- = 3: High current TRI-STATE push-pull output
- = 4: Low-current LED direct segment drive output
- = 5: Low-current TRI-STATE push-pull output

Option 6: L_6 Driver
same as Option 5

Option 7: L_5 Driver
same as Option 5

Option 8: L_4 Driver
same as Option 5

Option 9: IN_1 Input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 10: IN_2 Input
same as Option 9

Option 11: V_{CC} pin
- = 0: Standard V_{CC}
- = 1: Optional higher voltage V_{CC}

Option 12: L_3 Driver
same as Option 5

Option 13: L_2 Driver
same as Option 5

Option 14: L_1 Driver
same as Option 5

Option 15: L_0 Driver
same as Option 5

Option 16: SI Input
same as Option 9

Option 17: SO Driver
- = 0: standard output
- = 1: open-drain output
- = 2: push-pull output

Option 18: SK Driver
same as Option 17

Option 19: IN_0 Input
same as Option 9

Option 20: IN_3 Input
same as Option 9

Option 21: G_0 I/O Port
- = 0: very-high current standard output
- = 1: very-high current open-drain output
- = 2: high current open-drain output
- = 3: high current open-drain output
- = 4: standard LSTTL output (fanout = 1)
- = 5: open-drain LSTTL output (fanout = 1)

Option 22: G_1 I/O Port
same as Option 21

Option 23: G_2 I/O Port
same as Option 21

Option 24: G_3 I/O Port
same as Option 21

Option 25: D_3 Output
same as Option 21

Option 26: D_2 Output
same as Option 21

Option 27: D_1 Output
same as Option 21

Option 28: D_0 Output
same as Option 21

Option 29: L Input Levels
- = 0: standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
- = 1: higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 30: IN Input Levels
same as Option 29

Option 31: G Input Levels
same as Option 29

Option 32: SI Input Levels
same as Option 29

Option 33: $\overline{\text{RESET}}$ Input
- = 0: Schmitt trigger input
- = 1: standard TTL input levels
- = 2: higher voltage input levels

Option 34: CKO Input Levels
(CKO = input; Option 2 = 2,3)
same as Option 29

Option 35: Internal Initialization Logic
- = 0: Enabled
- = 1: Disable

Option 36: COP Bonding
- = 0: COP420L (28-pin device)
- = 1: COP421L (24-pin device)
- = 2: 28- and 24-pin versions
- = 3: COP422L (20-pin device)
- = 4: 28- and 20-pin versions
- = 5: 24- and 20-pin versions
- = 6: 28-, 24-, and 20-pin versions

Option 36: Internal Initialization Logic
- = 0: normal operation
- = 1: no internal initialization logic

COP420H/COP421H/COP422H Option Table

Please fill out the Option List and send it with the EPROM.

Option Data

OPTION 1 VALUE = _____ IS: GROUND PIN
OPTION 2 VALUE = _____ IS: CKO OUTPUT
OPTION 3 VALUE = _____ IS: CKI INPUT
OPTION 4 VALUE = _____ IS: RESET INPUT
OPTION 5 VALUE = _____ IS: L (7) DRIVER
OPTION 6 VALUE = _____ IS: L (6) DRIVER
OPTION 7 VALUE = _____ IS: L (5) DRIVER
OPTION 8 VALUE = _____ IS: L (4) DRIVER
OPTION 9 VALUE = _____ IS: IN1 INPUT
OPTION 10 VALUE = _____ IS: IN2 INPUT
OPTION 11 VALUE = _____ IS: VCC PIN
OPTION 12 VALUE = _____ IS: L (3) DRIVER
OPTION 13 VALUE = _____ IS: L (2) DRIVER
OPTION 14 VALUE = _____ IS: L (1) DRIVER
OPTION 15 VALUE = _____ IS: L (0) DRIVER
OPTION 16 VALUE = _____ IS: SI INPUT
OPTION 17 VALUE = _____ IS: SO DRIVER
OPTION 18 VALUE = _____ IS: SK DRIVER
OPTION 19 VALUE = _____ IS: IN0 INPUT
OPTION 20 VALUE = _____ IS: IN3 INPUT
OPTION 21 VALUE = _____ IS: G0 I/O PORT
OPTION 22 VALUE = _____ IS: G1 I/O PORT
OPTION 23 VALUE = _____ IS: G2 I/O PORT
OPTION 24 VALUE = _____ IS: G3 I/O PORT
OPTION 25 VALUE = _____ IS: D3 OUTPUT
OPTION 26 VALUE = _____ IS: D2 OUTPUT
OPTION 27 VALUE = _____ IS: D1 OUTPUT
OPTION 28 VALUE = _____ IS: D0 OUTPUT
OPTION 29 VALUE = _____ IS: L INPUT LEVELS
OPTION 30 VALUE = _____ IS: IN INPUT LEVELS
OPTION 31 VALUE = _____ IS: G INPUT LEVELS
OPTION 32 VALUE = _____ IS: SI INPUT LEVELS
OPTION 33 VALUE = _____ IS: RESET INPUT
OPTION 34 VALUE = _____ IS: CKO INPUT LEVELS
OPTION 35 VALUE = _____ IS: INTERNAL INITIALIZATION LOGIC
OPTION 36 VALUE = _____ IS: COP BONDING

Development Support

The MOLE (Microcontroller On Line Emulator) is a low cost development system and real time emulator for COPS' products. They also include TMP, 8050 and the new 16-bit HPC microcontroller family. The MOLE provides effective support for the development of both software and hardware in the user's application.

The purpose of the MOLE is to provide a tool to write and assemble code, emulate code for the target microcontroller and assist in debugging of the system.

The MOLE can be connected to various hosts, IBM PC, STARPLEX™, Kaypro, Apple and Intel systems, via RS-232 port. This link facilitates the up loading/down loading of code, supports host assembly and mass storage.

The MOLE consists of three parts; brain, personality and optional host software.

The brain board is the computing engine of the system. It is a self-contained computer with its own firmware which provides for all system operation, emulation control, communication, from programming and diagnostic operation. It has three serial ports which can be connected to a terminal, host system, printer, modem or to other MOLE's in a multi-MOLE environment.

The personality board contains the necessary hardware and firmware needed to emulate the target microcontroller. The emulation cable which replaces the target controller attaches to this board. The software contains a cross assembler and a communications program for up loading and down loading code from the MOLE.

MOLE Ordering Information

P/N	Description
MOLE-BRAIN	MOLE Computer Board
MOLE-COPS-PB1	COPS Personality Board
MOLE-XXX-YYY	Optional Software

Where XXX = COPS
YYY = Host System, IBM, Apple, KAY (Kaypro), CP/M

COPS Programming Manual

For detailed information on writing COPS programs, the COPS Programming Manual 424410284-001 provides an in-depth discussion of the COPS architecture, instruction set and general techniques of COPS programming. This manual is written with the programmer in mind.