STANDARD MICROSYSTEMS CORPORATION
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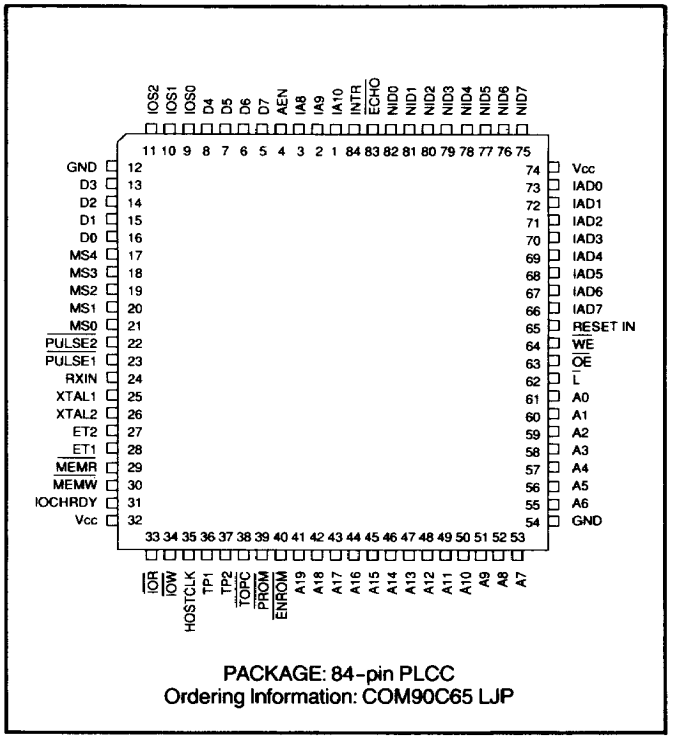
COM90C65
PRELIMINARY

Local Area Network Controller/ Transceiver/Support Logic

FEATURES:

- ☐ ARCNET® LAN Controller/Transceiver/Support Logic
- ☐ Combines SMC COM90C26/COM91C32/COM90C19
- ☐ Includes IBM® PC Bus Interface Circuitry
- ☐ Compatible with the SMC HYC9058 (HIT), HYC9068 (LAND), and HYC9088 (Twisted Pair LAN Driver)
- ☐ 2.5 Mbps Data Rate
- ☐ Token Passing Protocol
- ☐ Self Reconfiguration
- ☐ Variable Data Length Packets
- ☐ 16 Bits CRC Check/Generation
- ☐ Includes Address Decoding Circuitry for RAM, PROM and I/O
- ☐ Supports up to 255 Nodes
- ☐ Generates Interrupt Signals
- ☐ Addresses 2K RAM Buffer
- ☐ Arbitrates Buffer Access
- ☐ Allows Broadcast Messages
- ☐ Compatible with Broadband/Baseband Systems
- ☐ Compatible with Various Media (Twisted pair, Coax...)
- ☐ Compatible with Various Topologies (Star, Tree, Bus...)
- ☐ On Board Crystal Oscillator and Reset Circuitry
- ☐ Low Power CMOS, Single +5V Supply

PIN CONFIGURATION



PACKAGE: 84-pin PLCC
Ordering Information: COM90C65 LJP

GENERAL DESCRIPTION

The COM90C65 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET Local Area Network. The ARCNET Local Area Network is a token passing network operating at a 2.5 Mbps data rate. A token passing protocol provides predictable response times. Each network event occurs within a known time interval. Throughput can be reliably predetermined based upon the number of nodes and their expected traffic.

The COM90C65 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM90C65 establishes the network configuration and automatically reconfigures the token passing order as new nodes are added or deleted from the network.

The COM90C65 performs address recognition, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM90C65 interfaces directly to the host processor through a standard address and data bus.

An external 2K × 8 RAM buffer is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM90C65. The processor can write commands to the COM90C65 and also read status. The COM90C65 provides all of the signals necessary to allow smooth arbitration of all RAM buffer operations.

Additionally, the COM90C65 incorporates all the support logic circuitry provided for by the COM90C19 and all the clock generation functions, line drive signals and receive data conversion circuits of the COM91C32. This high level of integration further reduces ARCNET LAN node chip count, therefore minimizing costs.

*ARCNET is a registered trademark of the Datapoint Corporation.
IBM is a registered trademark of International Business Machines Corporation.

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DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	NAME	SYMBOL	DESCRIPTION
PROCESSOR INTERFACE			
51-53, 55-61	Address 9-7, Address 6-0	A9-A7 A6-A0	Input. These signals are connected to the address lines of the host processor. A0-A7 are used by the COM90C65 to generate the multiplexed address lines (IAD0-IAD7) during host accesses to the 2K x 8 RAM buffer. A4-A9 are used by the I/O decoder.
41-50	Address 19-10	A19-A10	Input. These signals are connected to the address lines of the host processor. A11-A19 are used by the memory decoder.
5-8, 13-16	Data 7-4, Data 3-0	D7-D4, D3-D0	Input/Output. These signals are connected to the data bus of the host microprocessor. They are used by the host to transmit data to and from the COM90C65 and are connected to internal pull-up resistors.
38	Data Bus Direction Control	$\overline{\text{TOPC}}$	Output. This active low signal controls the data bus transceiver. When this signal is high, data gets sent from the PC to the COM90C65. When this signal is low, data gets sent from the COM90C65 to the PC, and from PROM to the PC if the $\overline{\text{PROM}}$ signal is also low.
31	I/O Channel Ready	IOCHRDY	Output. This active high signal tells the host that the COM90C65 is ready for the intended operation. This signal is triggered by an I/O or a memory read or write operation.
4	Address Enable	AEN	Input. This signal, when low, acts as a qualifier for I/O Address Selection.
33	I/O Read	$\overline{\text{IOR}}$	Input. This active low signal is issued by the host microprocessor to indicate an I/O Read operation. A low pulse on this input when the COM90C65 is accessed enables data from the internal registers of the COM90C65 onto the Data Bus to be read by the host.
34	I/O Write	$\overline{\text{IOW}}$	Input. This active low signal is issued by the host microprocessor to indicate an I/O Write operation. A low pulse on this input when the COM90C65 is accessed enables data from the Data Bus to be written into the internal registers of the COM90C65.
29	Memory Read	$\overline{\text{MEMR}}$	Input. This active low signal is issued by the host microprocessor to indicate a Memory Read operation. A low pulse on this input when the COM90C65 is accessed enables data from the RAM or the PROM onto the Data Bus to be read by the host.
30	Memory Write	$\overline{\text{MEMW}}$	Input. This active low signal is issued by the host microprocessor to indicate a Memory Write operation. A low pulse on this input when the COM90C65 is accessed enables data from the Data Bus to be written into the RAM.
65	Reset In	RESET IN	Input. This active high signal is the power on reset signal from the host. It is used to activate the internal resets within the COM90C65.
40	ROM Enable	$\overline{\text{ENROM}}$	Input. This active low signal enables the decoding of the 8K PROM. This signal is connected to an internal pull-up resistor.
35	Host Clock	HOST CLK	Input. This signal is the clock pulse input from the host computer. It is used to generate the IOCHRDY signal during PROM access cycles.
84	Interrupt Request	INTR	Output. This active high signal is produced by the COM90C65 when an enabled interrupt condition occurs. INTR returns to its inactive state by resetting the interrupting status condition or the corresponding interrupt mask bit.
MEMORY INTERFACE			
1-3	Interface Address 10-8	IA10-IA8	Output. These signals issued by the COM90C65 are the three most significant bits of the RAM buffer address. They are active when either $\overline{\text{WE}}$ or $\overline{\text{OE}}$ is low and are otherwise in a tri-state condition. IA9 and IA10 will take on the value nn and should be viewed as page select bits. For packets less than 256 bytes, a 1K buffer can be used with IA8 unconnected. For packets greater than 256 bytes, a 2K buffer is needed with IA8 connected. These signals are connected to internal pull-up resistors
66-73	Interface Address/ Data 7-0	IAD7-IAD0	Input/Output. These signals are the means of communication when the RAM is accessed by either the host or the COM90C65. The COM90C65 converts the host's non-multiplexed address and data busses into these multiplexed 8 bits and latches them internally. These signals are connected to internal pull-up resistors.
62	Latch	$\overline{\text{L}}$	Output. This active low signal issued by the COM90C65 latches the IAD0-IAD7 lines onto the external LS373, which then feeds the lower 8 address bits of the RAM buffer during RAM access cycles.
64	Write Enable	$\overline{\text{WE}}$	Output. This active low signal issued by the COM90C65 enables the RAM buffer to input data from the Interface Address/Data Bus (IAD0-IAD7).
63	Output Enable	$\overline{\text{OE}}$	Ouput. This active low signal enables the external RAM buffer to output data to the Interface Address/Data Bus (IAD0-IAD7) during the data valid portion of all RAM buffer read operations.

DESCRIPTION OF PIN FUNCTIONS (CONTINUED)

PLCC PIN NO.	NAME	SYMBOL	DESCRIPTION
TRANSMISSION MEDIA INTERFACE			
39	ROM Select	$\overline{\text{PROM}}$	Output. This active low signal issued by the COM90C65 is used to enable the ROM chip.
22 23	Pulse 2 Pulse 1	$\overline{\text{PULSE2}}$ $\overline{\text{PULSE1}}$	Output. These active low signals carry the transmit data information, which is encoded in pulse format, from the COM90C65 to the LAN Driver.
24	Receive In	RXIN	Input. This signal carries the receive data information from the LAN Driver to the COM90C65.
MISCELLANEOUS			
17-21	Memory Base Address Select	MS4- MS0	Input. These signals are generated by external switches. They are used by the memory decoder to select a 16K block of memory. These signals are connected to internal pull-up resistors.
9-11	I/O Base Address Select	IOS0- IOS2	Input. These signals are generated by external switches. They are used by the I/O decoder to select a block of 16 I/O locations. These signals are connected to internal pull-up resistors.
75-82	Node ID Select	NID7- NID0	Input. These signals are generated by external switches. The node ID code represents the node identification of this particular COM90C65. These signals are connected to internal pull-up resistors.
27, 28	Extended Timeout Function 2, 1	ET2, ET1	Input. These signals are used to select timeout durations which are specified by the levels they are connected to. They are used by the COM90C65 in its network protocol. For standard ARCNET usage, make no connections to these pins. These signals are connected to internal pull-up resistors.
83	Echo Diagnostic Enable	$\overline{\text{ECHO}}$	Make no connection to this pin. This signal is connected to an internal pull-up resistor.
36	Test Point 1	TP1	This pin should be connected to ground. It is connected to an internal pull-up resistor.
37	Test Point 2	TP2	Make no connection to this pin. This signal is connected to an internal pull-up resistor.
25, 26	Crystal 1, Crystal 2	XTAL1, XTAL2	An external 20 MHz crystal should be connected to these pins. If an external 20 MHz TTL clock is used instead, it should be connected to XTAL1 with a 390 Ohm pull-up resistor and XTAL2 should be left floating.
32, 74	Power Supply	VCC	+5 V Power Supply pins.
12, 54	Ground	GND	Ground pins.

PROTOCOL DESCRIPTION

LINE PROTOCOL

The line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte takes up exactly 11 clock intervals with a single clock interval being 400 nS in duration. As a result, one byte is transmitted every 4.4 μS and the time to transmit a message can be precisely determined. The line idles in a spacing (logic "0") condition. A logic "0" is defined as no line activity and a logic "1" is defined as a pulse of 200 nS duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic "1"). Eight bit data characters are then sent with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be performed as described below:

Invitations To Transmit

An Invitation To Transmit is used to pass the token from one node to another and is sent by the following sequence:

- An ALERT BURST
- An EOT (End Of Transmission—ASCII code 04 HEX)
- Two (repeated) DID (Destination IDentification) characters

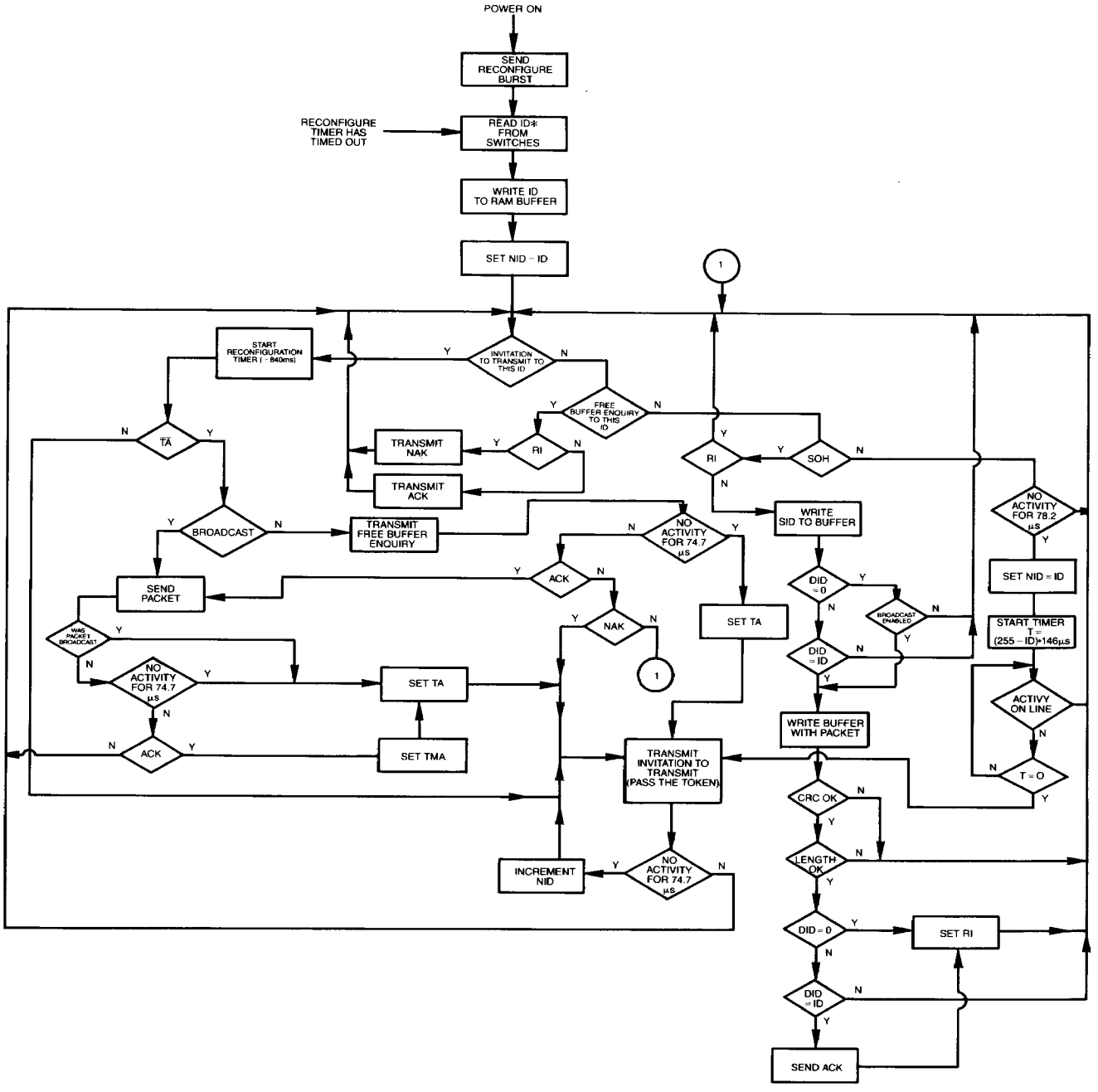
ALERT BURST	EOT	DID	DID

Free Buffer Enquiries

A Free Buffer Enquiry is used to ask another node if it is able to accept a packet of data and is sent by the following sequence:

- An ALERT BURST
- An ENQ (ENQuiry—ASCII code 85 HEX)
- Two (repeated) DID (Destination IDentification) characters

ALERT BURST	ENQ	DID	DID



* The ID set by the external switches is continually sampled during COM90C65 operation.
- ID refers to the identification number of the ID assigned to this node.
- NID refers to the next identification number that receives the token after this ID passes it.
- SID = source identification
- DID = destination identification
- SOH = start of header character; preceeds all data packets

FIGURE 1 - COM90C65 OPERATION

Data Packets

A Data Packet consists of the actual data being sent to another node and is sent by the following sequence:

- An ALERT BURST
- An SOH (Start Of Header—ASCII code 01 HEX)
- An SID (Source IDentification) character
- Two (repeated) DID (Destination IDentification) characters
- A single COUNT character which is the 2's complement of the number of data bytes to follow if a "short packet" is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a "long packet" is being sent
- N data bytes where COUNT = 256 - N (or 512 - N for a "long packet")
- Two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

ALERT BURST	SOH	SID	DID	DID	COUNT	data	data	CRC	CRC

Acknowledgements

An Acknowledgement is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- An ACK (ACKnowledgement—ASCII code 86 HEX) character

ALERT BURST	ACK

Negative Acknowledgements

A Negative Acknowledgement is used as a negative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- A NAK (Negative AcKnowledgement—ASCII code 15 HEX) character

ALERT BURST	NAK

NETWORK PROTOCOL

Communication on the network is based on a token passing protocol. Establishment of the network configuration and management of the network protocol are handled entirely by the COM90C65's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer, and issuing a command to enable the transmitter. When the COM90C65 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16 bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will verify the packet. If the packet is received successfully, the receiving node transmits an ACKnowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicate successful or unsuccessful delivery of the packet. An interrupt mask permits the COM90C65 to generate an interrupt to the processor when selected status bits become true. Figure 1 is a flow chart illustrating the internal operation of the COM90C65.

NETWORK RECONFIGURATION

A significant advantage of the COM90C65 is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated, a NETWORK RECONFIGURATION is performed. When a new COM90C65 is turned on (creating a new active node on the network), or if the COM90C65 has not received an INVITATION TO TRANSMIT for 840 mS, it causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line. It also provides line activity which allows the COM90C65 sending the INVITATION TO TRANSMIT to release control of the line.

When any COM90C65 senses an idle line for greater than 78.2 μS, which will only occur when the token is lost, each COM90C65 starts an internal timeout equal to 146 μS times the quantity 255 minus its own ID. It also sets the internally stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM90C65 starts sending INVITATION TO TRANSMIT with the Destination ID (DID) equal to the currently stored NID. Within a given network, only one COM90C65 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM90C65 waits for activity on the line. If there is no activity for 74.7 μS, the COM90C65 increments the NID value and transmits another INVITATION TO TRANSMIT using the new NID equal to the DID. If activity appears before the 74.7 μS timeout expires, the COM90C65 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible ID's. Each COM90C65 on the network will finally have saved a NID value equal to the ID of the COM90C65 that it released control to. At this point, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT being sent to ID's not on the network, until the next NETWORK RECONFIGURATION occurs. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will timeout and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propogation delay between nodes, and the highest ID number on the network, but will be in the range of 24 to 61 mS.

BROADCAST MESSAGES

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the DID equal to zero. Figure 8 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most significant bit of the ENABLE RECEIVE TO PAGE nn command (see Table 5) to a logic "0".

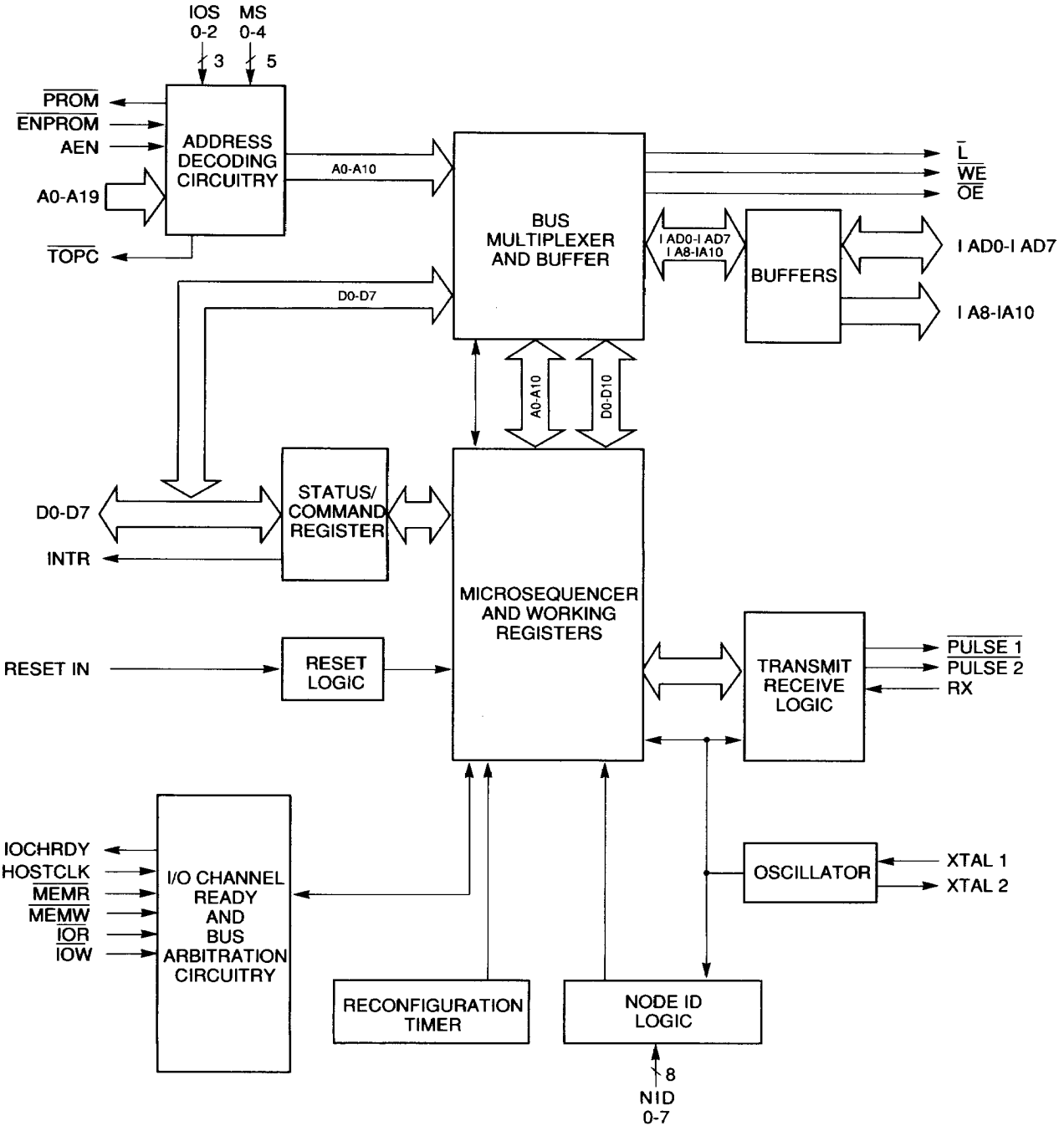


FIGURE 2 - INTERNAL BLOCK DIAGRAM

EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM90C65 operation.

Response Time

The Response Time is equal to the round trip propagation delay between the two furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM90C65 to start sending a message in response to a received message) which is approximately 12 μS. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 31 μS translates to a distance of about 4 miles. The flow chart in figure 1 uses a value of 74.7 μS (31 + 31 + 12 + margin) to determine if any node will respond.

Idle Time

The Idle Time is associated with a NETWORK RECONFIGURATION. Figure 4 illustrates that during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 78 μS. This 78 μS is equal to the Response Time of 74.7 μS plus the time it takes the COM90C65 to retransmit another message (usually another INVITATION TO TRANSMIT). The actual timeout is set to 78.2 μS to allow for margin.

Reconfiguration Time

If any node does not receive the token within the Reconfiguration Time, the node will initiate a NETWORK RECONFIGURATION.

The ET2 and ET1 inputs allow the network to operate over longer distances than the 4 miles stated earlier. DC levels on these inputs control the maximum distances over which the COM90C65 can operate by controlling the three timeout values described above. Table 1 illustrated the response time and reconfiguration time as a function of the ET2 and ET1 inputs. It should be noted that for proper network operation, all COM90C65s connected to the same network must have the same Response Time, Idle Time, and Reconfiguration Time.

Table 1
COM90C65 Internal Programmable Timer Values

ET2	ET1	Response Time (μS)	Idle Time (μS)	Reconfiguration Time (mS)
0	0	1130	1237	1680
0	1	563	624	1680
1	0	285	316	1680
1	1	78	86	840

SYSTEM DESCRIPTION

The System Block Diagram shown in figure 7 illustrates a typical implementation of an ARCNET node using the COM90C65. The only external components required to complete an ARCNET node design are a 2K x 8 static RAM, an octal latch, and the transmission media interface circuitry. This eliminates the need for space consuming and costly hardware which would otherwise be required to implement a node. The COM90C65 provides for simple interfacing to each of the three sections of the ARCNET system, namely the microprocessor, the transmission media and the static RAM.

MICROPROCESSOR INTERFACE

The left half of figure 7 illustrates a typical COM90C65 interface to the microprocessor. It consists of a 20 bit address bus, an 8 bit data bus, and a control bus. All accesses to the 2K x 8 RAM buffer, the optional PROM, and the internal registers of the COM90C65 are controlled by the COM90C65. Memory accesses are initiated by activating the $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ signals, while I/O accesses are initiated by activating the $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ signals.

The microprocessor's address lines are directly connected to the COM90C65. The address decoding circuitry of the COM90C65 monitors the address bus to determine valid accesses to the chip.

The microprocessor's data lines may be directly connected to the COM90C65. When interfacing to a high current driving data bus such as the IBM PC data bus, an octal bus transceiver should be used. The COM90C65 provides the $\overline{\text{TOPC}}$ signal to control the external transceiver. During RAM accesses, the address bus and data bus of the microprocessor are multiplexed within the COM90C65 and are fed through the IAD lines of the chip.

The microprocessor's control bus is directly connected to the COM90C65 and is used to inform the chip of the types of microprocessor access cycles which are occurring. The COM90C65 synchronizes all of the access cycles through the use of the IOCHRDY signal.

TRANSMISSION MEDIA INTERFACE

The right half of figure 7 illustrates the COM90C65 interface to the transmission media used to connect the node to the network. Either the HYC9058, the HYC9068, or the HYC9088 may be used to drive the media. During transmission, the COM90C65 transmits a logic "1" by generating two 100 nS non-overlapping negative pulses, $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$. These signals are sent to the LAN Driver, which in turn creates a 200 nS dipulse signal on the media. A logic "0" is transmitted by the absence of the two negative pulses, that is, the $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ outputs remain high, therefore there is an absence of a dipulse. During reception, the 200 nS dipulse appearing on the media is coupled through the RF transformer of the LAN Driver. A positive pulse at the RXIN pin of the COM90C65 is interpreted as a logic "1". Again, if no dipulse is present, the COM90C65 interprets a logic "0".

Typically, RXIN pulses occur at multiples of 400 nS. The COM90C65 can tolerate distortion of plus and minus 100 nS and still correctly capture the RXIN pulses.

During Reset, the transmitter portion of the COM90C65 is disabled and the $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ pins are inactive high.

RAM INTERFACE

The upper portion of figure 7 illustrates a typical COM90C65 interface to RAM. The RAM buffer is shared between the host microprocessor and the COM90C65's internal microsequencer and is used to hold incoming and outgoing data packets. There are two types of accesses to this buffer, namely, microprocessor initiated accesses and microsequencer initiated accesses. During microprocessor accesses, the COM90C65 multiplexes the address and data busses of the microprocessor onto the IAD lines. An external octal latch (74LS373) is used to hold the lower 8 bits of the addresses for the RAM. The COM90C65 generates the $\overline{\text{OE}}$ or $\overline{\text{WE}}$ signals to perform a read or write operation.

FUNCTIONAL DESCRIPTION

MICROSEQUENCER

The COM90C65 contains an internal microsequencer which performs all of the control operations necessary to carry out the ARCNET protocol. It consists of a clock generator, a 544 x 8 ROM, a program counter, two instruction registers, an instruction decoder, a noop generator, jump logic, and reconfiguration logic.

The COM90C65 derives a 5 MHz and a 2.5 MHz clock from the external crystal. These clocks provide the rate at which the instructions are executed within the COM90C65. The 5 MHz clock is the rate at which the program counter operates, while the 2.5 MHz clock is the rate at which the instructions are executed. The microprogram is stored in the ROM and the instructions are fetched and then placed into the instruction registers. One register holds the op code, while the other holds the immediate data. Once the instruction is fetched, it is decoded by the internal instruction decoder, at which point the COM90C65 proceeds to execute the instruction. When a noop instruction is encountered, the microsequencer enters a timed wait state, in which case the program counter is temporarily stopped until the wait state is complete. When a jump instruction is encountered, the program counter is loaded with the jump address from the ROM. The COM90C65 contains an internal reconfiguration timer which interrupts the microsequencer if it has timed out. At this point the program counter is loaded with the address containing the instruction to set the RECON status bit.

ADDRESS DECODING

The COM90C65 includes address decoding circuitry that compares the value of the address bus to the Memory Select (MS0-MS4) and I/O Select (IOS0-IOS2) pins in order to determine processor accesses to the on board PROM, RAM, and I/O locations. By placing switches on the MS0-MS4 and the IOS0-IOS2 pins, a user configures the Memory Map and I/O Map according to the possible address ranges shown in Tables 2 and 3.

Memory Address Decoding

This section is used to select a 16K block from the memory map of the processor for PROM and RAM accesses. Figure 3 illustrates how the memory selection works. The MS4-MS0 pins are decoded through a 5 To 9 Decoder to generate a 9-bit value. These 9 bits are compared to the A19-A11 lines of the address bus in order to select a particular 16K memory segment. Figure 5 illustrates a 16K block of memory that has been selected by the MS4-MS0 pins. The PROM occupies the upper 8K area of the selected 16K segment and is accessed when A13 = 1. The RAM occupies the lower 8K area and is accessed when A13 = 0. A11 and A12 are used to determine which 2K segment of the lower 8K area will be used for the RAM buffer.

The $\overline{\text{ENROM}}$ pin is used to enable decoding for the on board PROM. If $\overline{\text{ENROM}}$ is connected to a logic "1", the COM90C65 will not generate the $\overline{\text{PROM}}$ signal, the $\overline{\text{TOPC}}$ signal, or the IOCHRDY signal for accesses to the upper 8K area. In this configuration, the COM90C65 will only occupy a 2K segment of memory.

I/O Address Decoding

This section is used to select a block of 16 I/O locations from the I/O map of the processor. Figure 4 illustrates how the I/O selection process works. The IOS2-IOS0 pins are decoded through a 3 To 6 Decoder to generate a 6 bit value. These 6 bits are compared to the A9-A4 lines of the address bus in order to determine which block of 16 I/O locations will be used by the chip. Figure 6 illustrates the COM90C65 register map. All reserved locations should not be accessed.

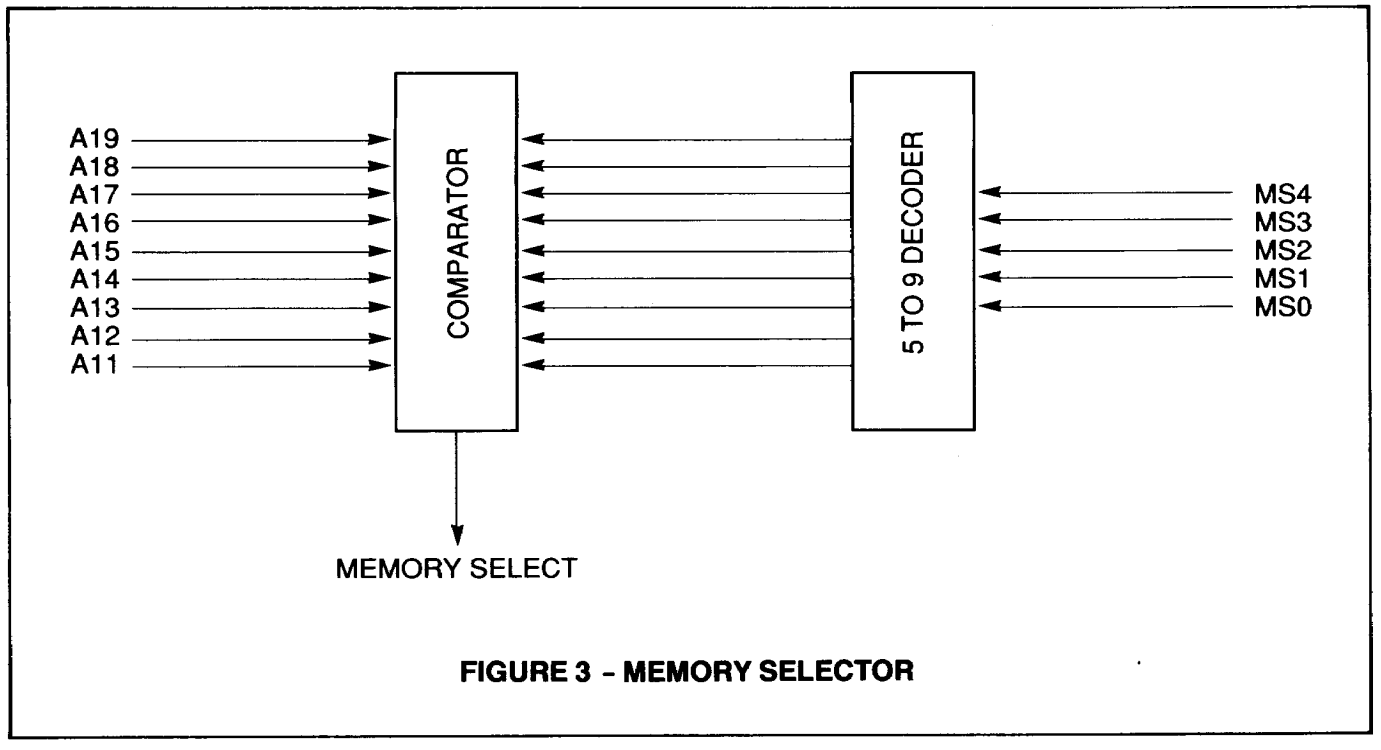


FIGURE 3 - MEMORY SELECTOR

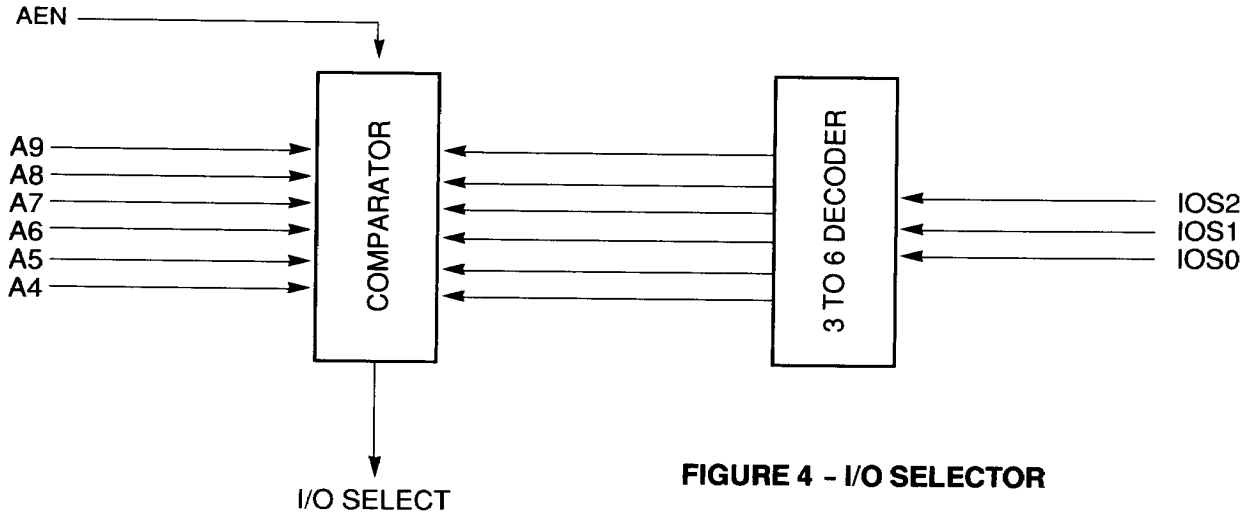


FIGURE 4 - I/O SELECTOR

Table 2 — User Configuration of Memory Map

MS4	MS3	MS2	MS1	MS0	RAM Address Range	PROM Address Range
0	0	0	0	0	C:0000-C:07FF	C:2000-C:3FFF
0	0	0	0	1	C:0800-C:0FFF	C:2000-C:3FFF
0	0	0	1	0	C:1000-C:17FF	C:2000-C:3FFF
0	0	0	1	1	C:1800-C:1FFF	C:2000-C:3FFF
0	0	1	0	0	C:4000-C:47FF	C:6000-C:7FFF
0	0	1	0	1	C:4800-C:4FFF	C:6000-C:7FFF
0	0	1	1	0	C:5000-C:57FF	C:6000-C:7FFF
0	0	1	1	1	C:5800-C:5FFF	C:6000-C:7FFF
0	1	0	0	0	C:C000-C:C7FF	C:E000-C:FFFF
0	1	0	0	1	C:C800-C:CFFF	C:E000-C:FFFF
0	1	0	1	0	C:D000-C:D7FF	C:E000-C:FFFF
0	1	0	1	1	C:D800-C:DFFF	C:E000-C:FFFF
0	1	1	0	0	D:0000-D:07FF	D:2000-D:3FFF
0	1	1	0	1	D:0800-D:0FFF	D:2000-D:3FFF
0	1	1	1	0	D:1000-D:17FF	D:2000-D:3FFF
0	1	1	1	1	D:1800-D:1FFF	D:2000-D:3FFF
1	0	0	0	0	D:4000-D:47FF	D:6000-D:7FFF
1	0	0	0	1	D:4800-D:4FFF	D:6000-D:7FFF
1	0	0	1	0	D:5000-D:57FF	D:6000-D:7FFF
1	0	0	1	1	D:5800-D:5FFF	D:6000-D:7FFF
1	0	1	0	0	D:8000-D:87FF	D:A000-D:BFFF
1	0	1	0	1	D:8800-D:8FFF	D:A000-D:BFFF
1	0	1	1	0	D:9000-D:97FF	D:A000-D:BFFF
1	0	1	1	1	D:9800-D:9FFF	D:A000-D:BFFF
1	1	0	0	0	D:C000-D:C7FF	D:E000-D:FFFF
1	1	0	0	1	D:C800-D:CFFF	D:E000-D:FFFF
1	1	0	1	0	D:D000-D:D7FF	D:E000-D:FFFF
1	1	0	1	1	D:D800-D:DFFF	D:E000-D:FFFF
1	1	1	0	0	E:0000-E:07FF	E:2000-E:3FFF
1	1	1	0	1	E:0800-E:0FFF	E:2000-E:3FFF
1	1	1	1	0	E:1000-E:17FF	E:2000-E:3FFF
1	1	1	1	1	E:1800-E:1FFF	E:2000-E:3FFF

Table 3 — User Configuration of I/O Map

IOS2	IOS1	IOS0	I/O Address Range
0	0	0	260-26F
0	0	1	290-29F
0	1	0	2E0-2EF
0	1	1	2F0-2FF
1	0	0	300-30F
1	0	1	350-35F
1	1	0	380-38F
1	1	1	3E0-3EF

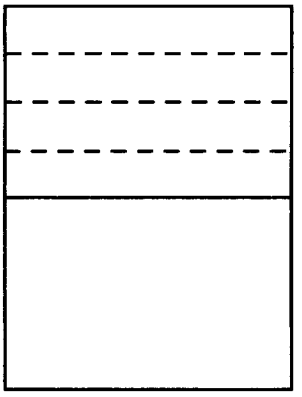


FIGURE 5
16K Memory Segment chosen by MS0-MS4

Address	READ	WRITE
00	Status Register	Interrupt Mask
01	RESERVED	Command Register
02	RESERVED	
03	RESERVED	
04	RESERVED	
05	RESERVED	
06	RESERVED	
07	RESERVED	
08	RESET	
09	RESET	
0A	RESET	
0B	RESET	
0C	RESERVED	
0D	RESERVED	
0E	RESERVED	
0F	RESERVED	

FIGURE 6 — REGISTER MAP

INTERNAL REGISTERS

The COM90C65 contains four internal registers which may be accessed by the microprocessor. They are the Status Register, the Command Register, the Interrupt Mask Register, and the Reset Register.

Status Register

The COM90C65 Status Register is an 8 bit read-only register which can be accessed by the microprocessor. The Status Register contents are defined as in Table 4:

Table 4 — Status Register

BIT	NAME	SYMBOL	DESCRIPTION
7	Receiver Inhibited	RI	This bit, if high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. No messages will be received until this command is issued, and once the message has been received, the RI bit gets set, thereby inhibiting the receiver. The RI bit is cleared by issuing an ENABLE RECEIVE TO PAGE nn command. This bit, when set, will cause an interrupt if the corresponding bit in the Interrupt Mask Register is also set.

Table 4 — Status Register

BIT	NAME	SYMBOL	DESCRIPTION
6	Extended Timeout Status 2	ETS2	This bit reflects the current logic value tied to the ET2 input pin (pin 27).
5	Extended Timeout Status 1	ETS1	This bit reflects the current logic value tied to the ET1 input pin (pin 28).
4	Power On Reset	POR	This bit, if high, indicates that the COM90C65 has been reset by either a software or a hardware reset. The POR bit is cleared by the CLEAR FLAGS command. This bit, when set, will cause a non-maskable interrupt.
3	Test	TEST	This bit is intended for test and diagnostic purposes. It is a logic zero under any normal operating conditions.
2	Reconfiguration	RECON	This bit, if high, indicates that the reconfiguration timer has timed out because the RXIN pin (pin 24) was idle for 78.2 μS. The RECON bit is cleared during a CLEAR FLAGS command. This bit, when set, will cause an interrupt if the corresponding bit in the Interrupt Mask Register is also set.
1	Transmitter Message Acknowledged	TMA	This bit, if high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast messages are never acknowledged. The TMA bit is cleared by issuing the ENABLE TRANSMIT FROM PAGE nn command.
0	Transmitter Available	TA	This bit, if high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of an ENABLE TRANSMIT FROM PAGE nn command or upon execution of a DISABLE TRANSMITTER command. The TA bit is cleared by issuing the ENABLE TRANSMIT FROM PAGE nn command. This bit, when set, will cause an interrupt if the corresponding bit in the Interrupt Mask Register is also set.

Command Register

Execution of the following commands are initiated by performing a processor I/O write with the written data defining the commands listed in Table 5. Any combinations of written data other than those listed in Table 5 are not permitted and can result in incorrect chip and/or network operation.

Table 5 — Command Register

WRITTEN DATA	COMMAND
00000000	Reserved for future use.
00000001	DISABLE TRANSMITTER—This command will cancel any pending transmit command (transmission that has not yet started) when the COM90C65 next receives the token. This command will set the TA (Transmitter Available) status bit to logic "1" when the token is received.
00000010	DISABLE RECEIVER—This command will cancel any pending receive command. If the COM90C65 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set to logic "1" the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.
000nn011	ENABLE TRANSMIT FROM PAGE nn—This command prepares the COM90C65 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are reset to logic "0". The TA bit is set to logic "1" upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM90C65 has received an acknowledgement from the destination node. This acknowledgement is strictly hardware level which is sent by the receiving node before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors. This implies that the TMA bit is not a guarantee of proper destination reception. Refer to figure 1 for details of the transmit sequence and its relation to the TA and TMA status bits.

Table 5 — Command Register

WRITTEN DATA	COMMAND
b00nn100	ENABLE RECEIVE TO PAGE nn—This command allows the COM90C65 to receive data packets into RAM buffer page nn and resets the RI status bit to logic "0". If "b" is high, the COM90C65 will also receive broadcast transmissions. A broadcast transmission is a transmission to ID zero. The RI status bit is set to logic "1" upon successful reception of a message.
0000c101	DEFINE CONFIGURATION—If "c" is a logic "1," the COM90C65 will handle long as well as short packets. If "c" is a logic "0," the COM90C65 will only handle short packets (less than 254 bytes).
000rp110	CLEAR FLAGS—If "p" is a logic "1," the POR status flag is reset to logic "0". If "r" is a logic "1," the RECON status flag is reset to logic "0".

Interrupt Mask Register

The COM90C65 is capable of generating an interrupt signal when certain status bits become true. A write to the Mask Register specifies which status bits will be enabled to generate the interrupt. The bit positions in the Mask Register are in the same position as their corresponding status bits in the Status Register, and a logic one in a particular bit position enables the corresponding interrupt. While the RI, RECON, and TA status bits are capable of generating an interrupt if enabled, the ETS2, ETS1 and TMA status bits will never cause an interrupt, and the POR status bit will cause a non-maskable interrupt regardless of the value of the corresponding Mask Register bit. The Mask Register takes on the following bit definition:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	X	X	X	X	RECON TIMER	X	TRANSMITTER AVAILABLE

The three maskable status bits are ANDed with their respective mask bits, and the results, along with the POR status bit, are ORed to produce the processor interrupt signal INTR. This signal returns to its inactive low state when either the interrupting status bit or the corresponding bit in the Mask Register is reset. To clear an interrupt generated as a result of a Power On Reset or Reconfiguration occurance, the CLEAR FLAGS command should be used. To clear an interrupt generated as a result of a completed transmission (TA) or a completed reception (RI), the corresponding mask bits should be reset.

Reset Register

The Reset Register consists of four I/O locations which are mapped at 8, 9, A, and B. Any time these locations are accessed by the microprocessor, a software reset is generated. Figure 6 illustrates the mapping of the Internal Registers of the COM90C65. For details on the Reset Logic, refer to the RESET LOGIC section of this document.

SOFTWARE INTERFACE

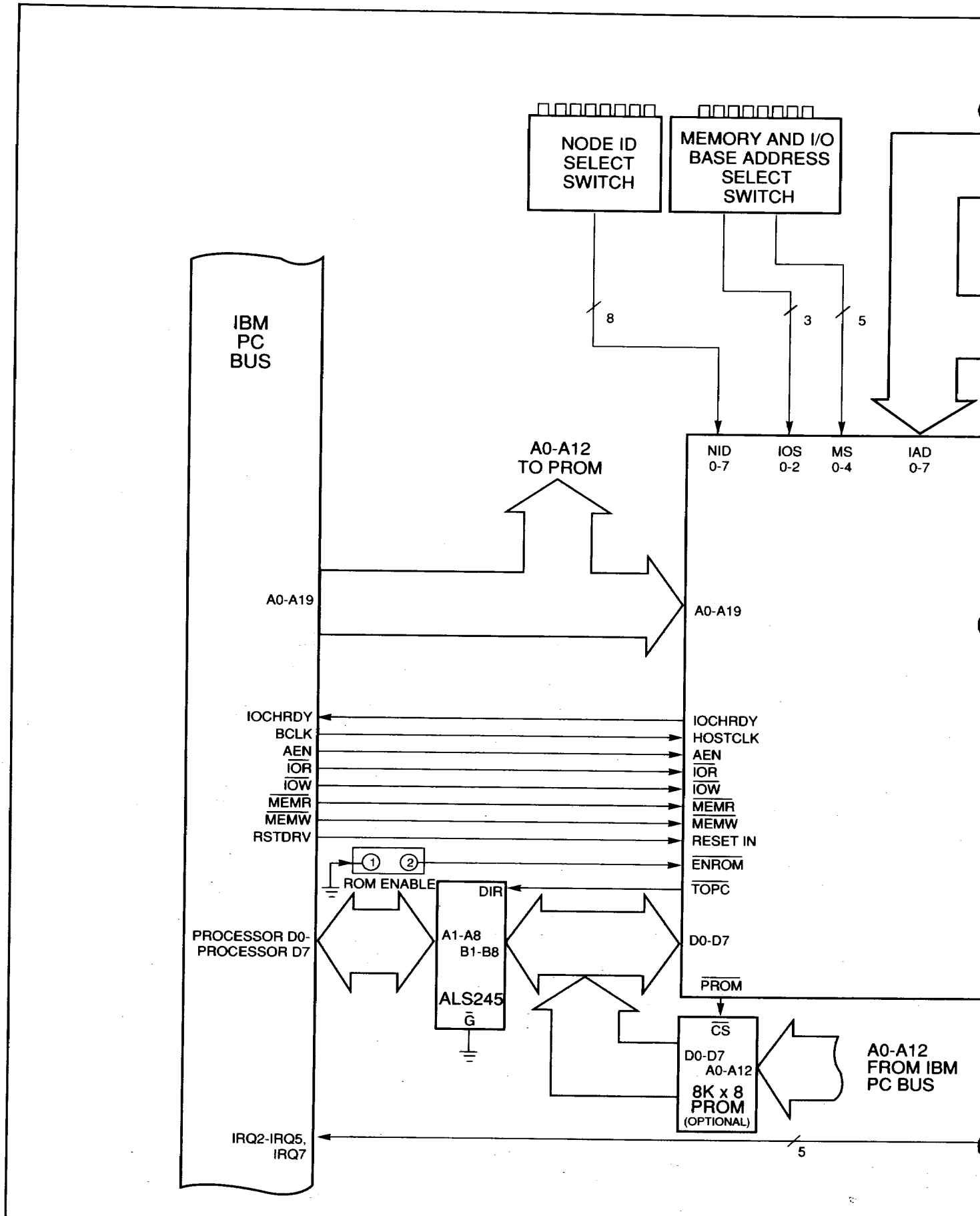
The microprocessor interfaces to the COM90C65 via software by accessing the Status, Command, Interrupt Mask, and Reset Registers. These actions were discussed in the Internal Registers section of this document. Additionally, it is necessary to know the details of how the Internal Registers are used in the transmit and receive sequences and to know how the RAM buffer is properly set up. The sequence of events that tie these actions together are discussed as follows.

Transmit Sequence

During a transmit sequence, the microprocessor selects a 256 or 512 byte segment of the RAM buffer and writes into it. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM90C65 interprets the packet as a long or short packet, depending on whether the content of the buffer address 2 is zero or non-zero. The format of the buffer is shown in figure 8. Address 0 contains the Source Identifier (SID), Address 1 contains the Destination Identifier (DID), and Address 2 contains, for short packets, the value 256-N, where N represents the message length, or for long packets, the value 0, indicating that it is indeed a long packet. In the latter case, Address 3 would contain the value 512-N, where N represents the message length. The SID in Address 0 is used by the receiving node to reply to the transmitting node. The COM90C65 puts the local ID in this location, therefore it is not necessary to write into this location.

Once the buffer is written into, the microprocessor awaits a logic "1" on the TA bit, indicating that a previous transmit command has concluded and another may be issued. Each time the message is loaded and a transmit command issued, it will take a variable amount of time before the message is transmitted, depending on the traffic on the network and the location of the token at the time the transmit command was issued. Typically, the conclusion of the transmit command, which is flagged when TA becomes a logic one, generates an interrupt. While waiting for the interrupt to occur, the processor may load another page into the RAM buffer with the next message to be sent in anticipation of the transmitter becoming available (TA becomes a logic "1"). In this way, double buffering is accomplished by loading a second message while the first message is being transmitted. The interrupt will then allow the software to time the repeated issuing of transmit commands.

Once the TA bit becomes a logic "1," the microprocessor issues the ENABLE TRANSMIT FROM PAGE nn command, which resets the TA and TMA bits to logic "0." If the message is not a BROADCAST, the COM90C65 automatically issues a FREE BUFFER ENQUIRY to the destination node in order to send the message. At this point, one of three possibilities may occur. The first possibility is if a free buffer is available at the destination node, in which case it responds with an ACKnowledgement. At this point, the COM90C65 fetches the data from the Transmit Buffer and performs the


NODE ID SELECT SWITCH
MEMORY AND I/O BASE ADDRESS SELECT SWITCH
8
3
5
IBM PC BUS
A0-A12 TO PROM
NID 0-7
IOS 0-2
MS 0-4
IAD 0-7
A0-A19
A0-A19
IOCHRDY
BCLK
AEN
IOR
IOW
MEMR
MEMW
RSTDRV
IOCHRDY
HOSTCLK
AEN
IOR
IOW
MEMR
MEMW
RESET IN
ENROM
TOPC
ROM ENABLE
DIR
A1-A8
B1-B8
ALS245
G
PROCESSOR D0-
PROCESSOR D7
D0-D7
PROM
CS
D0-D7
A0-A12
8K x 8
PROM
(OPTIONAL)
A0-A12
FROM IBM
PC BUS
IRQ2-IRQ5,
IRQ7
5

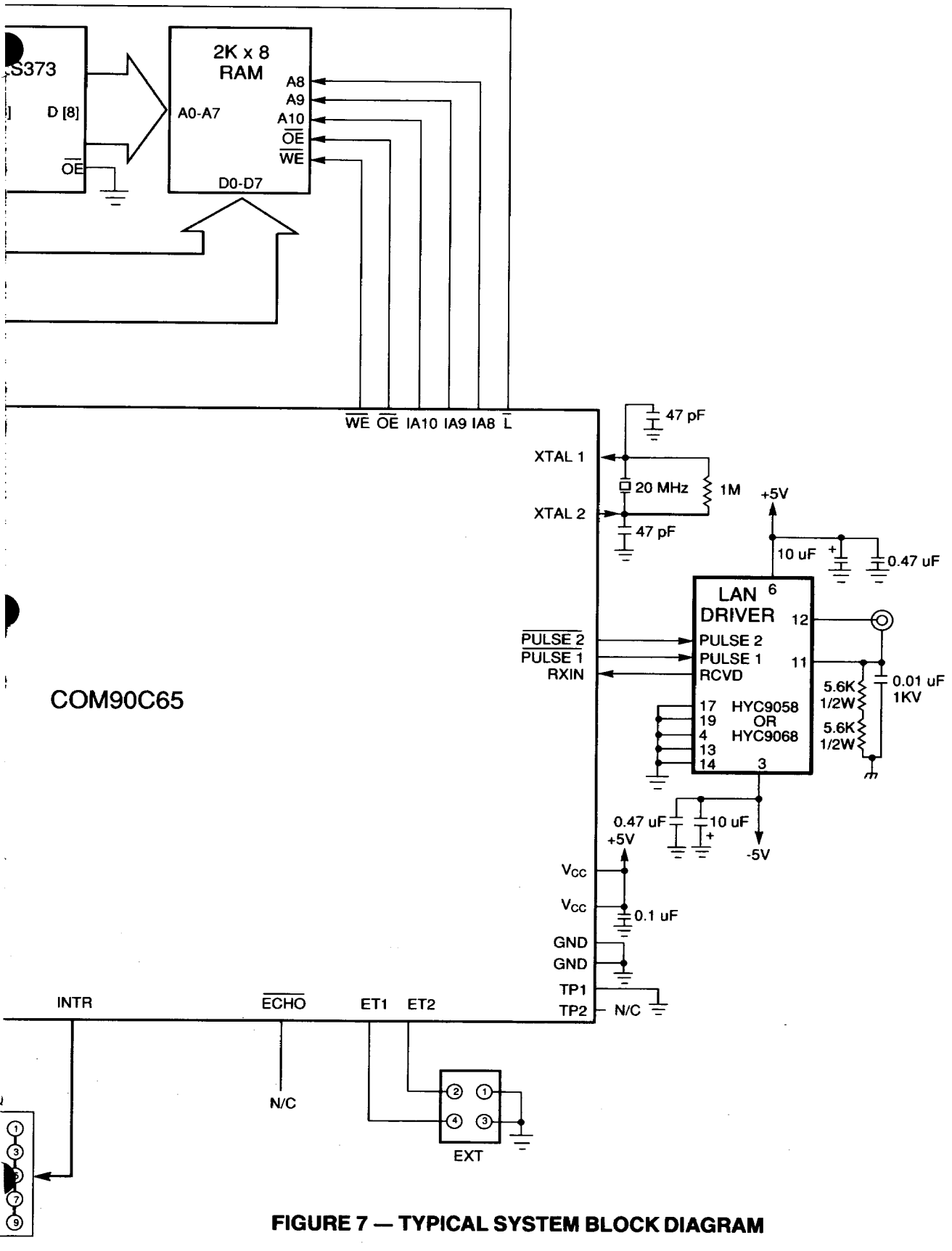


FIGURE 7 — TYPICAL SYSTEM BLOCK DIAGRAM

transmit sequence. After the transmit sequence is completed, the TMA bit and the TA bit are set to logic "1." The second possibility which may occur after a FREE BUFFER ENQUIRY is issued is if the destination node responds with a Negative AcKnowledgement. In this case, the RI bit of the destination node is set to a logic "1," the token is passed on from the transmitting node to the next node, and the TA bit is set to logic "1" in preparation for the next time the token is received, while the TMA bit remains at a logic "0." The third possibility which may occur after a FREE BUFFER ENQUIRY is issued is if no response is received from the destination node. In this case, a software timeout on the TA bit is used to tell the microprocessor to disable the transmitter via the DISABLE TRANSMITTER command. This causes the transmission to be abandoned and the TA bit to be set to a logic "1" when the node next receives the token, while the TMA bit remains at a logic "0." If the disable transmitter command does not cause the TA bit to be set in the time it takes the token to make a round trip through the network, one of three situations exists. Either the node is disconnected from the network, or there are no other active nodes on the network, or the external receive circuitry has failed. These situations can be determined by using another software timeout which is greater than the worst case time for a round trip token pass which occurs when all nodes transmit a maximum length message.

Receive Sequence

A receive sequence begins with the RI status bit becoming a logic "1," which indicates that a previous reception has concluded. The microprocessor will be interrupted if the corresponding bit in the Interrupt Mask Register is set to logic "1." Otherwise, it is the user's responsibility to have the microprocessor periodically check the Status Register. Once the microprocessor is alerted to the fact that the previous reception has concluded, it may issue the ENABLE RECEIVE TO PAGE nn command, which resets the RI bit to logic "0" and selects a new page in the RAM buffer. Again, the appropriate buffer size is specified in the DEFINE CONFIGURATION command. Typically, the page which just received the data packet will be read by the microprocessor at this point.

Once the ENABLE RECEIVE TO PAGE nn command is issued, the microprocessor attends to other duties. There is no way of telling how long the new reception will take, since another node may transmit a packet at any time. When another node does transmit a packet to this node, if the DEFINE CONFIGURATION command has enabled the reception of long packets, the COM90C65 interprets the packet as a long or short packet, depending on whether the content of the buffer location 002 is zero or non-zero. The format of the buffer is shown in figure 8. Address 0 contains the Source Identifier (SID), Address 1 contains the Destination Identifier (DID), and Address 2 contains, for short packets, the value 256-N, where N represents the message length, or for long packets, the value 0, indicating that it is indeed a long packet. In the latter case, Address 3 contains the value 512-N, where N represents the message length. Note that the COM90C65 deposits packets in the RAM buffer in the same format that the transmitting node arranged it, which allows for a message to be received and then retransmitted without rearranging any bytes in the RAM buffer. Once the packet is received and stored correctly in the selected buffer, the COM90C65 sets the RI bit to logic "1" to signal the microprocessor that the reception is complete.

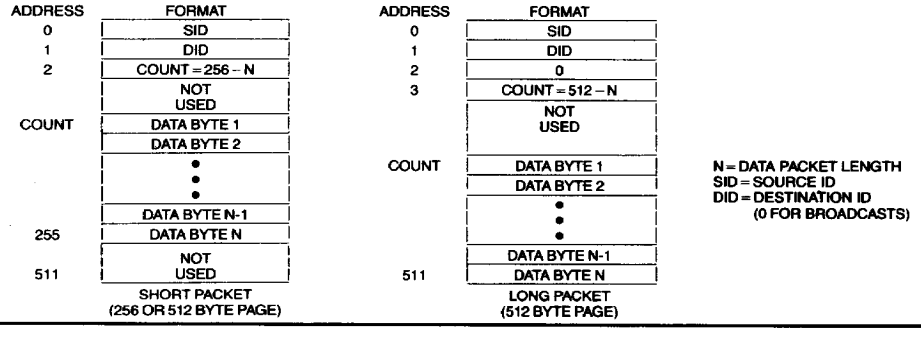
RESET LOGIC

An internal reset signal of pulse width equal to 102.4 μS is generated from either a hardware or a software reset. The hardware reset occurs when a high signal is asserted on the RESET IN input (pin 65). The minimum reset pulse width is 120 nS (or 2T+20 nS for crystal frequencies other than 20 MHz, where T = 1/f). A software reset is generated when the microprocessor accesses I/O locations 8, 9, A, or B. When the COM90C65 is reset, the following events take place. First, during the entire reset process, the transmitter portion of the COM90C65 will be disabled and the Status Register will assume the following state:

BIT 7	(RI)	= 1
BIT 6	(ETS2)	not affected
BIT 5	(ETS1)	not affected
BIT 4	(POR)	= 1
BIT 3	(TEST)	= 0
BIT 2	(RECON)	= 0
BIT 1	(TMA)	= 0
BIT 0	(TA)	= 1

Next, the Interrupt Mask Register will be cleared, that is, no maskable interrupts will be enabled. Page 00 will be selected for both the receive and the transmit RAM buffer. When the RESET IN signal occurs, the COM90C65 will generate an interrupt from the nonmaskable Power On Reset interrupt. The COM90C65 will start 102.4μs after the RESET IN signal is removed. At this time, the COM90C65, after reading its own ID, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and the address 01 HEX will be written with the ID number read from the Node

FIGURE 8 RAM BUFFER PACKET CONFIGURATION



ID Select Switch. The processor may then read RAM buffer address 01 to determine the COM90C65 ID. It should be noted that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

TRANSMIT/RECEIVE LOGIC

Figure 9 illustrates the events which occur in transmission or reception of data consisting of 1, 1, 0. The COM90C65, during transmission, produces two 100 nS nonoverlapping pulses on the $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ lines to indicate a logic "1," whereas a lack of pulses indicates a logic "0." The $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ signals are used to drive the HYC9058, the HYC9068 or the HYC9088, which in turn creates a 200 nS dipulse signal on the transmission media. During reception, each dipulse appearing on the transmission media is coupled through the RF transformer of the LAN Driver to produce a positive pulse on the RXIN pin. The pulse is captured by the COM90C65 and is then converted to NRZ data. Typically, RXIN pulses occur at multiples of 400 nS, although the COM90C65 can tolerate distortion of plus or minus 100 nS and still correctly capture and convert the RXIN pulses to NRZ format.

READ AND WRITE CYCLES

Microprocessor Read RAM Cycle

As stated in the Microprocessor Interface section of the System Description, all accesses to the RAM buffer are under the control of the COM90C65. Since the RAM buffer is shared between the host microprocessor and the COM90C65's microsequencer, the COM90C65's arbitration circuitry resolves contention between these two channels.

During a Microprocessor Read RAM Cycle (see Figure 10), the following sequence of events occurs. Immediately following the $\overline{\text{MEMR}}$ signal issued by the host microprocessor, the COM90C65 signals the host microprocessor to wait by deactivating the IOCHRDY signal, and activates the $\overline{\text{TOPC}}$ signal to provide the external LS245 with the data direction. While the host microprocessor is being waited, the COM90C65 performs a read RAM cycle by using the address provided by the host microprocessor. The COM90C65's read RAM cycle, which is controlled by an internal 5 MHz clock, consists of the following events. With the rising edge of the clock (time T1), a valid address from the host microprocessor appears on the IADO-7 and IA8-10 lines. The address on the IADO-7 lines gets latched onto the external LS373 by the $\overline{\text{L}}$ signal, which is triggered by the falling edge of the clock (time T2). Since the COM90C65 converts the non-multiplexed Address and Data busses of the microprocessor into the multiplexed IADO-7 lines, the next rising edge of the clock (time T3) causes the IADO-7 lines to become tri-state to allow data from the RAM onto the IADO-7 lines. With the next falling edge of the clock (time T4), the $\overline{\text{OE}}$ signal is generated by the COM90C65, which allows the data from the RAM onto the IADO-7 lines. 200 ns after the assertion of the $\overline{\text{OE}}$ signal (at time T6), the data on the IADO-7 lines is latched internally. At time T6, with the falling edge of the clock, the IOCHRDY signal becomes active, signaling the host to proceed with the Read RAM operation. The host microprocessor, at this time, completes the read operation by reading the internal data latch which holds the RAM information. The details of how the microprocessor completes the read operation are discussed in the Microprocessor Read RAM and I/O Cycle section. The following rising edge of the clock (time T7) causes both the $\overline{\text{L}}$ and the $\overline{\text{OE}}$ signals to become inactive. Some time later, the processor withdraws the $\overline{\text{MEMR}}$ signal, which causes the data bus to go into tristate and the $\overline{\text{TOPC}}$ signal to become inactive. Once the $\overline{\text{MEMR}}$ signal is withdrawn, the Microprocessor Read RAM cycle is complete.

Microprocessor Write RAM Cycle

During a Microprocessor Write RAM Cycle (see figure 11), much like the Read RAM Cycle explained above, the COM90C65 controls the operation. Immediately following the $\overline{\text{MEMW}}$ signal issued by the host microprocessor, the IOCHRDY signal becomes inactive, telling the microprocessor to wait. While the microprocessor is being waited, the COM90C65 addresses the correct location on the RAM and controls the entire write operation by using the address and data provided by the microprocessor. The $\overline{\text{TOPC}}$ signal remains at a high level during the entire cycle to provide the external LS245 with the data direction. The COM90C65's write RAM cycle, which is controlled by an internal 5 MHz clock, consists of the following events. At the rising edge of the internal clock (time T1 in figure 11), a valid address from the host microprocessor appears on the IADO-7 and IA8-10 lines. The address on the IADO-7 lines gets latched onto the external LS373 by the $\overline{\text{L}}$ signal, which is triggered by the falling edge of the clock (time T2). Since the COM90C65 converts the non-multiplexed Address and Data busses into the multiplexed IADO-7 lines, the next rising edge of the clock (time T3) causes the IADO-7 lines to be replaced with the data provided by the host microprocessor. At this point the $\overline{\text{WE}}$ signal is activated, which allows the data from the IADO-7 lines to be written into the RAM. The $\overline{\text{WE}}$ signal is withdrawn after 300 ns (at time T6), at which time the IOCHRDY signal is activated. At the following rising edge of the clock (time T7), the $\overline{\text{L}}$ signal is deactivated and the IADO-7 and IA8-10 lines become invalid. At this point, the microprocessor may withdraw the $\overline{\text{MEMW}}$ signal and the Microprocessor Write RAM Cycle is complete.

Microprocessor Read RAM and I/O Cycle

The microprocessor may read the COM90C65 for two purposes (see figure 12). One purpose, described above in the Microprocessor Read RAM Cycle section, is to empty a received data packet which was stored in RAM, in which case the microprocessor issues the $\overline{\text{MEMR}}$ command. The other purpose is to read the Status Register, in which case the microprocessor issues the $\overline{\text{IOR}}$ command. The $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ signal causes the immediate deactivation of the IOCHRDY signal, thereby signaling the microprocessor to wait, and causes the $\overline{\text{TOPC}}$ signal to become active. While the microprocessor is being waited, the COM90C65 fetches the information from either RAM or the Status Register, depending on the operation. The fetching of data from RAM was described in the Microprocessor Read RAM Cycle section and the fetching of information from the Status Register is done internally. Once the information is obtained, the COM90C65 signals the microprocessor to proceed with the operation by generating the IOCHRDY signal at time T6.

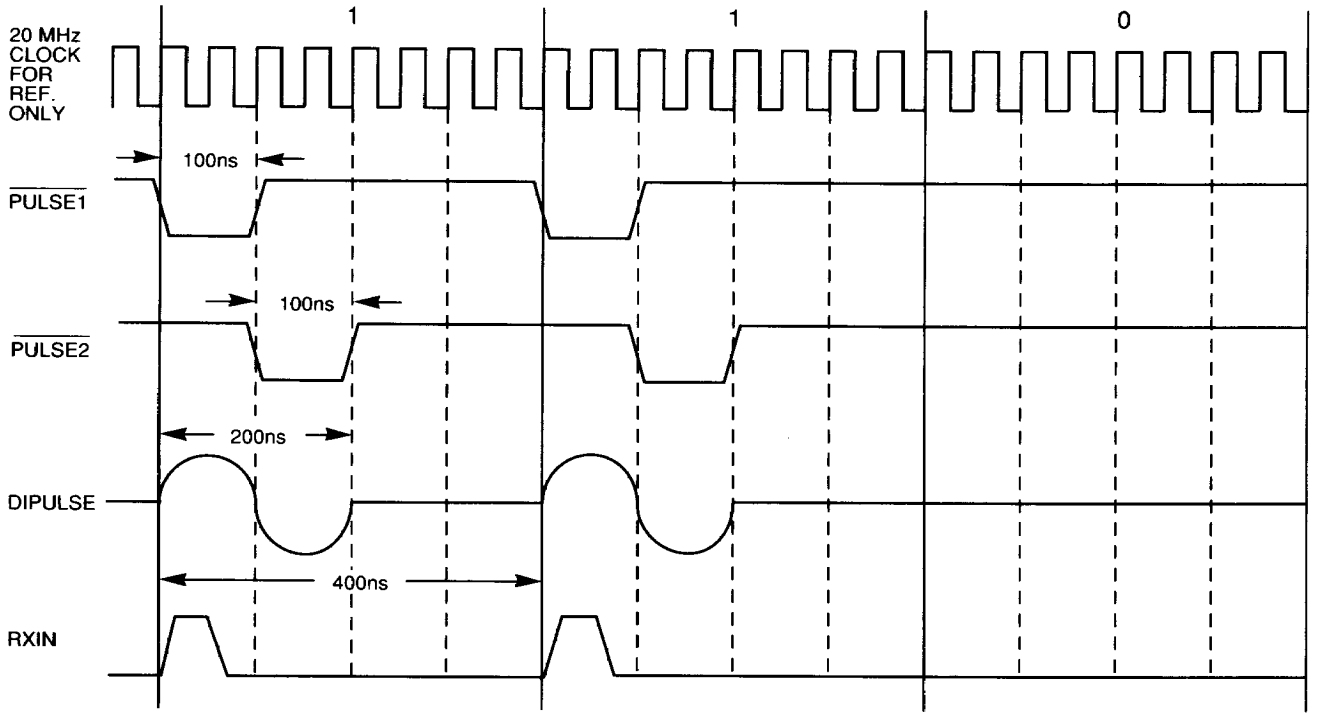


FIGURE 9 - DIPULSE GENERATION AND RECEIVE WAVEFORM FOR DATA OF 1, 1, 0

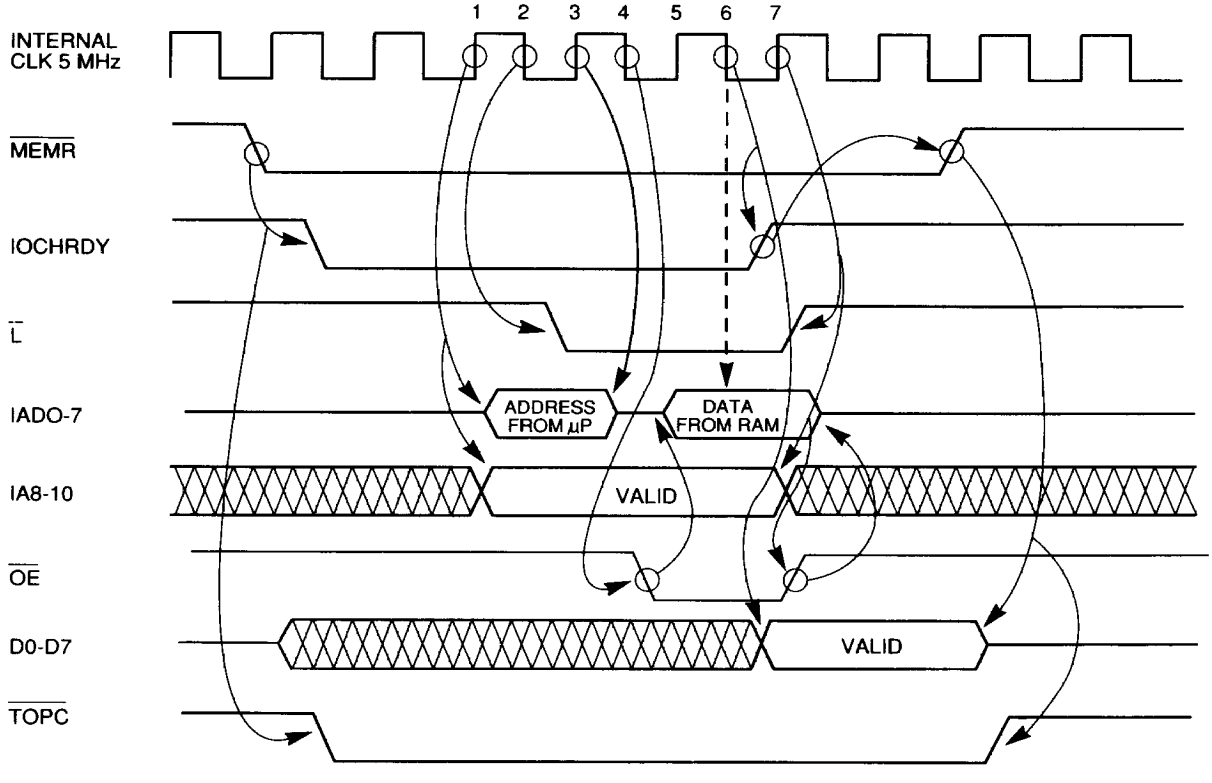


FIGURE 10 - MICROPROCESSOR READ RAM CYCLE

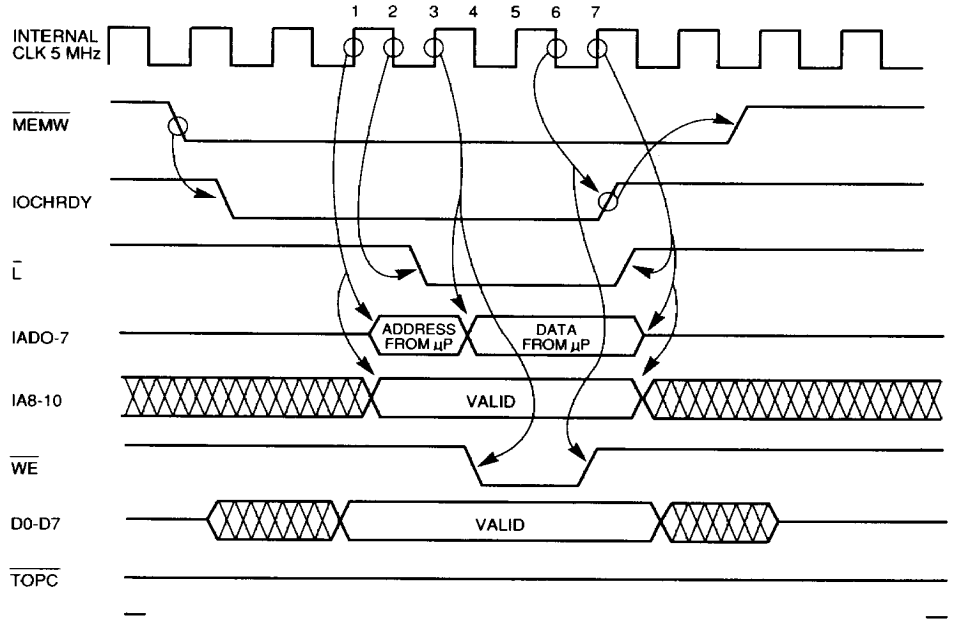


FIGURE 11 - MICROPROCESSOR WRITE RAM CYCLE

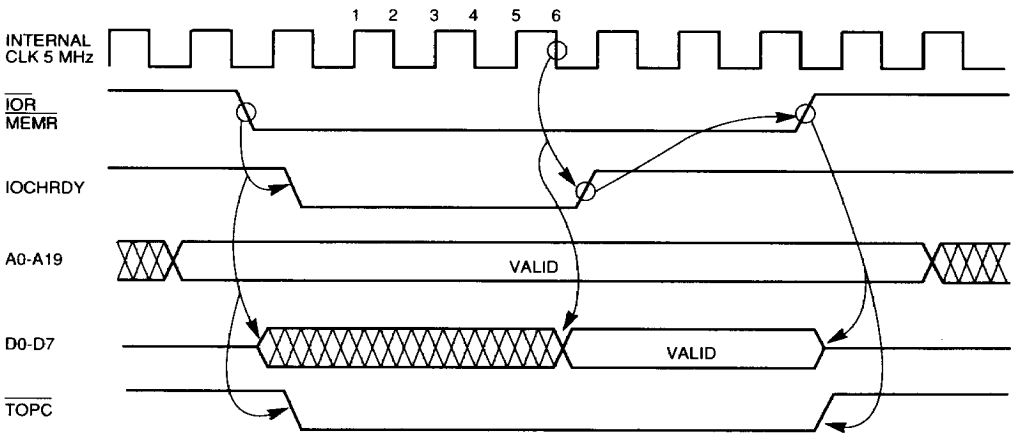


FIGURE 12 - MICROPROCESSOR READ RAM & I/O CYCLE

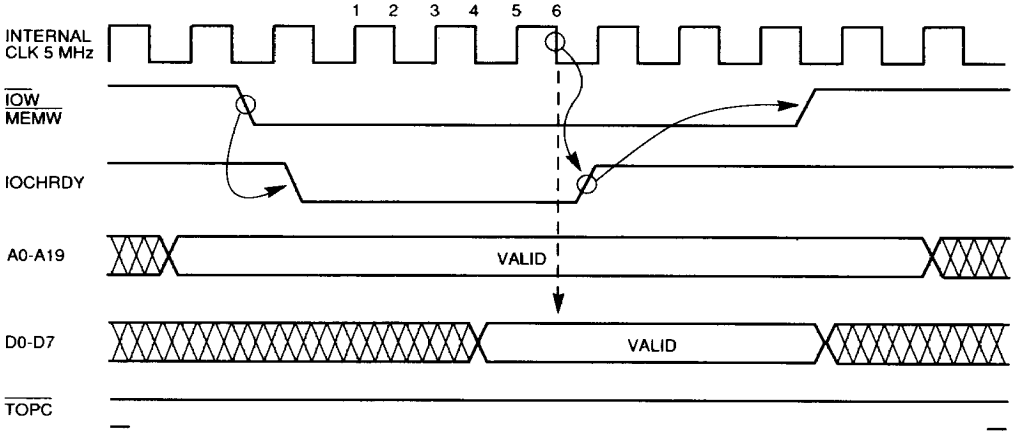


FIGURE 13 - MICROPROCESSOR WRITE RAM & I/O CYCLE

Simultaneously, valid data appears on the Data Bus for the microprocessor. The rising edge of the IOCHRDY signal causes the microprocessor to remove the $\overline{MEMR}$ or $\overline{IOR}$ signal, which in turn causes the Data Bus to become tri-state and the $\overline{TOPC}$ signal to return to a high level. At this point the read cycle is complete.

Microprocessor Write RAM and I/O Cycle

The microprocessor may write the COM90C65 for two purposes (see figure 13). One purpose, described above in the Microprocessor Write RAM Cycle section, is to write data into RAM in preparation for transmission to another node, in which case the microprocessor issues a $\overline{MEMW}$ command. The other purpose is to write either the Command Register or the Interrupt Mask Register, or to access the Reset Register, in which case it issues an $\overline{IOW}$ command. The $\overline{MEMW}$ or the $\overline{IOW}$ signal causes the immediate deactivation of the IOCHRDY signal, thereby signaling the microprocessor to wait. The $\overline{TOPC}$ signal remains at a high level during the entire write cycle. While the microprocessor is being waited, the COM90C65 takes over the operation. Some time later, after the appearance of valid data on the Data Bus, the COM90C65 generates the IOCHRDY signal (time T6) and samples and internally latches the data on the Data Bus. The writing of data into RAM was described in the Microprocessor Write RAM Cycle section and the writing of information into the registers is done internally. The rising edge of the IOCHRDY signal causes the microprocessor to remove the $\overline{MEMW}$ or $\overline{IOW}$ signal, at which point the write cycle is complete.

COM90C65 Read RAM Cycle for Transmission

The COM90C65 Read RAM Cycle (see Figure 14) occurs when the COM90C65 must transmit information stored in RAM to another node. The sequence of events which occur is similar to those which occur when the COM90C65 reads the RAM during the Microprocessor Read RAM Cycle, except that the timing parameters are different. The cycle, which is still controlled by a 5 MHz internal clock, begins with the falling edge of the clock (time T2) which causes a valid address to be placed on the IADO-7 and IA8-10 lines. With the next rising edge of the clock (time T3), the $\overline{L}$ signal is generated to latch the IADO-7 lines onto the LS373. With the next falling edge of the clock (time T4), the IADO-7 lines become tri-state to allow data from the RAM onto the IADO-7 lines. Simultaneously the $\overline{OE}$ signal is generated, which enables the data from the RAM to appear on the IADO-7 lines. This data is sampled at time T8. At the following rising edge of the clock (time T9), the IA8-10 lines become tri-state and the $\overline{L}$ and $\overline{OE}$ signals return to the inactive state, which causes the IADO-7 lines to return to tri-state. This concludes the COM90C65 Read RAM Cycle.

COM90C65 Write RAM Cycle for Reception

The COM90C65 Write RAM Cycle (see figure 15) occurs when the COM90C65 must write information received from another node into RAM. The sequence of events which occur is similar to those which occur when the COM90C65 writes RAM during the Microprocessor Write RAM Cycle, except that the timing parameters are different. The cycle, which is still controlled by a 5 MHz internal clock, begins with the falling edge of the clock (time T2) which causes a valid address to be placed on the IADO-7 and IA8-10 lines. With the next rising edge (time T3), the $\overline{L}$ signal is generated to latch the IADO-7 lines onto the LS373. With the next falling edge of the clock (time T4), the address on the IADO-7 lines is replaced with the data to be written into RAM and the $\overline{WE}$ signal is generated. Some time later, with the rising edge of the clock (time T7), the $\overline{WE}$ signal returns to the inactive state. The following rising edge of the clock (time T9) causes the IADO-7 and IA8-10 lines to become tri-state and the $\overline{L}$ signal returns to the inactive state. This concludes the COM90C65 Write RAM Cycle.

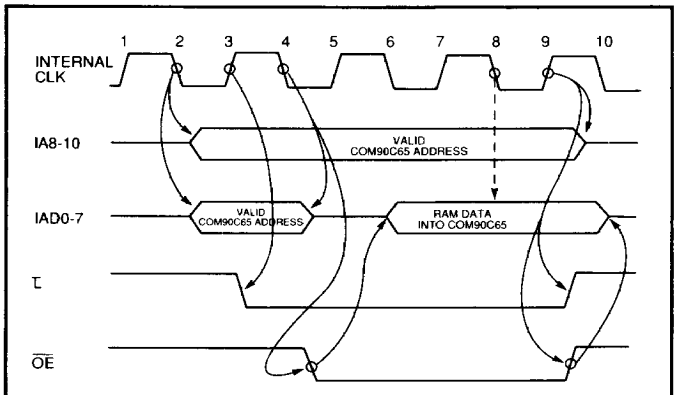


FIGURE 14 - COM90C65 READ RAM CYCLE

OSCILLATOR

The COM90C65 incorporates on-board circuitry which, in conjunction with an external parallel resonant crystal, forms an oscillator. The oscillator frequency may vary from 8 MHz to 20 MHz to allow for a variable data rate from 1.0 Mbps to 2.5 Mbps.

The COM90C65 crystal oscillator has been designed to work with a parallel resonant crystal. A resistor and two capacitors are needed (one from each leg of the crystal to ground). The resistor value is 1 MOhm and the values of the capacitors are two times the load capacitance of the crystal. The external crystal must have an accuracy of 0.020% or better.

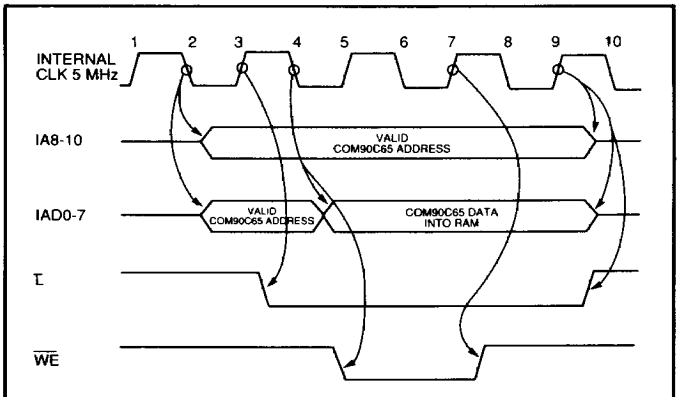


FIGURE 15 - COM90C65 WRITE RAM CYCLE

NODE ID LOGIC

The Node ID code generated by the external Node ID Select Switch is used to identify this particular COM90C65. The code, which is input by the COM90C65 in parallel format, is used by the COM90C65 during transmission, reception, reset, and reconfiguration.

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin, with respect to ground ..... V_{CC}+0.3V
Negative Voltage on any pin, with respect to ground ..... -0.3V
Maximum V_{CC} ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

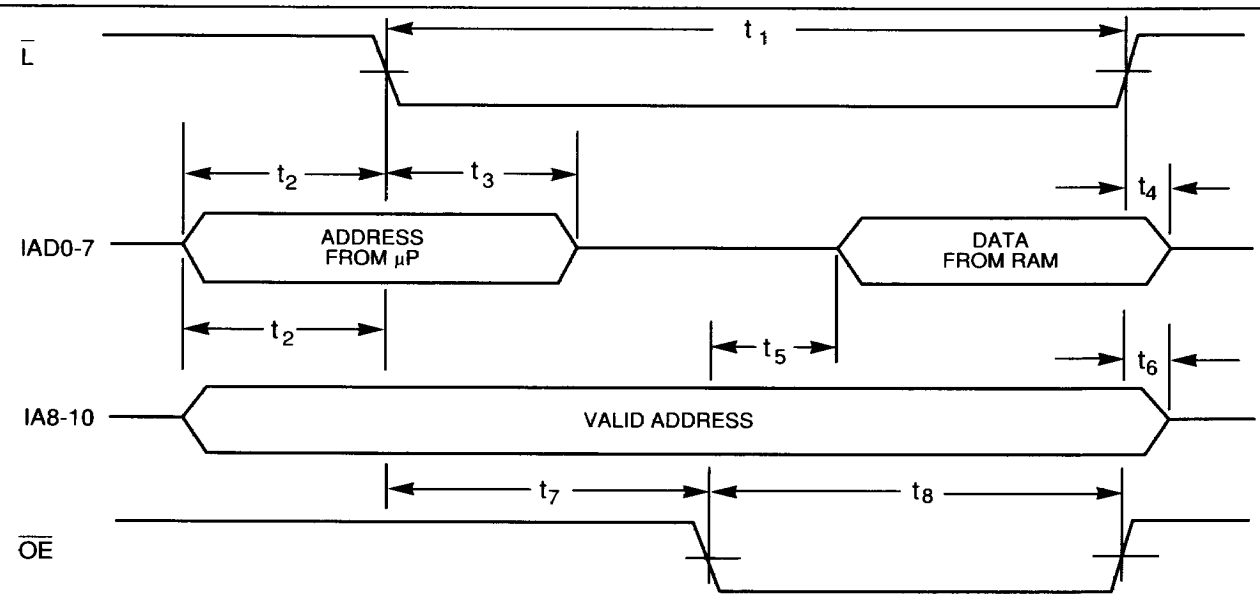
DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V±5%)

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	COMMENTS
Low Input Voltage 1 (All inputs except RESET IN, XTAL 1)	V_{IL1}			0.8	V	TTL Levels
High Input Voltage 1 (All inputs except RESET IN, XTAL 1)	V_{IH1}	2.0			V	TTL Levels
Low Input Voltage 2 (Low to High Threshold) (RESET IN)	V_{IL2}		1.8		V	Schmitt Trigger; All values at V_{DD} = 5V
High Input Voltage 2 (High to Low Threshold) (RESET IN)	V_{IH2}		1.2		V	
Low Input Voltage 3 (XTAL 1)	V_{IL3}			1.0	V	TTL Clock Input
High Input Voltage 3 (XTAL 1)	V_{IH3}		V_{CC}-1.0		V	
Low Output Voltage 1 (All outputs except IOCHRDY)	V_{OL1}			0.4	V	I_{OL} = 2.0mA
High Output Voltage	V_{OH}	2.4			V	I_{OH} = -0.4mA
Low Output Voltage 2 (IOCHRDY)	V_{OL2}			0.4	V	Open Drain Driver I_{OL} = 5.0mA
Input Leakage Current (A0-A19, AEN, RXIN, RESET IN, HOST CLK, XTAL1, IOR, IOW, MEMR, MEMW)	I_L			±10	μA	$V_{SS}<V_{IN}<V_{DD}$
Input Pull-Up Current (ET1, ET2, ENROM, TP1, ECHO, D0-D7, IAD0-IAD7, MS0-MS4, IOS0-IOS2, NID0-NID7)	I_P	0.4		3.0	mA	V_{IN} = 0.0V
V_{CC} Supply Current	I_{CC}		10		mA	
Input Capacitance	C_{IN}			10	pf	

CAPACITANCE (T_A = 25°C; f_C = 1MHz; V_{CC} = 0V)

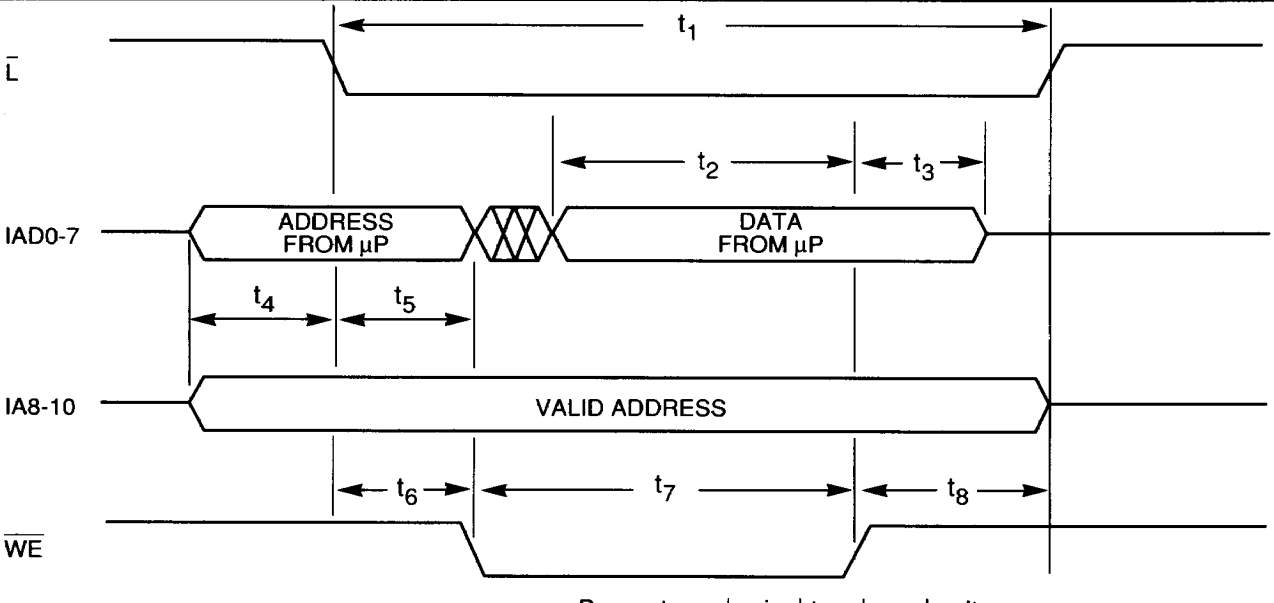
Output and I/O pins capacitive load specified as follows:

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	COMMENTS
Output Capacitance (All outputs except IOCHRDY)	C_{out1}			45	pf	
Output Capacitance (IOCHRDY)	C_{out2}			100	pf	



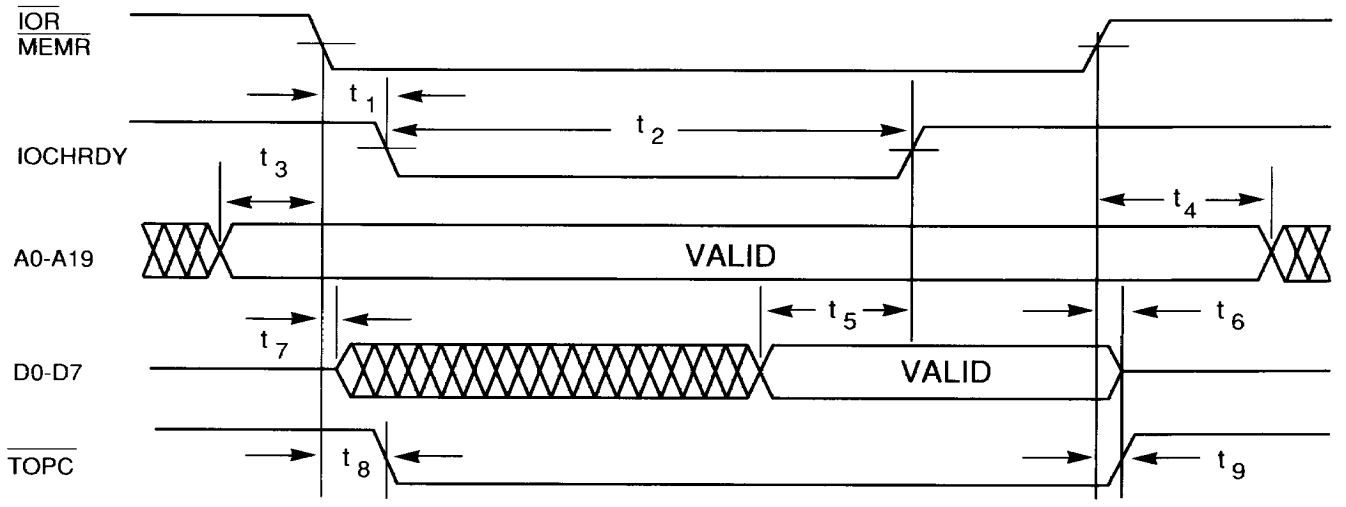
Parameter		min	typ	max	unit
$\overline{L}$ PULSE WIDTH	t1	475	500	525	nS
ADDRESS SET UP TIME	t2	75	100	125	nS
ADDRESS HOLD TIME	t3	75	100	125	nS
$\overline{OE}$ ↑ TO DATA TRISTATE, DATA HOLD	t4	0		80	nS
$\overline{OE}$ ↓ TO DATA VALID	t5	0		100	nS
$\overline{OE}$ ↑ TO IA8 - 10 HOLD	t6	0			nS
$\overline{L}$ ↓ to OE ↓	t7	175	200	225	nS
$\overline{OE}$ PULSE WIDTH	t8	275	300	325	nS

FIGURE 16 — MICROPROCESSOR READ RAM TIMING



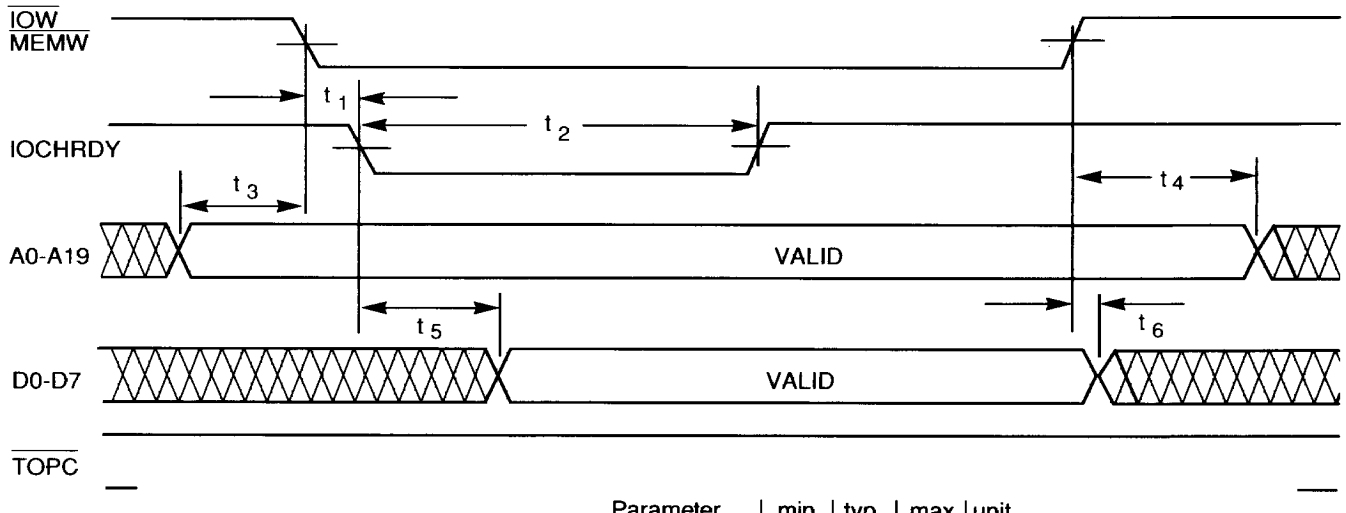
Parameter		min	typ	max	unit
$\overline{L}$ PULSE WIDTH	t1	475	500	525	nS
DATA VALID TO $\overline{WE}$ ↑	t2	125			nS
$\overline{WE}$ ↑ TO DATA TRISTATE	t3	25	100		nS
ADDRESS SET UP TIME	t4	75	100	125	nS
ADDRESS HOLD TIME	t5	75	100	125	nS
$\overline{L}$ ↓ TO $\overline{WE}$ ↓	t6	75	100	125	nS
$\overline{WE}$ PULSE WIDTH	t7	275	300	325	nS
$\overline{WE}$ ↑ TO $\overline{L}$ ↑	t8	75			nS

FIGURE 17 — MICROPROCESSOR WRITE RAM TIMING



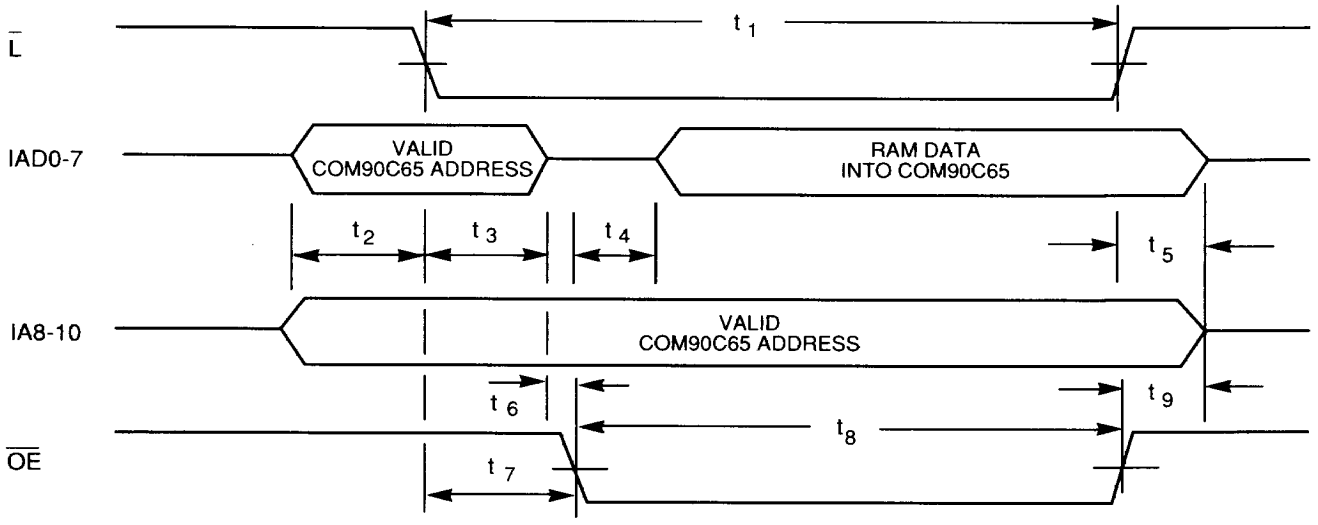
Parameter		min	typ	max	unit
IOR ↓, MEMR ↓ TO IOCHRDY ↓	t1			40	nS
IOCHRDY PULSE WIDTH	t2	500		1400	nS
ADDRESS SET UP TIME	t3	40			nS
ADDRESS HOLD TIME	t4	20			nS
DATA SET UP TIME	t5	60	100		nS
IOR↓, MEMR↓ TO TRISTATE	t6	0		25	nS
IOR ↓, MEMR ↓ TO DATA ACTIVE	t7	0		25	nS
IOR ↓, MEMR ↓ TO TOPC ↓	t8	0		25	nS
IOR ↑, MEMR ↑ TO TOPC ↑	t9	0		25	nS

FIGURE 18 — MICROPROCESSOR READ RAM & I/O TIMING



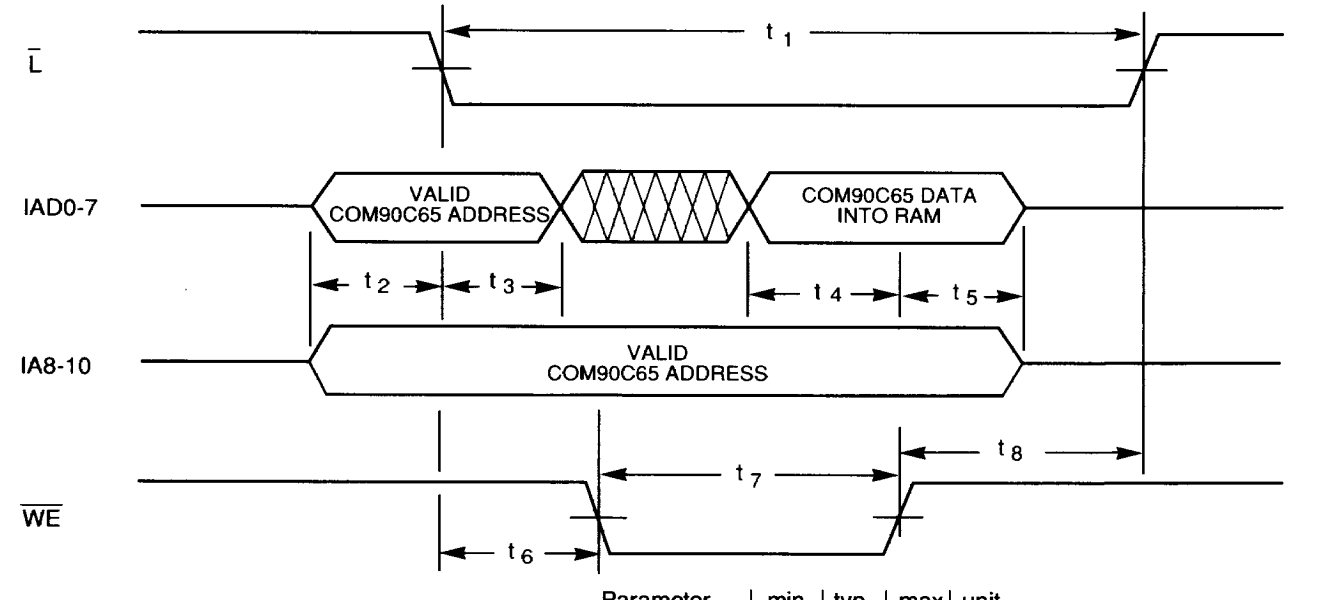
Parameter		min	typ	max	unit
IOW ↓ TO IOCHRDY ↓	t1			35	nS
IOCHRDY PULSE WIDTH	t2	500		1400	nS
ADDRESS SET UP TIME	t3	40			nS
ADDRESS HOLD TIME	t4	20			nS
DATA VALID DELAY	t5			100	nS
DATA HOLD TIME	t6	0			nS

FIGURE 19 — MICROPROCESSOR WRITE RAM & I/O TIMING



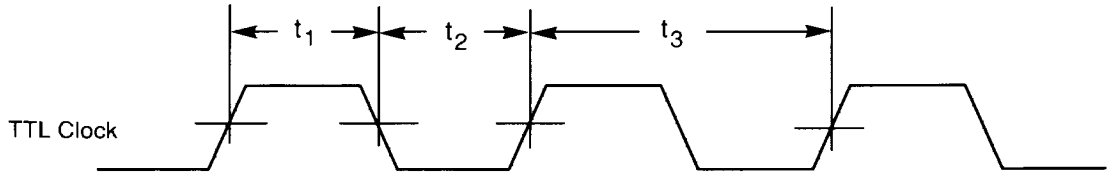
Parameter		min	typ	max	unit
L PULSE WIDTH	t1	575	600	625	nS
ADDRESS SET UP TIME	t2	75	100	125	nS
ADDRESS HOLD TIME	t3	75	100	125	nS
OE ↓ TO DATA VALID	t4	0		100	nS
OE ↑ TO DATA TRISTATE, DATA HOLD	t5	0		80	nS
ADDRESS TRISTATE TO OE ↓	t6	0			nS
L ↓ TO OE ↓	t7	75	100	125	nS
OE PULSE WIDTH	t8	475	500	525	nS
OE ↑ TO IA8-10 HOLD	t9	0			nS

FIGURE 20 — COM90C65 READ RAM TIMING



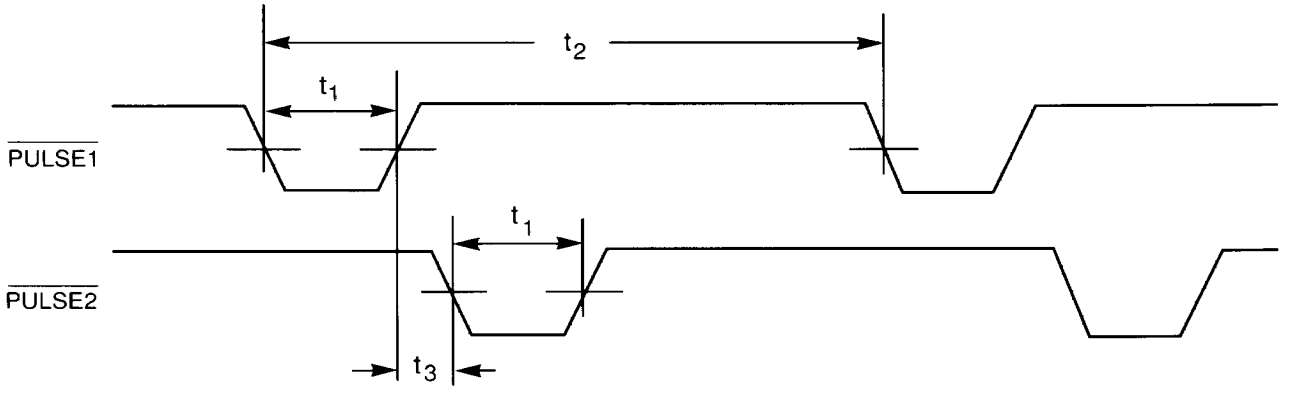
Parameter		min	typ	max	unit
L PULSE WIDTH	t1	575	600	625	nS
ADDRESS SET UP TIME	t2	75	100	125	nS
ADDRESS HOLD TIME	t3	75	100	125	nS
DATA VALID TO WE ↑	t4	125			nS
WE ↑ TO DATA TRISTATE	t5	25			nS
L ↓ TO WE ↓	t6	75	100	125	nS
WE PULSE WIDTH	t7	275	300	325	nS
WE ↑ TO L ↑	t8	175	200		nS

FIGURE 21 — COM90C65 WRITE RAM TIMING



Parameter		min	typ	max	unit
INPUT CLOCK HIGH TIME	t1	20			nS
INPUT CLOCK LOW TIME	t2	20			nS
INPUT CLOCK PERIOD	t3	50		1000	nS
INPUT CLOCK FREQUENCY	f	1		20	MHz

FIGURE 22 — TTL INPUT CLOCK TIMING ON HOST CLK PIN

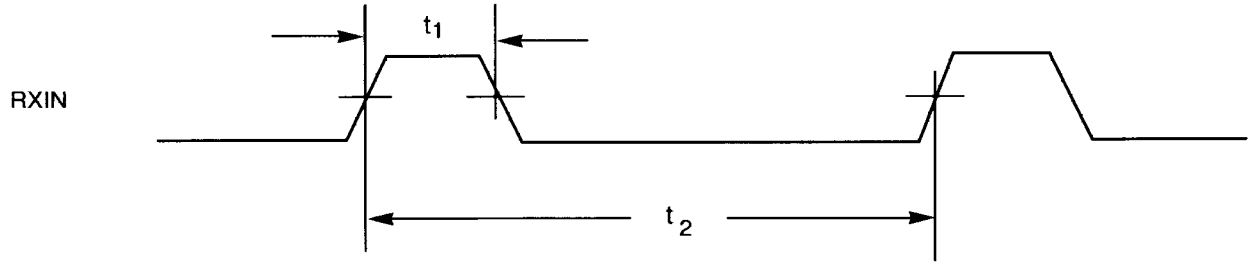


Parameter		min	typ	max	unit	
$\overline{\text{PULSE1}}$, $\overline{\text{PULSE2}}$ PULSE WIDTH	t1		100		nS	*
$\overline{\text{PULSE1}}$, $\overline{\text{PULSE2}}$ PERIOD	t2		400		nS	**
$\overline{\text{PULSE1}}$, $\overline{\text{PULSE2}}$ OVERLAP	t3	-10	0	+10	nS	

*NOTE 1: t_1 = 2 x (crystal period) for clock frequencies other than 20 MHz.

**NOTE 2: t_2 = 8 x (crystal period) for clock frequencies other than 20 MHz. This period applies to data of two consecutive one's.

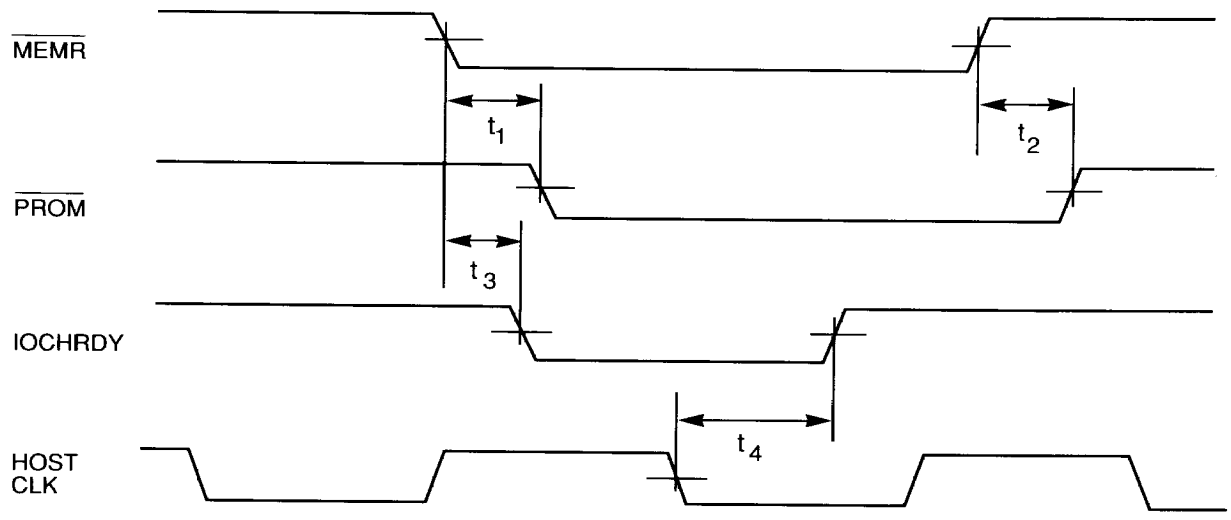
FIGURE 23 — TRANSMIT TIMING



Parameter		min	typ	max	unit	
RXIN PULSE WIDTH	t1	10			nS	
RXIN PERIOD	t2		400		nS	*

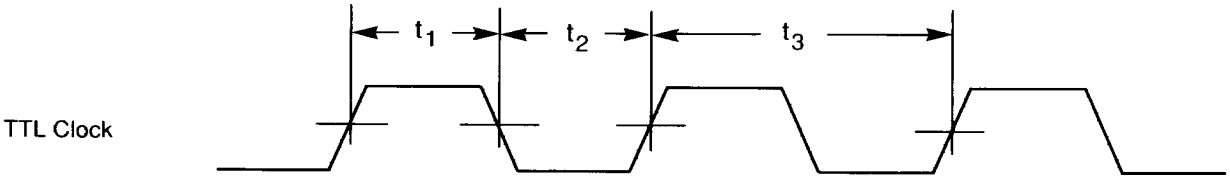
*NOTE: This period applies to data of two consecutive one's.

FIGURE 24 — RECEIVE TIMING



Parameter		min	typ	max	unit
MEMR ↓ TO PROM ↓	t1			30	nS
MEMR ↑ TO PROM ↑	t2			30	nS
MEMR ↓ TO IOCHRDY ↓	t3			25	nS
HOST CLK ↓ TO IOCHRDY ↑	t4			60	nS

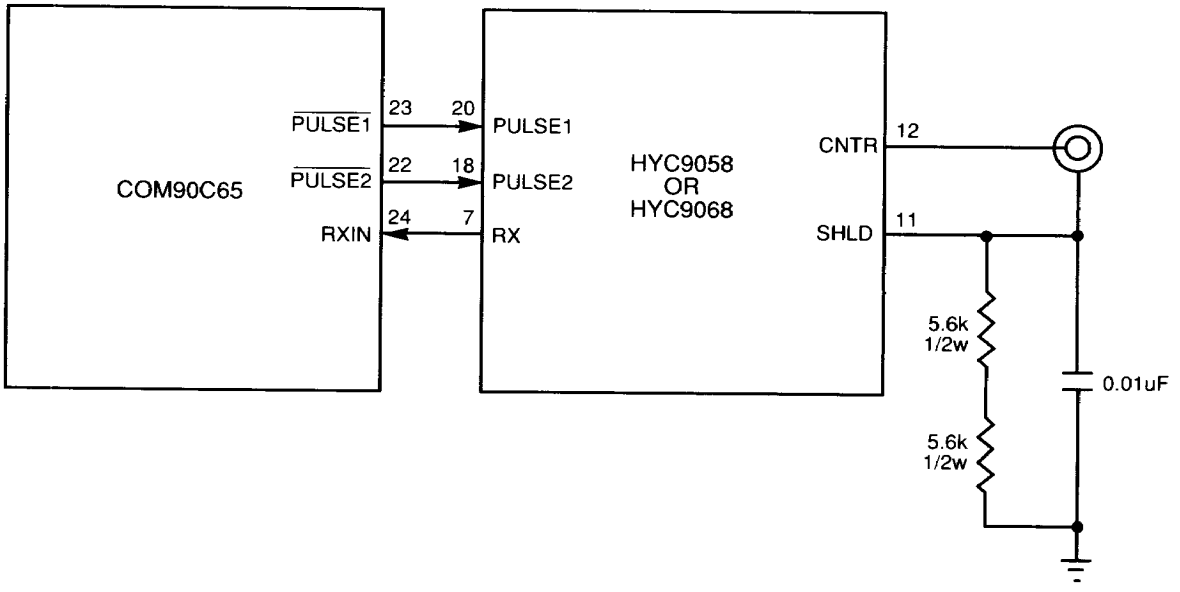
FIGURE 25 — PROM TIMING



Parameter		min	typ	max	unit
INPUT CLOCK HIGH TIME	t1	20			nS
INPUT CLOCK LOW TIME	t2	20			nS
INPUT CLOCK PERIOD	t3	50		125	nS
INPUT CLOCK FREQUENCY	f	8		20	MHz

FIGURE 26 — TTL INPUT CLOCK TIMING ON XTAL1 PIN

COAX INTERFACE



TWISTED PAIR INTERFACE

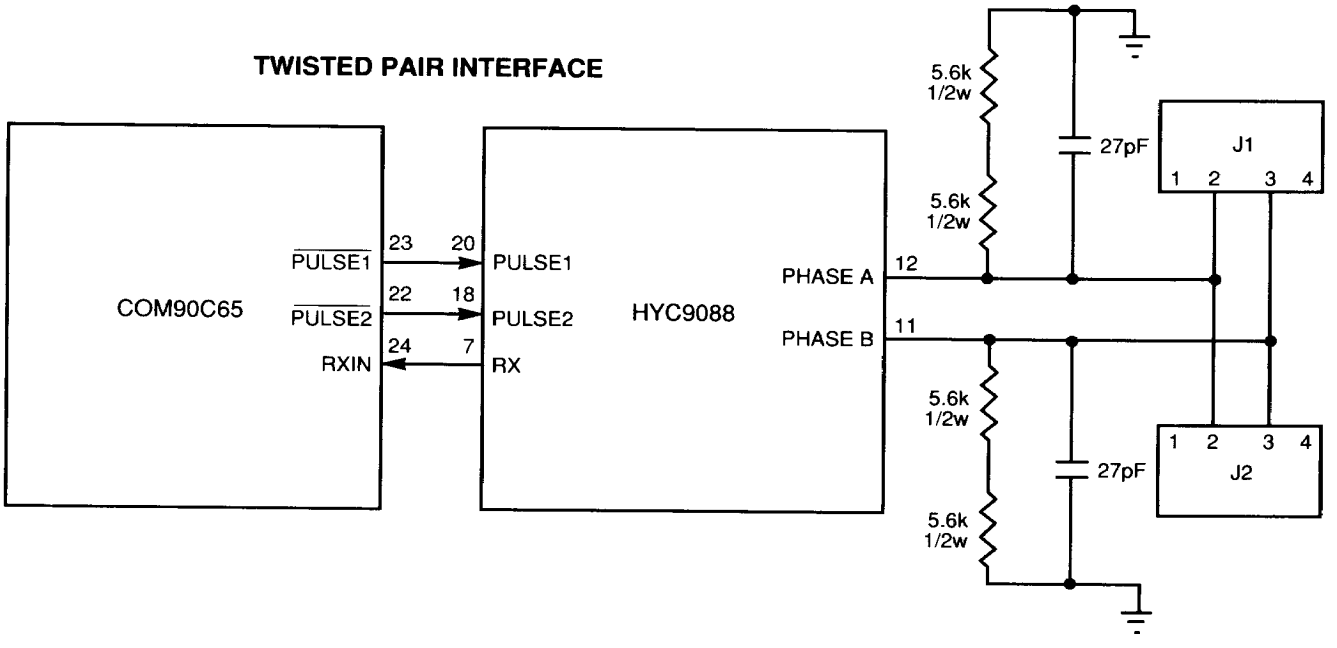
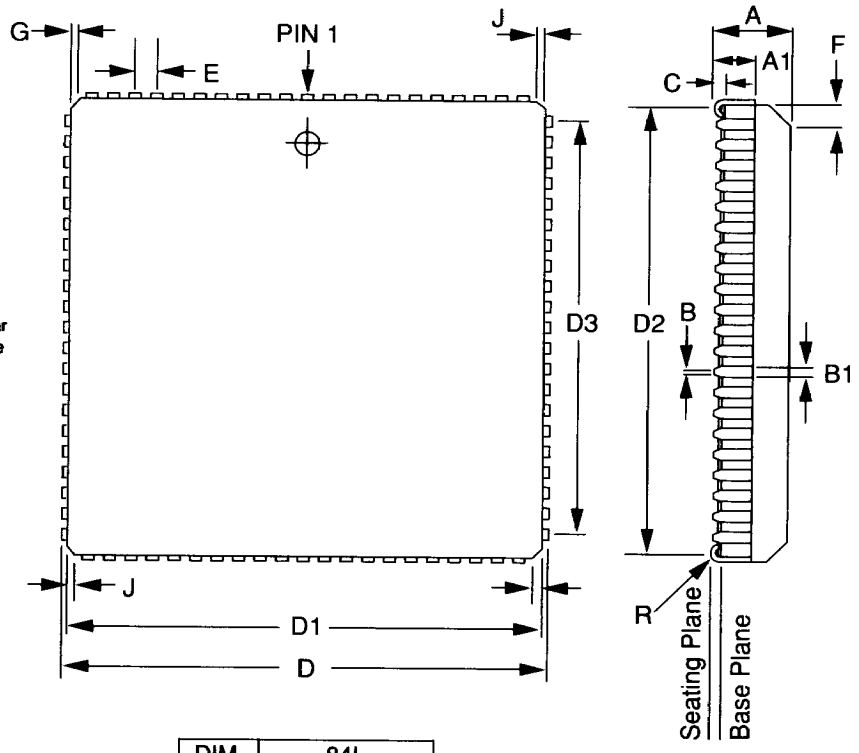


FIGURE 27 - MEDIA INTERFACES

NOTE:

1. All dimensions are in inches.
2. Circle indicating pin 1 can appear on a top surface as shown on the drawing or right above it on a beveled edge.



DIM	84L
A	.165-.179
A1	.095-.109
D	1.185-1.195
D1	1.150-1.156
D2	1.090-1.130
D3	1.000
F	.050 TYP
G	.045 TYP
J	.010
E	.047-.053
R	.025-.045
B	.013-.021
B1	.027
C	.020-.045

FIGURE 28 — 84-PIN PLCC PACKAGE DIMENSIONS

STANDARD MICROSYSTEMS CORPORATION
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