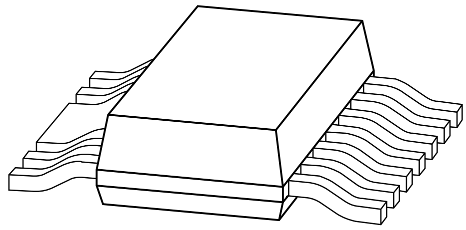
GaAs MMIC — CGY 181

Data Sheet

- Power amplifier for PCN/PCS applications
- Fully integrated 2 stage amplifier
- Operating voltage range: 2.7 to 6 V
- Overall power added efficiency 35%
- Input matched to 50 Ω, simple output match

ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!



Type	Marking	Ordering Code (8-mm taped)	Package[1]
CGY 181	CGY 181	Q68000-A8883	MW-12

[1] Plastic body identical to P-SOT-223, dimensions see **Page 14**.

Maximum Ratings	Symbol	Value	Unit
Positive supply voltage	V_D	9	V
Negative supply voltage[1]	V_G	– 8	V
Supply current	I_D	2	A
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	– 55 … + 150	°C
RF input power	P_{in}	25	dBm
Total power dissipation ($T_s \leq 81$ °C) T_s: Temperature at soldering point	P_{tot}	5	W

[1] $V_G = -8$ V only in combination with $V_{TR} = 0$ V; $V_G = -6$ V while $V_{TR} \neq 0$ V

Thermal Resistance	Symbol	Value	Unit
Channel-soldering point	R_{thChS}	≤ 14	K/W

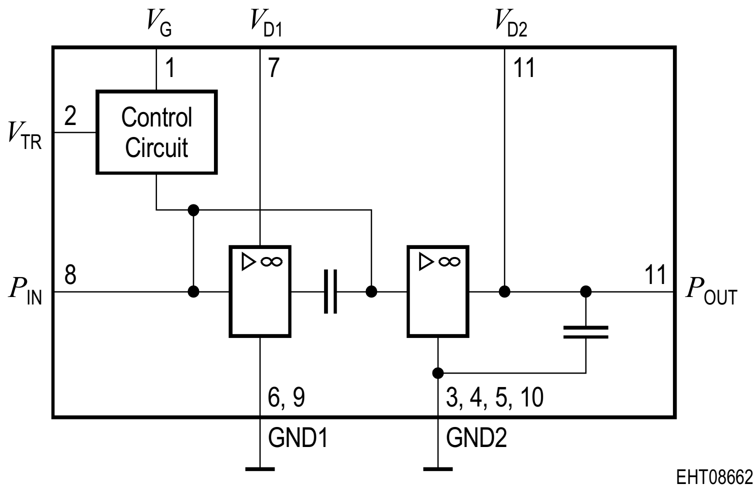


Figure 1 Functional Block Diagram

Short Description of CGY 181 Operation

A negative voltage between – 4 V to – 6 V (stabilization not necessary) has to be connected to the VG-pin, a positive supply voltage has to be applied to the VD-pins.

The VTR-pin has to switched to 0 V (GND) during transmit operation. The MMIC CGY 181 is self-biased, the operating current is adjusted by the internal control circuit.

In receive mode the VTR-pin is not connected (shut off mode).

Pin #	Symbol	Configuration
1	VG	Negative voltage at control circuit (– 4 V … – 8 V)
2	VTR	Control voltage for transmit mode (0 V) or receive mode (open)
3, 4, 5, 10	GND 2	RF and DC ground of the 2nd stage
6, 9	GND 1	RF and DC ground of the 1st stage
7	VD1	Positive drain voltage of the 1st stage
8	RFin	RF input power
11	VD2, RFout	Positive drain voltage of the 2nd stage, RF output power
12	–	not connected

DC Characteristics

Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Drain current (stage 1 and 2)	I_{DSS1}	0.6	0.9	1.2	A	V_D = 3 V, V_G = 0 V, V_{TR} n.c.
	I_{DSS2}	2.4	3.5	4.8	A	
Drain current with active current control	I_D	–	1.0	–	A	V_D = 3 V, V_G = – 4 V, V_{TR} = 0 V
Transconductance (stage 1 and 2)	G_{fs1}	0.28	0.32	–	S	V_D = 3 V, I_D = 350 mA
	G_{fs2}	1.1	1.3	–	S	V_D = 3 V, I_D = 700 mA
Pinch off voltage	V_p	– 3.8	– 2.8	– 1.8	V	V_D = 3 V, I_D < 500 µA (all stages)

Electrical Characteristics
T_A = 25 °C, f = 1.75 GHz, Z_S = Z_L = 50 Ω, V_D = 3.6 V, V_g = – 4 V, VTR pin connected to ground; unless otherwise specified

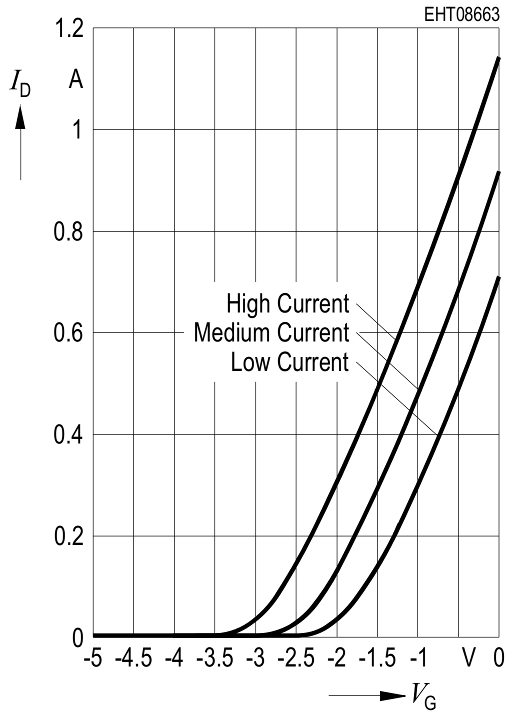
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_{DD}	–	1.2	–	A	P_{in} = 0 dBm
Negative supply current	I_G	–	2	3	mA	(normal operation)
Shut-off current	I_D	–	400	–	µA	VTR n.c.
Negative supply current	I_G	–	10	–	µA	(shut off mode, VTR pin n.c.)
Small signal gain	G	–	20.5	–	dB	P_{in} = – 5 dBm
Power Gain	G	14.5	15.5	–	dB	V_D = 3.6 V, P_{in} = 16 dBm
Power Gain	G	17.5	18.5	–	dB	V_D = 5 V, P_{in} = 16 dBm

Electrical Characteristics (cont'd)
T_A = 25 °C, f = 1.75 GHz, Z_S = Z_L = 50 Ω, V_D = 3.6 V, V_g = – 4 V, VTR pin connected to ground; unless otherwise specified

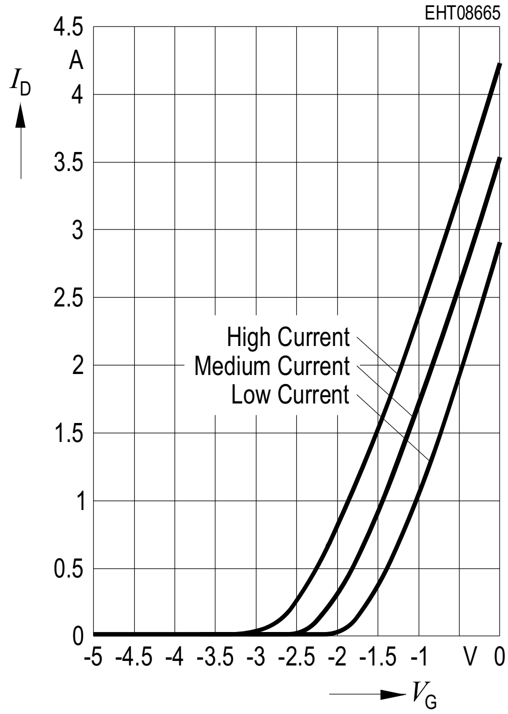
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Output Power	P_0	30.5	31.5	–	dBm	V_D = 3.6 V, P_{in} = 16 dBm
Output Power	P_0	33.5	34.5	–	dBm	V_D = 5 V, P_{in} = 16 dBm
Overall Power Added Efficiency	η	–	37	–	%	V_D = 3.6 V, P_{in} = 16 dBm
Overall Power Added Efficiency	η	–	35	–	%	V_D = 5 V, P_{in} = 16 dBm
Harmonics $2f_0$ $3f_0$	–	– –	– 44.8 – 70	– –	dBc	P_{in} = 16 dBm, V_D = 3.6 V, P_{out} = 31.85 dBm
Harmonics $2f_0$ $3f_0$	–	– –	– 45.1 – 75	– –	dBc	P_{in} = 16 dBm, V_D = 5 V, P_{out} = 31.85 dBm
Input VSWR	–	–	1.9:1	–	–	V_D = 3.6 V
Third order intercept point	IP_3	–	41	–	dBm	f_1 = 1.7500 GHz; f_2 = 1.7502 GHz; V_D = 3.6V
Third order intercept point	IP_3	–	44	–	dBm	f_1 = 1.7500 GHz; f_2 = 1.7502 GHz; V_D = 5 V

All RF-measurements were done in a pulsed mode with a duty cycle of 10%
(t_{on} = 0.33 ms)!

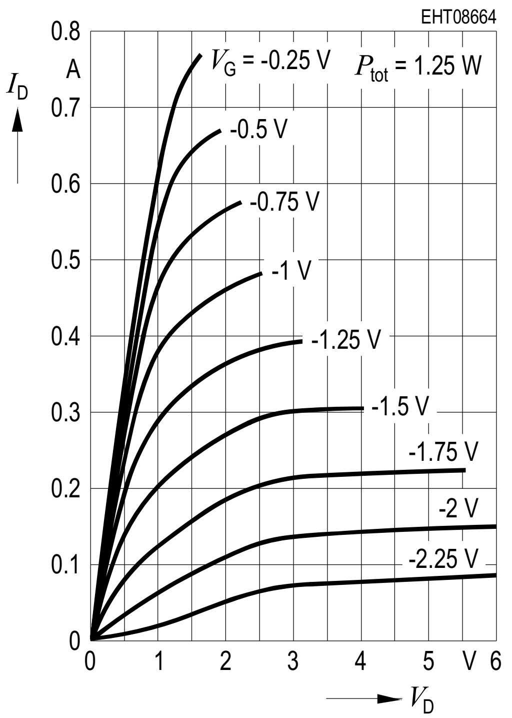
DC-I_D (V_G) Characteristics - Typical Values of Stage 1, V_D = 3 V



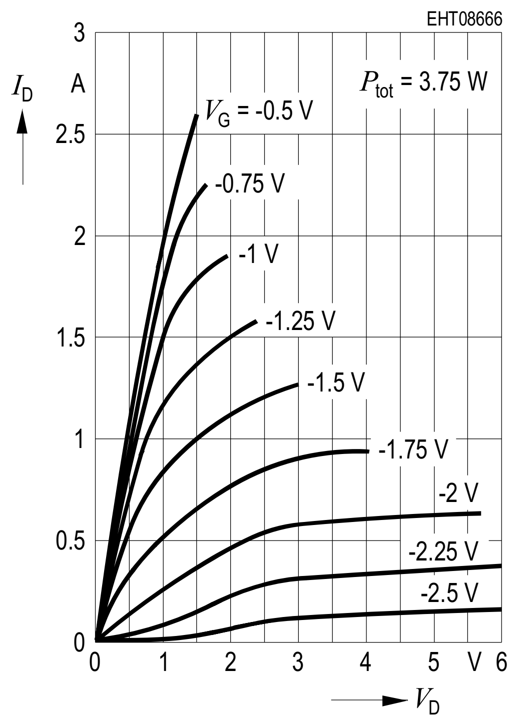
DC-I_D (V_G) Characteristics - Typical Values of Stage 2, V_D = 3 V



DC-Output Characteristics - Typical Values of Stage 1*

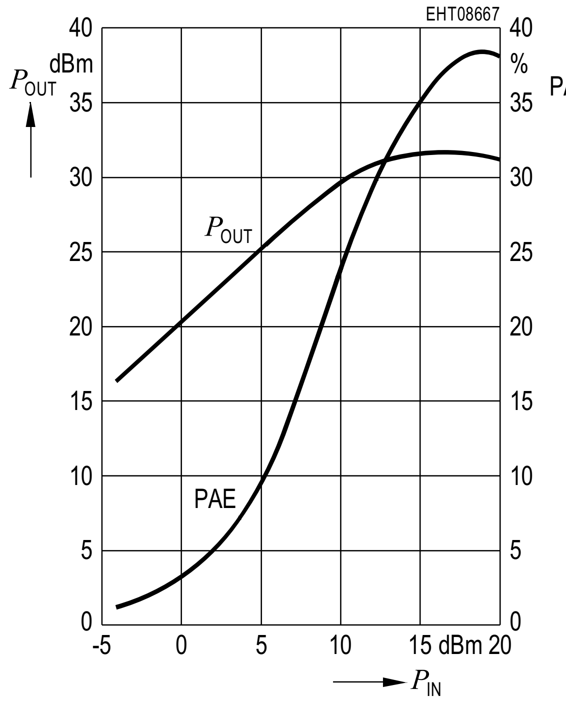


DC-Output Characteristics - Typical Values of Stage 2*

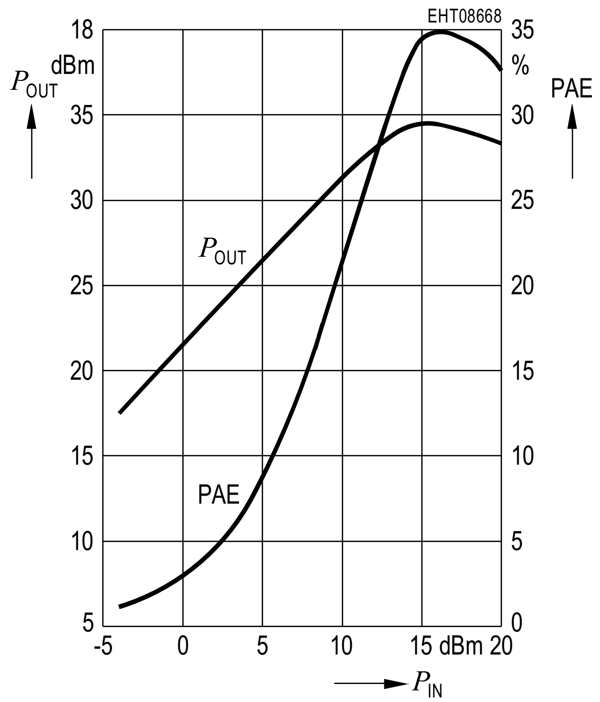


*Pin 2 (V_{TR}) has to be open during measuring DC-characteristics!

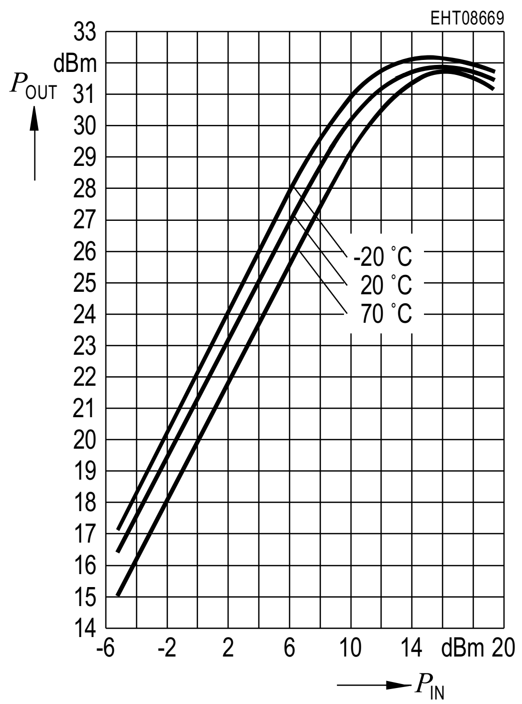
P_{out} and PAE vs. P_{in}, V_D = 3.6 V, V_G = – 4 V, f = 1.75 GHz, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



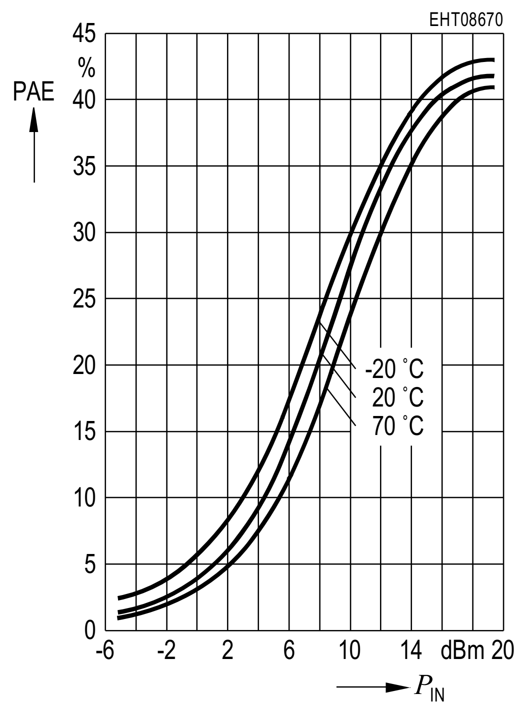
P_{out} and PAE vs. P_{in}, V_D = 5 V, V_G = – 4 V, f = 1.75 GHz, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



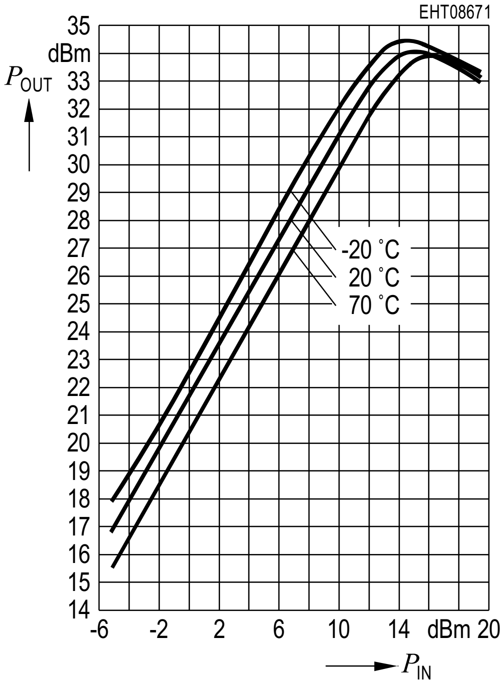
Output Power at Different Temperatures, V_D = 3.6 V, V_G = – 4 V, f = 1.75 GHz, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



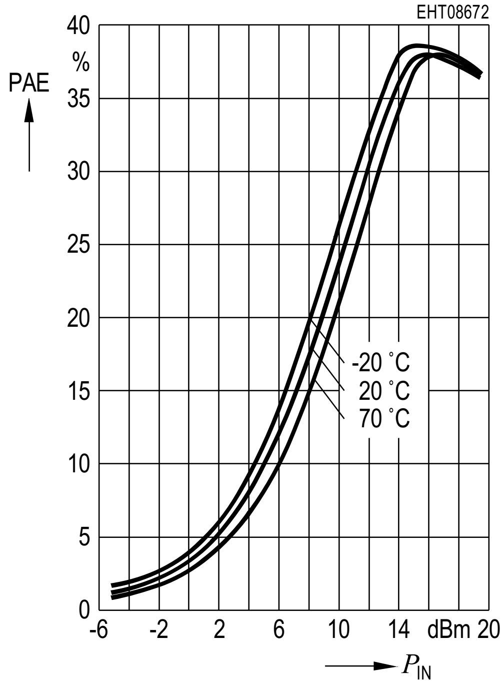
Power Added Efficiency at Different Temperatures, V_D = 3.6 V, V_G = – 4 V, f = 1.75 GHz, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



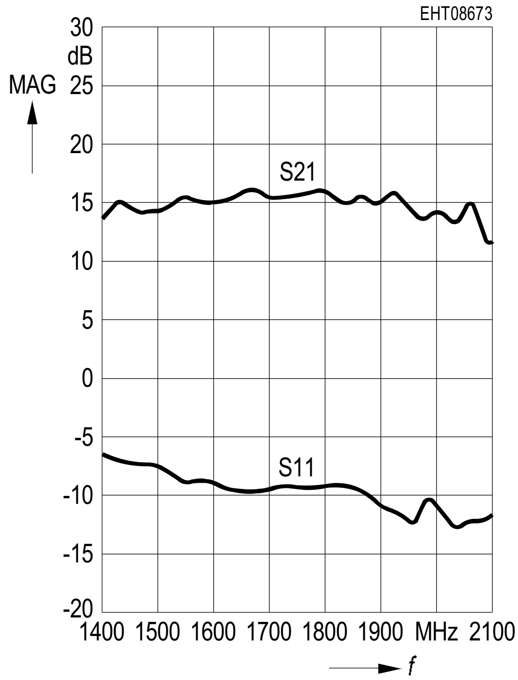
Output Power at Different Temperatures, V_D = 5 V, V_G = – 4 V, f = 1.75 GHz, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



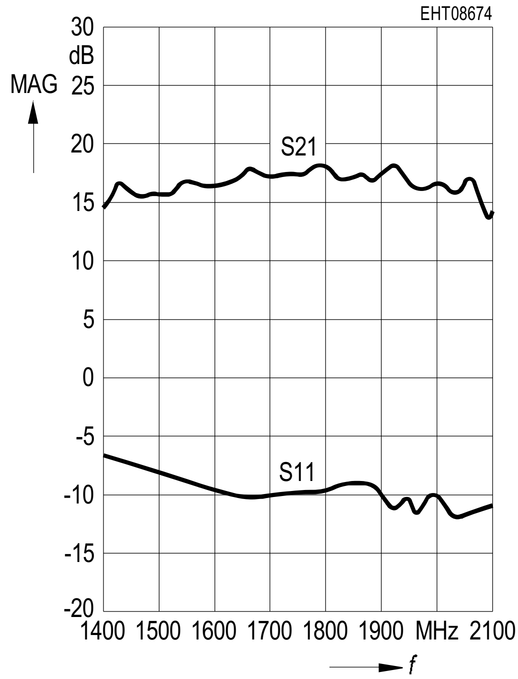
Power Added Efficiency at Different Temperatures, V_D = 5 V, V_G = – 4 V, f = 1.75 GHz, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



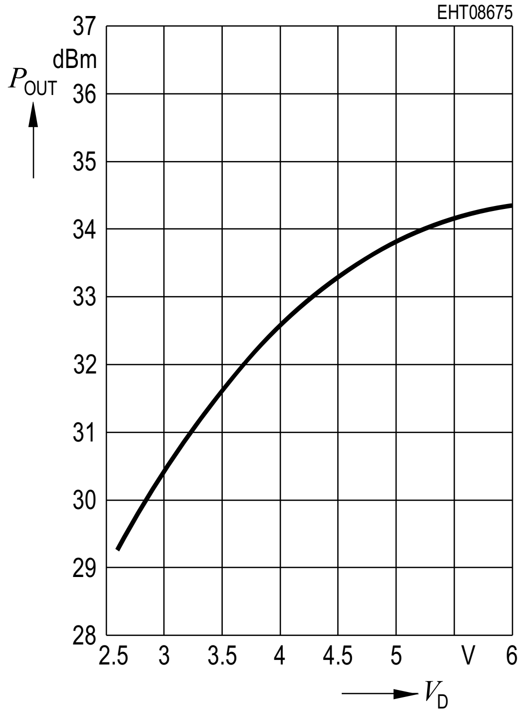
Measured S-Parameter at V_D = 3.6 V and P_{in} = 16 dBm, V_G = – 4 V, VTR connected to ground, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



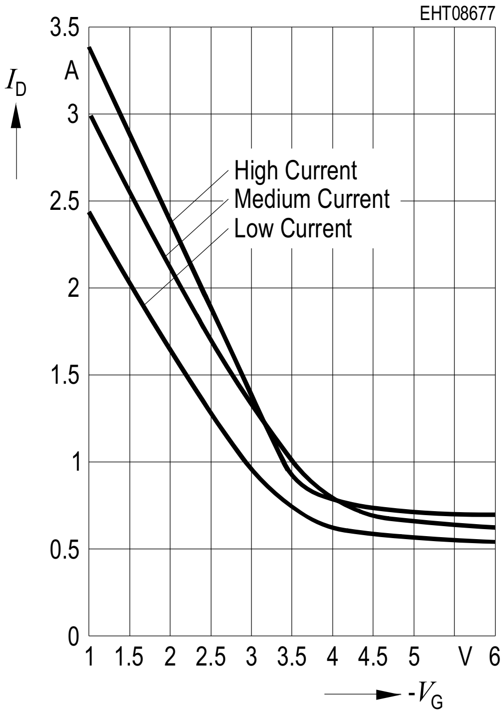
Measured S-Parameter at V_D = 5 V and P_{in} = 16 dBm, V_G = – 4 V, VTR connected to ground, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



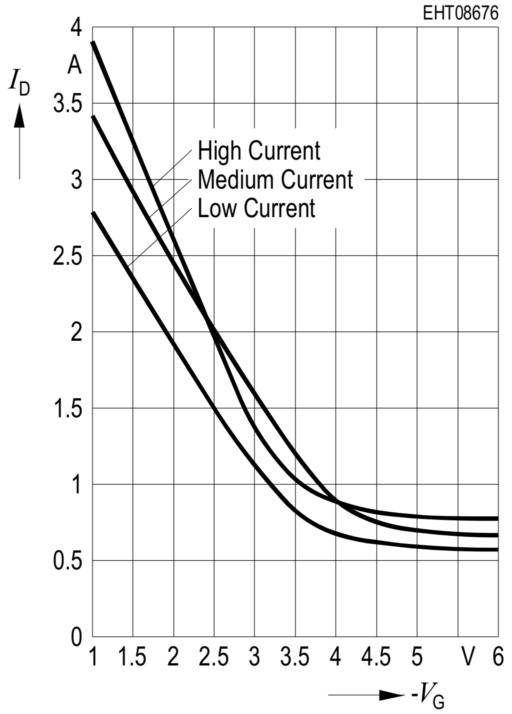
P_{out} vs. V_D, V_G = – 4 V, f = 1.75 GHz, P_{in} = 16 dBm, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



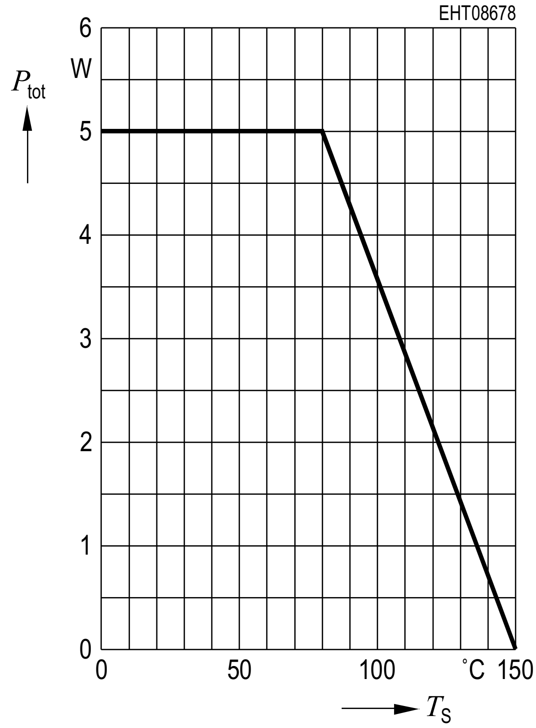
Performance of Internal Bias Control Circuit @ V_D = 5 V, V_{TR} = 0 V, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



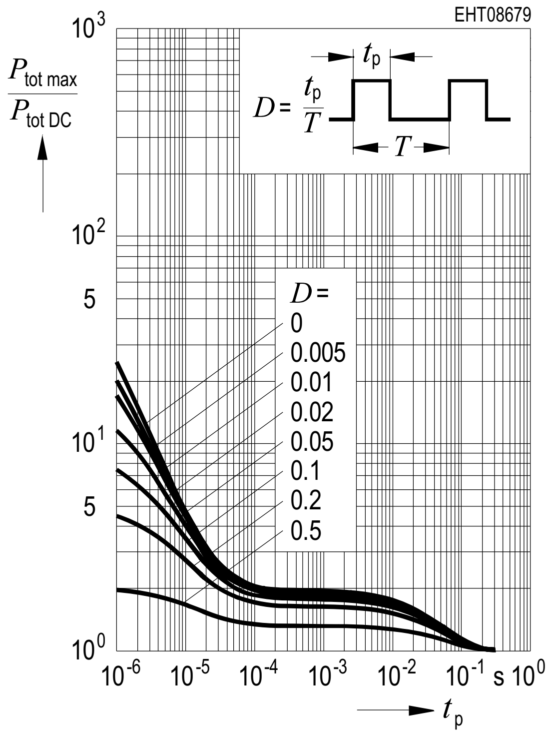
Performance of Internal Bias Control Circuit @ V_D = 3 V, V_{TR} = 0 V, pulsed with a duty cycle of 10% (t_{on} = 0.33 ms)



Total Power Dissipation
$P_{tot} = f(T_S)$



Permissible Pulse Load
$P_{tot\_max}/P_{tot\_DC} = f(t_{\_P})$



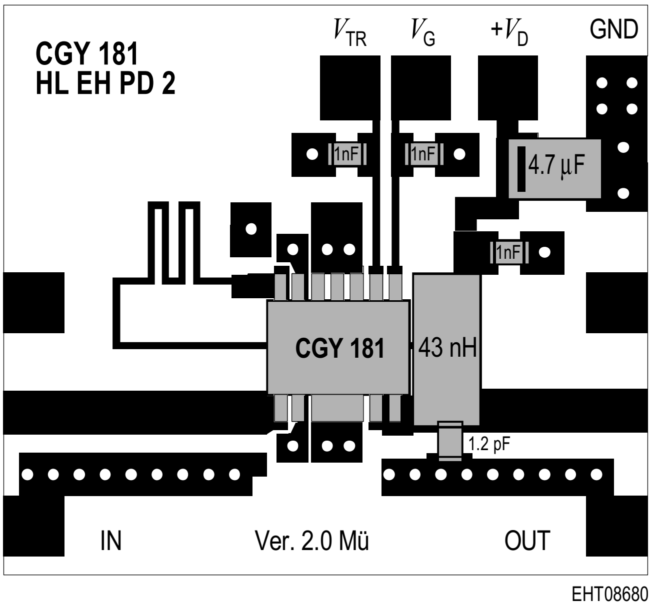


Figure 2 CGY 181 Application Board

Layout size is 30 mm × 26 mm.

Part Type	Description
CGY 181	Infineon GaAs-MMIC
1 nF	Capacitor SMD 0805
1 nF	Capacitor SMD 0805
1 nF	Capacitor SMD 0805
1 p2	Capacitor SMD 0805
4 µ7	Capacitor SMD Tantal
43 nH	Coilcraft SMD Spring Inductor B10T (distributed by Ginsbury Electronic GmbH, Am Moosfeld 85, D-81829 München Tel.: 089/45170-223)

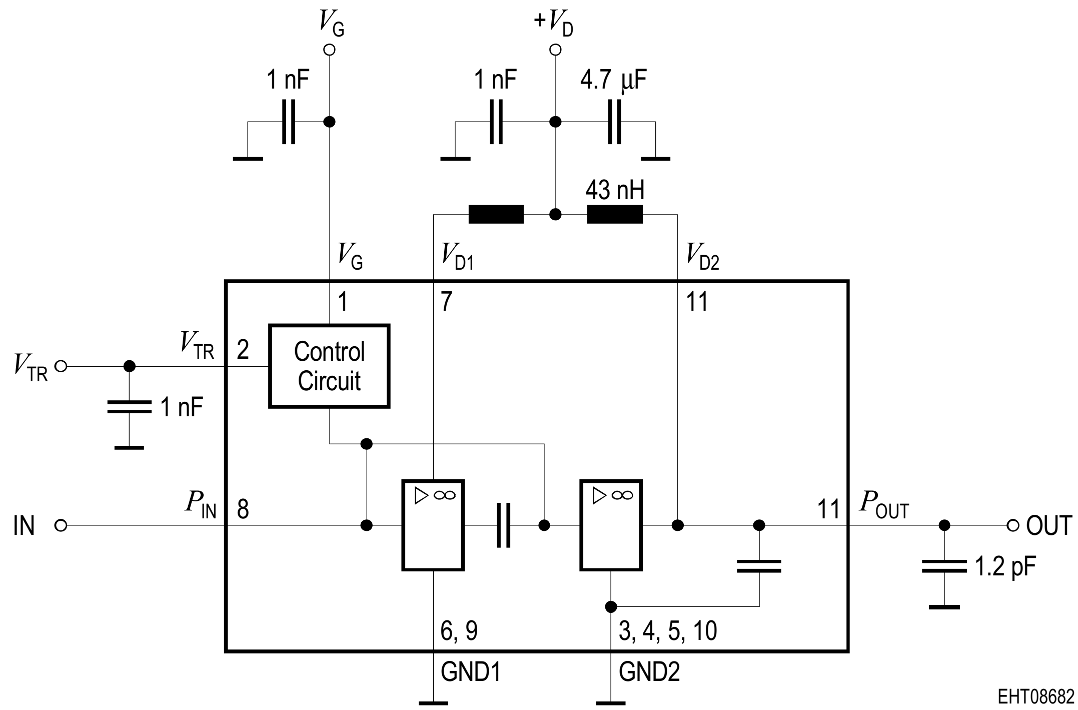


Figure 3 Principal Circuit

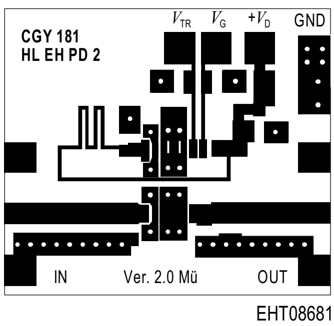


Figure 4 Original Size

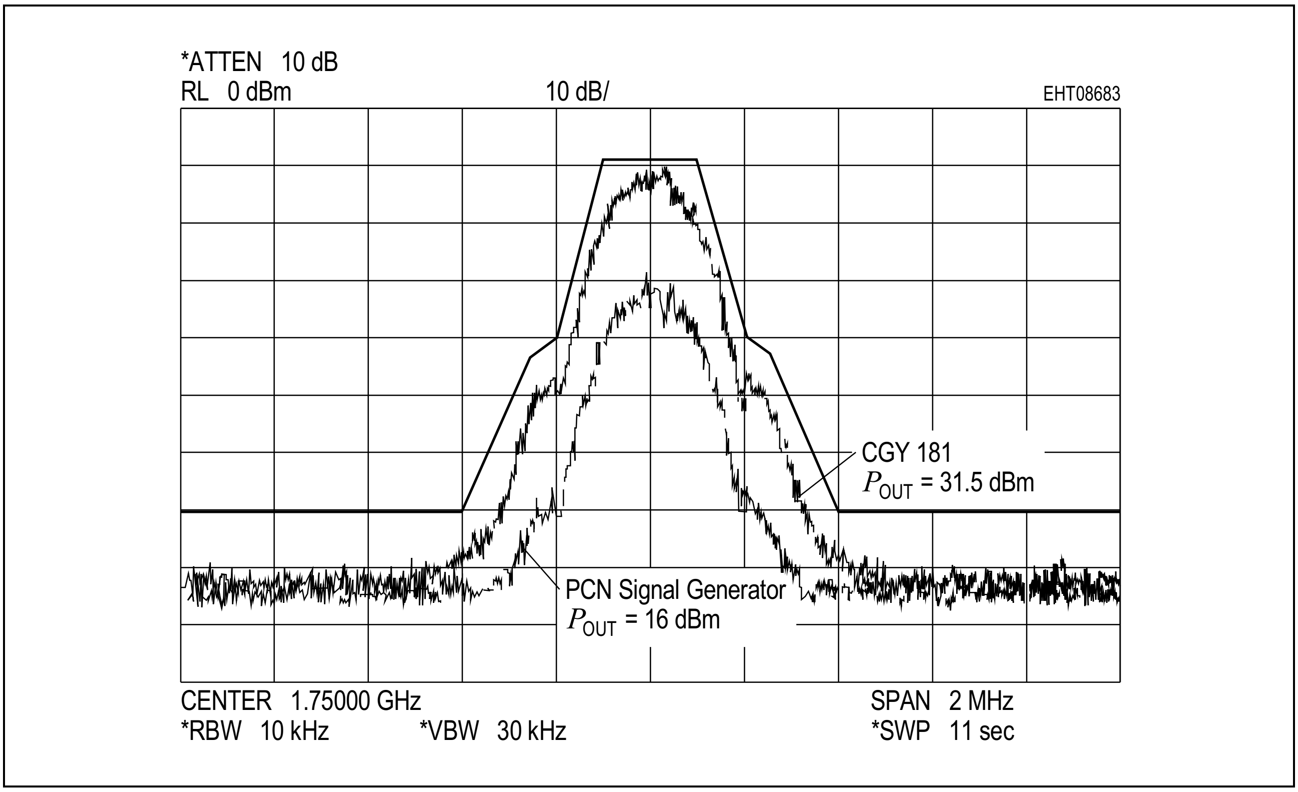


Figure 5 Emissions due to GMSK Modulation

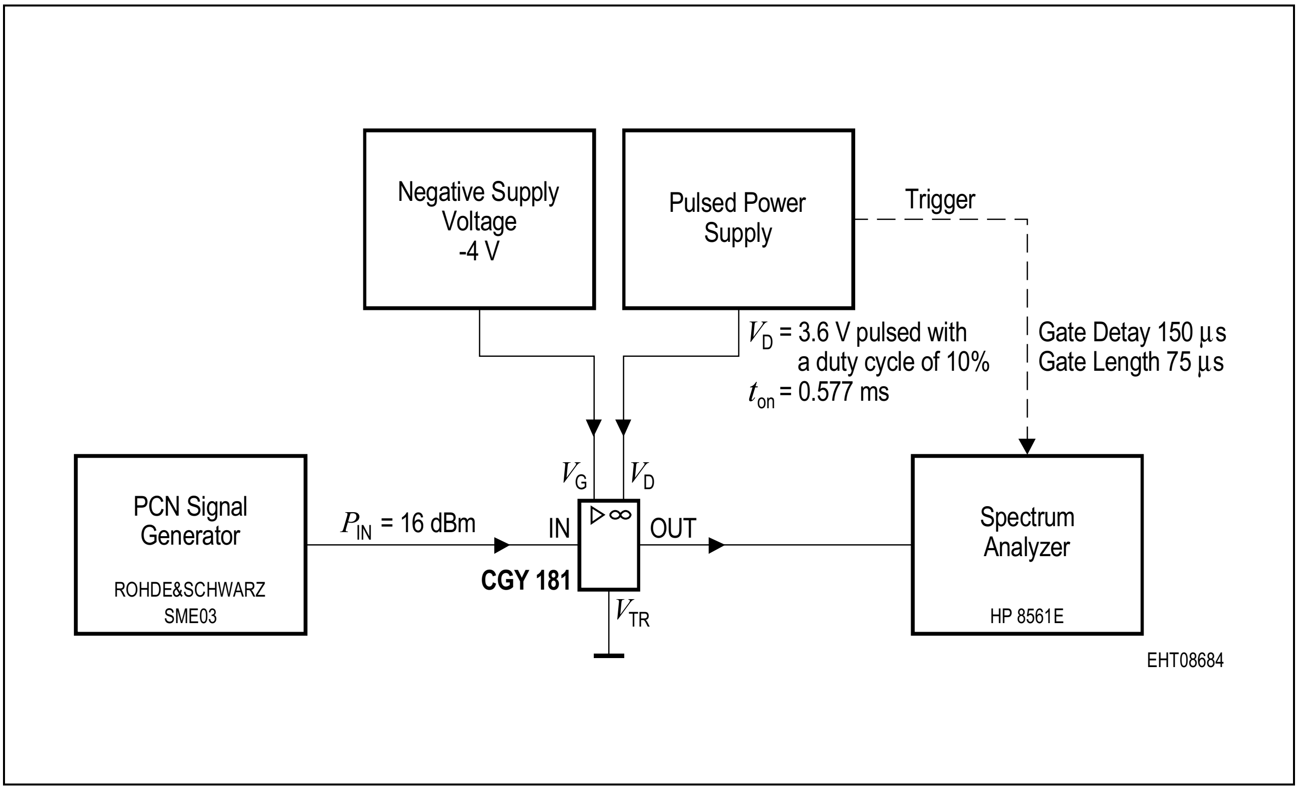


Figure 6 Measurement was Done with the Following Equipment

Application Hints

1. CW - Capability of the CGY 181

Proving the possibility of CW - operations there must be known the total power dissipation of the device. This value can be found as a function of temperature in the data sheet (**Page 9**). The CGY 181 has a maximum total power dissipation of P_{tot} = 5 W.

As an example we take the operating point with a drain voltage V_D = 3.6 V and a typical drain current of I_D = 1.2 A. So the maximum DC - power can be calculated to:

$$P_{DC} = V_D \times I_D = 4.32 \text{ W}$$

This value is smaller than 5 W and CW - operation is possible.

By decoupling RF power out of the CGY 181 the power dissipation of the device can be further reduced. Assuming a power added efficiency PAE of 35% the total power dissipation P_{tot} can be calculated using the following formula:

$$P_{tot} = P_{DC} \times (1 - \text{PAE}) = 4.32 \text{ W} \times (1 - 0.35) = 2.808 \text{ W}$$

2. Operation without Using the Internal Current Control

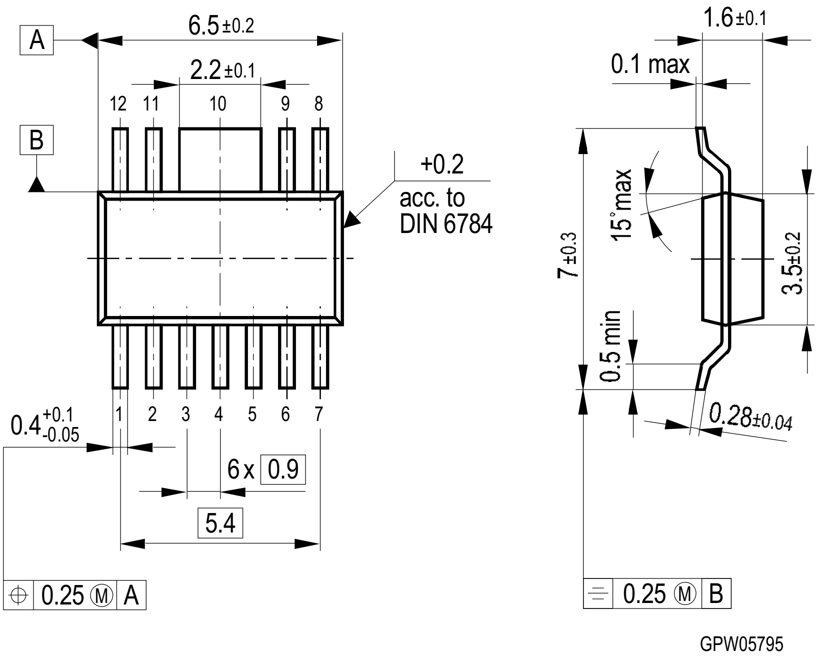
If you don’t want to use the internal current control, it is recommended to connect the negative gate voltage at pin 2 (V_{TR}) instead of pin 1 (V_G). In that case V_G is not connected.

3. Biasing and Use Considerations

Biasing should be timed in such a way that the gate voltage (V_G) is always applied before the drain voltages (V_D), and when returning to the standby mode, the drain voltages have to be removed before the gate voltage.

Package Outlines

MW-12
(Special Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm