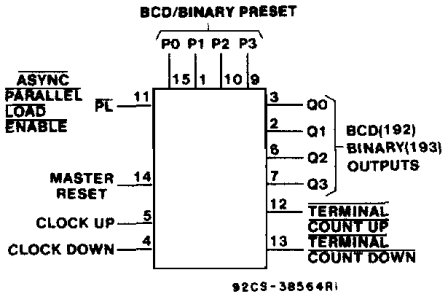
File Number **1674**

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Presettable Synchronous 4-Bit Up/Down Counters

CD54/74HC/HCT192 BCD Decade Counter, Asynchronous Reset

CD54/74HC/HCT193 4-Bit Binary Counter, Asynchronous Reset

Type Features:

- *Synchronous counting and asynchronous loading*
- *Two outputs for n-bit cascading*
- *Look-ahead carry for high-speed counting*

The RCA-CD54/74HC/HCT192/193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

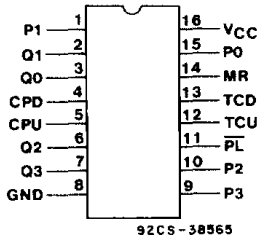
Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ($\overline{PL}$). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low-to-high transition of the Clock-Down input (and a high level on the Clock-Up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count Up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

The CD54HC/HCT192 and the CD54HC/HCT193 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT192 and CD74HC/HCT193 are supplied in 16-lead plastic dual-in-line packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT192 and the CD54/74HC/HCT193 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

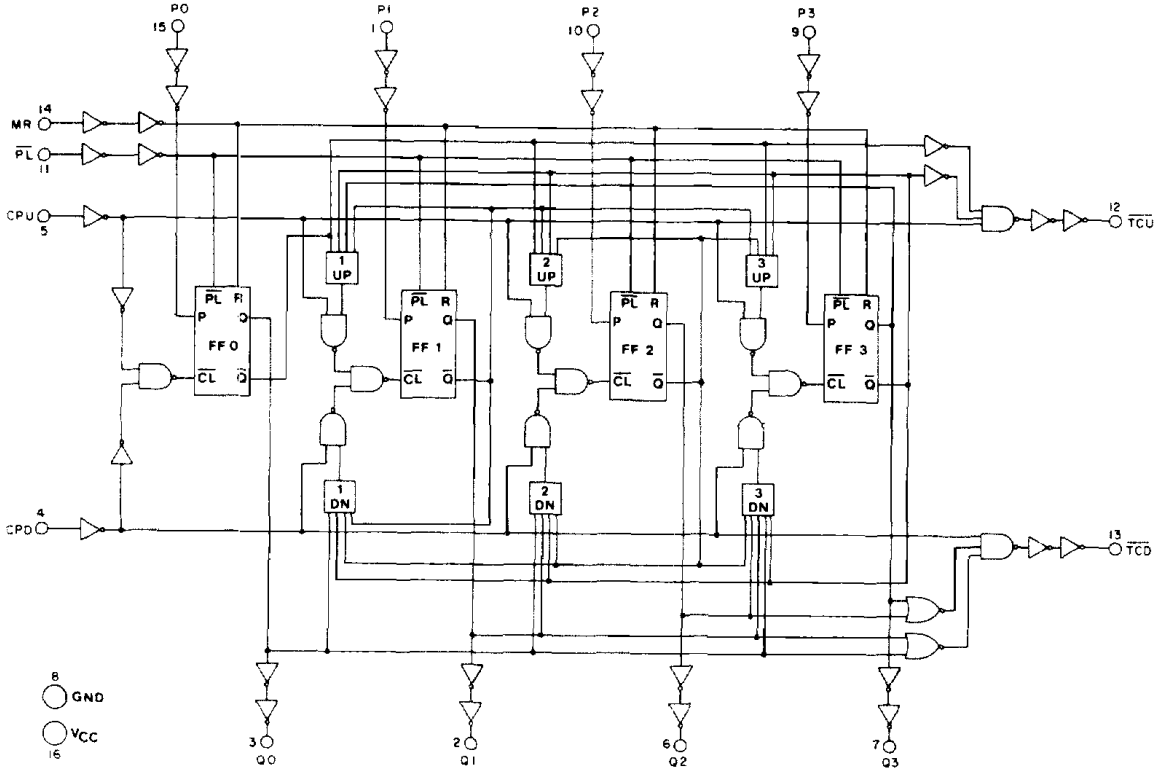
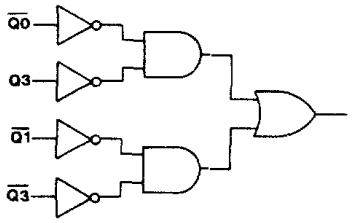
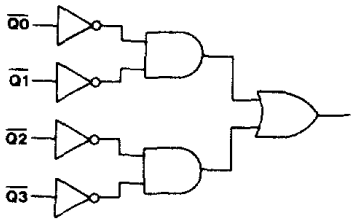


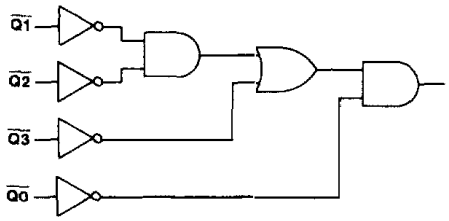
Fig. 1 - Logic diagram for HC/HCT192.



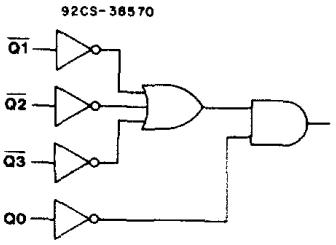
(a) Cell 1Up



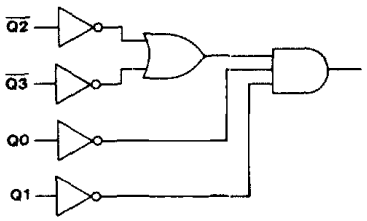
(b) Cell 2UP



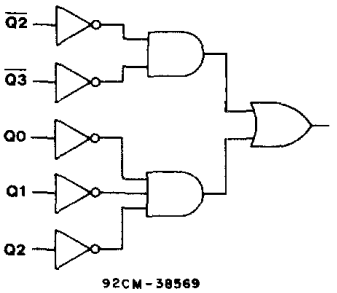
(c) Cell 3UP



(d) Cell 1Dn



(e) Cell 2Dn



(f) Cell 3Dr

Fig. 2 - CARRY logic cells for CD54/74HC/HCT192

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

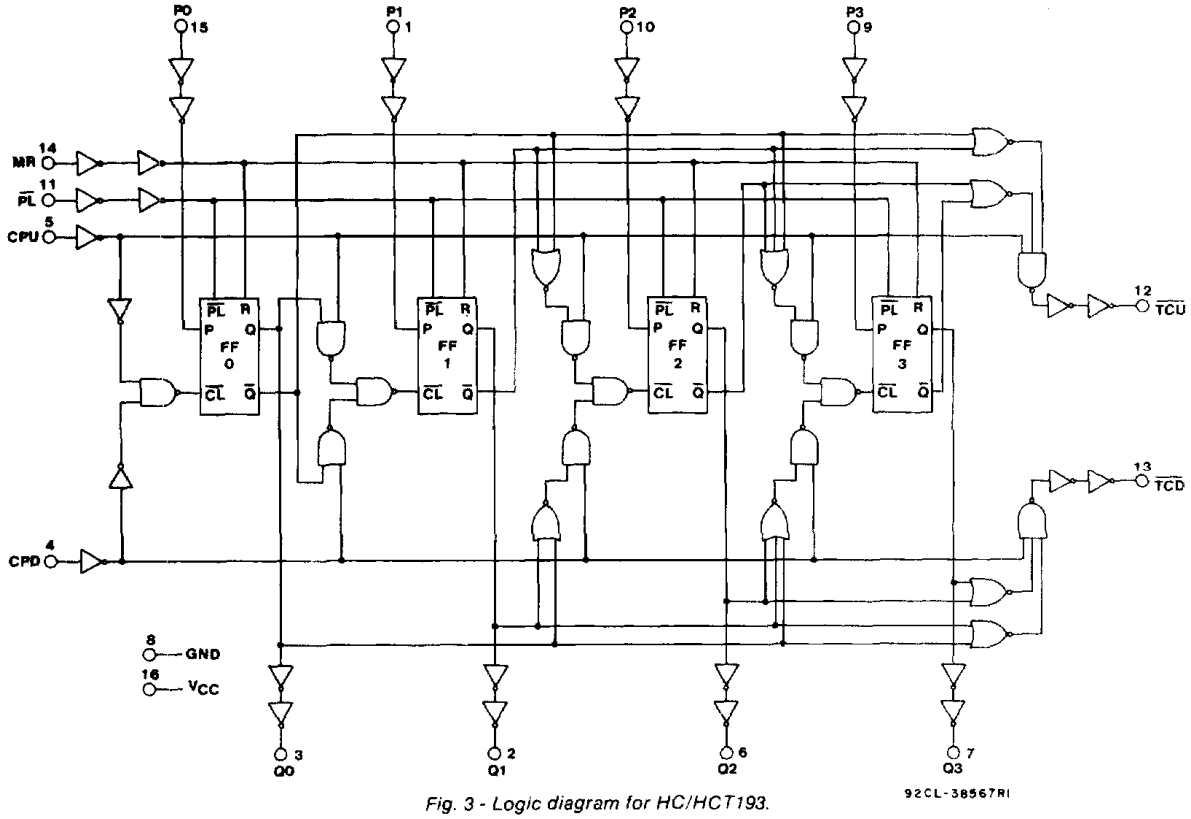


Fig. 3 - Logic diagram for HC/HCT193.

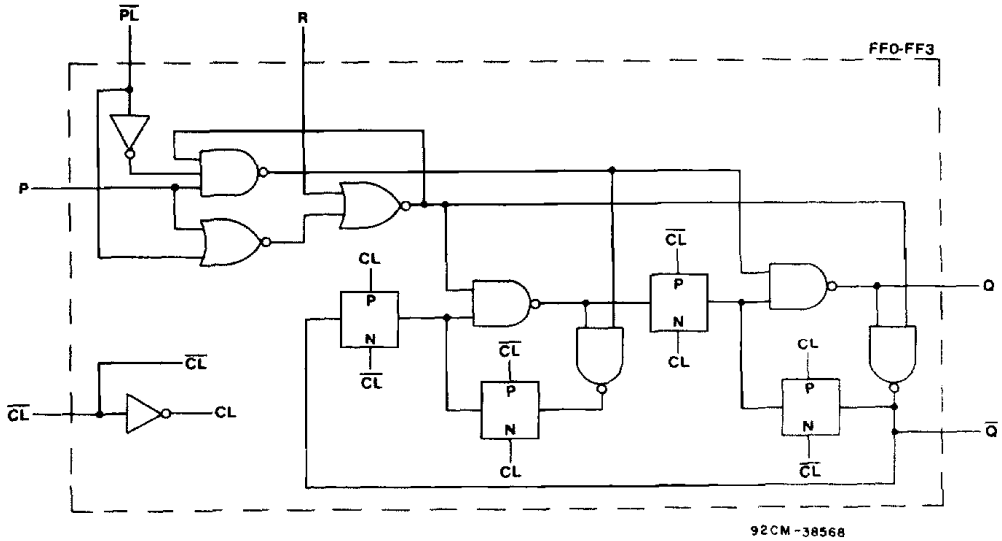


Fig. 4 - Logic diagram of flip-flops for HC/HCT192/193.

TRUTH TABLE

Clock Up	Clock Down	Reset	Parallel Load	Function
⎍	H	L	H	Count Up
H	⎍	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

⎍ = low-to-high transition
x = don't care

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_o < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC192/193CD54HC192/193										CD74HCT192/193/CD54HCT192/193									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
P0-P3	0.4
MR	1.45
$\overline{PL}$	0.85
CPU, CPD	1.45

*Unit load is Δ I_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL VALUES		UNITS
		HC	HCT	
Propagation Delay (C_L = 15 pF)				
CPU to $\overline{TCU}$ and CPD to $\overline{TCD}$	t_{PLH}	10	11	ns
CPU; CPD to Qn	t_{PHL}	18	17	
$\overline{PL}$ to Qn		18	21	
MR to Qn	t_{PHL}	17	18	
Power Dissipation Capacitance	C_{PD}*	40	50	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:
f_i=input frequency
f_o=output frequency
C_L=output load capacitance
V_{CC}=supply voltage

Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width:		2	115	—	—	—	145	—	—	—	175	—	—	—	ns
CPU, CPD	t_W	4.5	23	—	23	—	29	—	29	—	35	—	35	—	
192		6	20	—	—	—	25	—	—	—	30	—	—	—	
CPU, CPD		2	100	—	—	—	125	—	—	—	150	—	—	—	
		4.5	20	—	23	—	25	—	29	—	30	—	35	—	
193		6	17	—	—	—	21	—	—	—	26	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{PL}$	t_W	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	100	—	—	—	125	—	—	—	150	—	—	—	
MR	t_W	4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Setup Time		2	80	—	—	—	100	—	—	—	120	—	—	—	
Pn to $\overline{PL}$	t_{SU}	4.5	16	—	15	—	20	—	19	—	24	—	22	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time		2	0	—	—	—	0	—	—	—	0	—	—	—	
Pn to $\overline{PL}$	t_H	4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Hold Time		2	80	—	—	—	100	—	—	—	120	—	—	—	
CPD to CPU	t_H	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
or CPU to CPD		6	14	—	—	—	17	—	—	—	20	—	—	—	
Recovery Time		2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{PL}$ to CPU, CPD	t_{REC}	4.5	16	—	15	—	20	—	19	—	24	—	22	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	5	—	—	—	5	—	—	—	5	—	—	—	
MR to CPU, CPD	t_{REC}	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Maximum Frequency		2	5	—	—	—	4	—	—	—	3	—	—	—	
CPU, CPD	f_{MAX}	4.5	22	—	22	—	18	—	18	—	15	—	15	—	MHz
192		6	24	—	—	—	21	—	—	—	18	—	—	—	
CPU, CPD		2	5	—	—	—	4	—	—	—	3	—	—	—	
		4.5	25	—	22	—	20	—	18	—	17	—	15	—	
193		6	29	—	—	—	24	—	—	—	20	—	—	—	

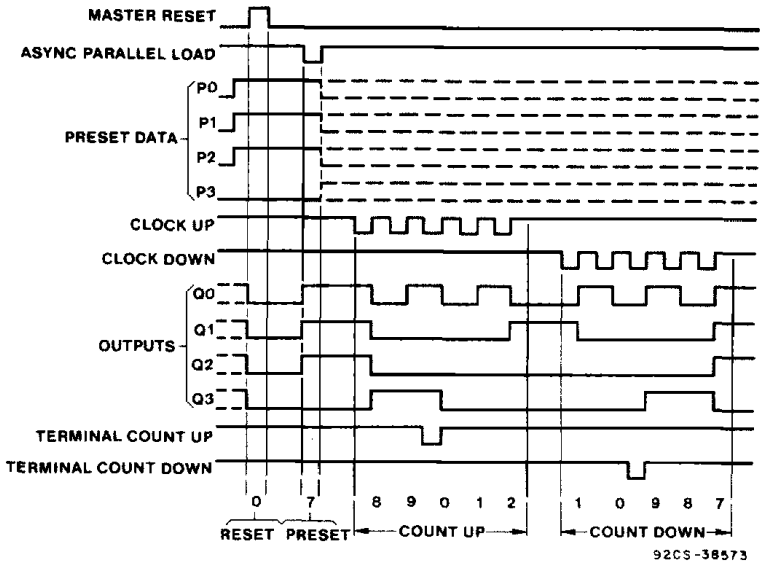
CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	
CPU to $\overline{TCU}$	t_{PHL}	4.5	—	25	—	27	—	31	—	34	—	38	—	41	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
CPD to $\overline{TCD}$		2	—	125	—	—	—	155	—	—	—	190	—	—	
		4.5	—	25	—	27	—	31	—	34	—	38	—	41	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
CPU to Qn		2	—	220	—	—	—	270	—	—	—	325	—	—	
		4.5	—	43	—	40	—	54	—	50	—	65	—	60	
		6	—	37	—	—	—	46	—	—	—	55	—	—	
CPD to Qn		2	—	220	—	—	—	270	—	—	—	325	—	—	
		4.5	—	43	—	40	—	54	—	50	—	65	—	60	
		6	—	37	—	—	—	46	—	—	—	55	—	—	
$\overline{PL}$ to Qn		2	—	220	—	—	—	275	—	—	—	330	—	—	
		4.5	—	44	—	46	—	55	—	58	—	66	—	69	ns
		6	—	37	—	—	—	47	—	—	—	56	—	—	
MR to Qn	t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	
		4.5	—	40	—	43	—	50	—	54	—	60	—	65	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Transition Time:	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Q, TCU, TCD	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

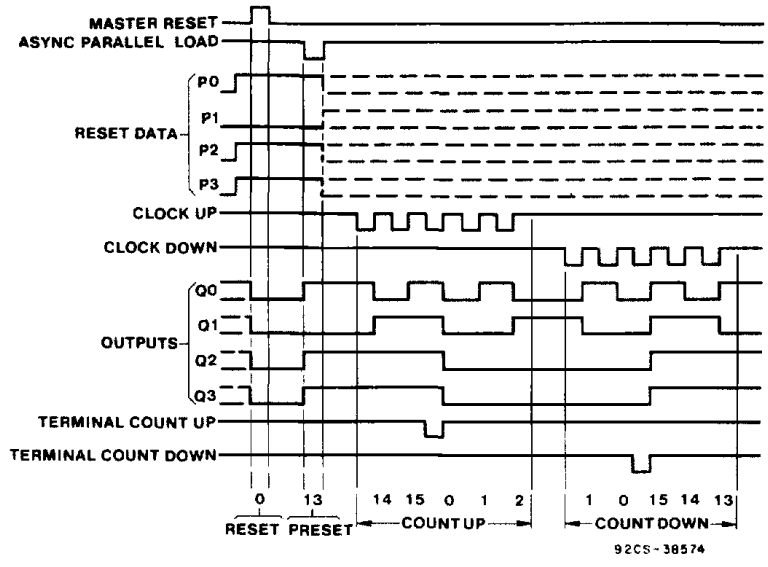
Sequences:
(1) Reset outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, terminal count up, zero, one and two.
(4) Count down to one, zero, terminal count down, nine, eight and seven.



(a) HC192 synchronous decade counters. Typical reset, preset and count sequences.

Sequences:
(1) Reset outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, terminal count up, zero, one and two.
(4) Count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

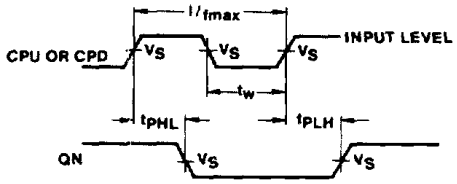
Note 1: Master reset overrides load data and clock inputs
Note 2: When counting up, clock-down input must be high; when counting down, clock-up input must be high



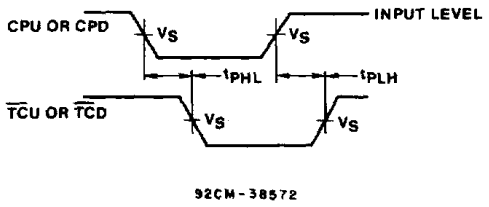
(b) HC193 synchronous binary counters. Typical reset, preset and count sequences.

Fig. 6 - Timing diagrams for the CD54/74HC/HCT192(a) and 193(b).

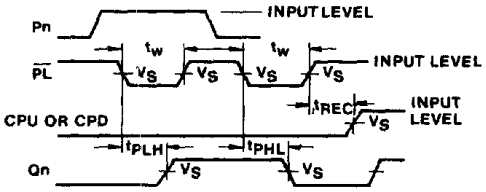
CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193



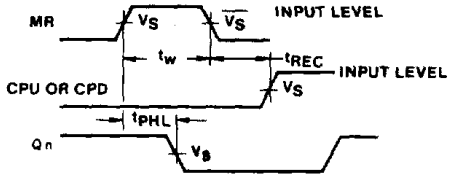
(a) *Clock to output delays and clock pulse width.*



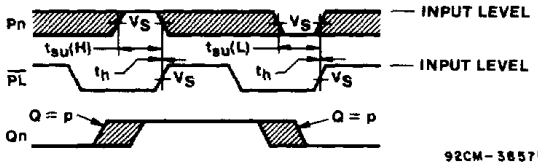
(b) *Clock to terminal count delays.*



(c) *Parallel load pulse width, parallel load to output delays, and parallel load to clock recovery time.*



(d) *Master reset pulse width, master reset to output delay and master reset to clock recovery time.*

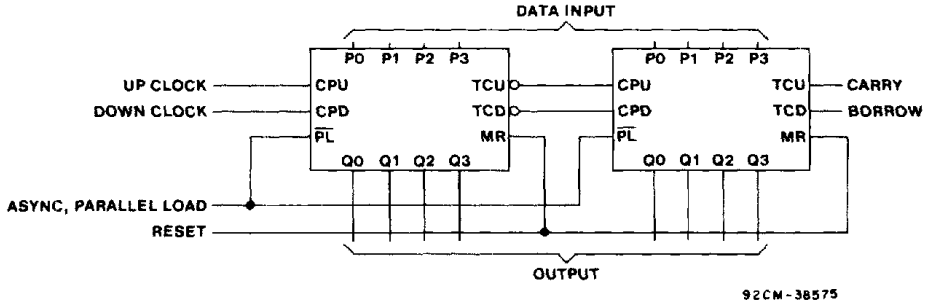


(e) *Setup and hold times data to parallel load (PL).*

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 5 - AC waveforms.

APPLICATION



CASCADED UP/DOWN COUNTER WITH PARALLEL LOAD

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

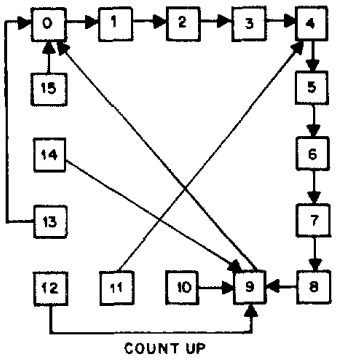


Fig. 6 - HC/HCT192 State Diagram.