

CD4086B Types

CMOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

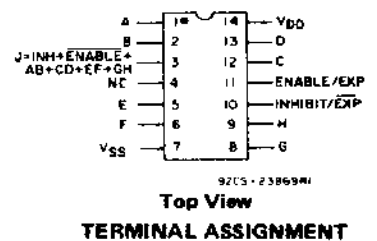
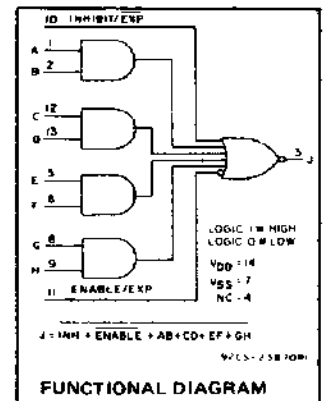
High-Voltage Types (20-Volt Rating)

The RCA-CD4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/EXP input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/EXP is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig.10 and its associated explanation for applications where a capability greater than 4-wide is required.

The CD4086B is supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation — t_{PHL} = 90 ns; t_{PLH} = 140 ns (typ.) at 10 V
- INHIBIT and ENABLE inputs
- Buffered outputs
- 100% tested for quiescent current at 20 V
- Maximum input leakage current of 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at V_{DD} = 5 V
 - 2 V at V_{DD} = 10 V
 - 2.5 V at V_{DD} = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD}) (Voltages referenced to V _{SS} Terminal)		-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS		-0.5 to V _{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT		±10 mA
POWER DISSIPATION PER PACKAGE (P _D):		
For T _A = -40 to +60°C (PACKAGE TYPE E)		500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C	to 200 mW
For T _A = -55 to +100°C (PACKAGE TYPES D, F, K)		500 mW
For T _A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C	to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)		100 mW
OPERATING-TEMPERATURE RANGE (T _A):		
PACKAGE TYPES D, F, K, H		-55 to +125°C
PACKAGE TYPE E		-40 to +85°C
STORAGE TEMPERATURE RANGE (T _{stg})		-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.58 ± 0.79 mm) from case for 10 s max.		+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range)	3	18	V

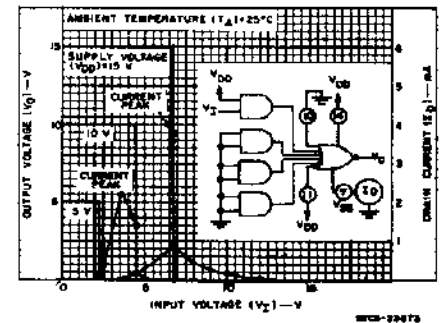


Fig. 1 - Typical voltage and current transfer characteristics.

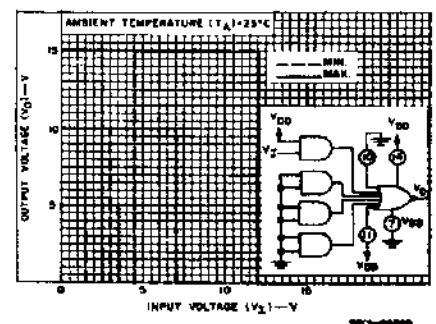


Fig. 2 - Minimum and maximum voltage transfer characteristics.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D, F, K, H Pkgs.				Values at -40, +25, +85 Apply to E Pkgs.			
				-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current I _{DD} Max.	-	0.5	5	1	1	30	30	-	0.02	1	μA
	-	0.10	10	2	2	60	60	-	0.02	2	
	-	0.15	15	4	4	120	120	-	0.02	4	
	-	0.20	20	20	20	600	600	-	0.04	20	
Output Low (Sink) Current, I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0.5	5		0.05			-	0	0.05	V
	-	0.10	10		0.05			-	0	0.05	
	-	0.15	15		0.05			-	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	-	0.5	5		4.95			4.95	5	-	
	-	0.10	10		9.95			9.95	10	-	
	-	0.15	15		14.95			14.95	15	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5		1.5			-	-	1.5	V
	1.9	-	10		3			-	-	3	
	1.5, 13.5	-	15		4			-	-	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5		3.5			3.5	-	-	
	1.9	-	10		7			7	-	-	
	1.5, 13.5	-	15		11			11	-	-	
Input Current, I _{IN} Max.	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

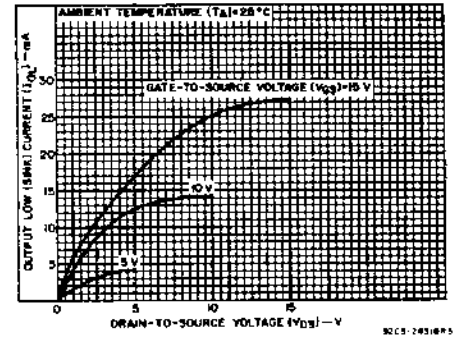


Fig. 3 - Typical output low (sink) current characteristics.

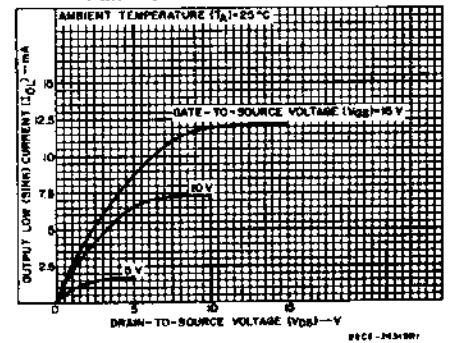


Fig. 4 - Minimum output low (sink) current characteristics.

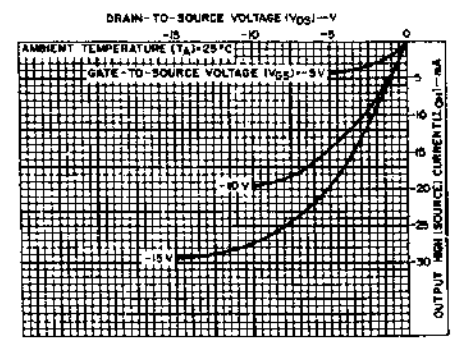


Fig. 5 - Typical output high (source) current characteristics.

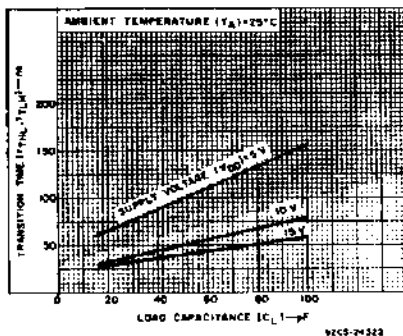


Fig. 6 - Typical transition time vs. load capacitance.

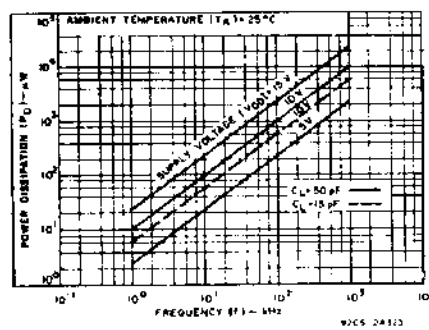


Fig. 7 - Typical power dissipation vs. frequency.

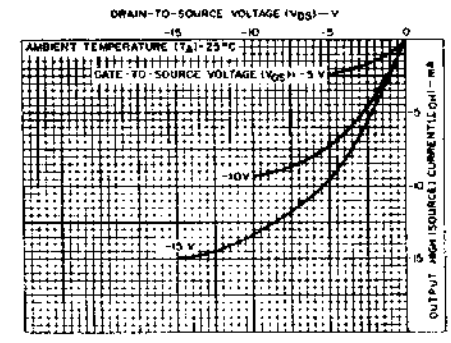


Fig. 8 - Minimum output high (source) current characteristics.

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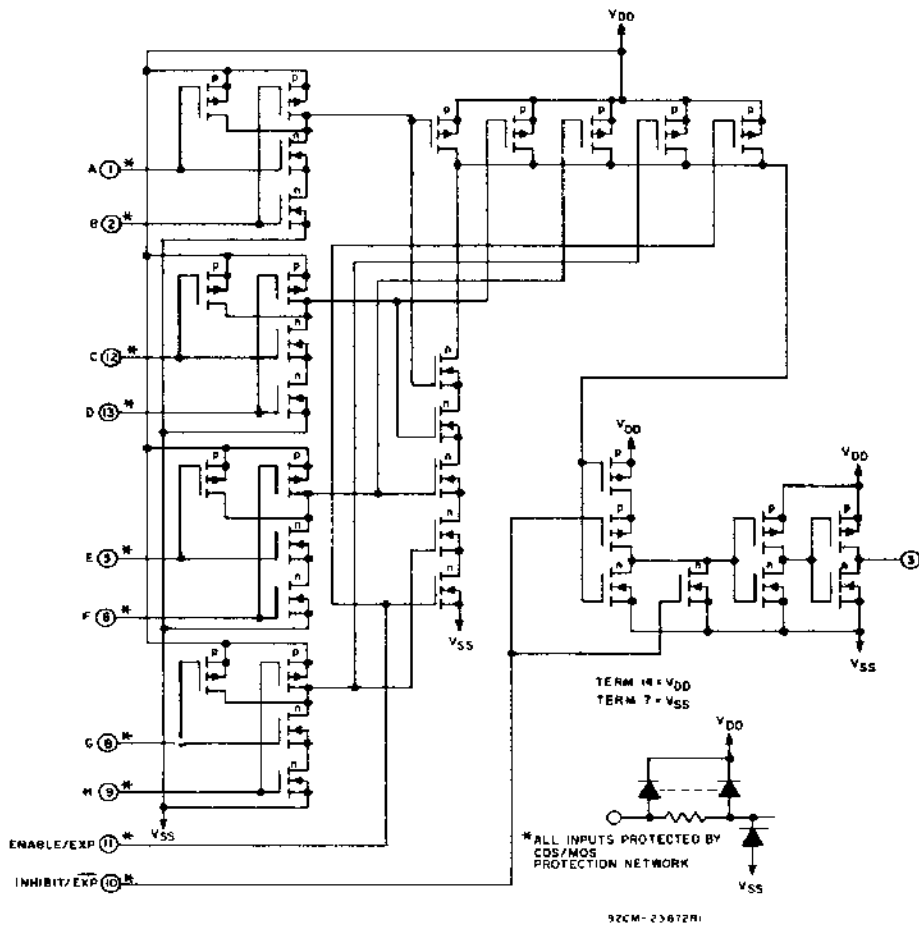


Fig. 9 - CD4086B schematic diagram.

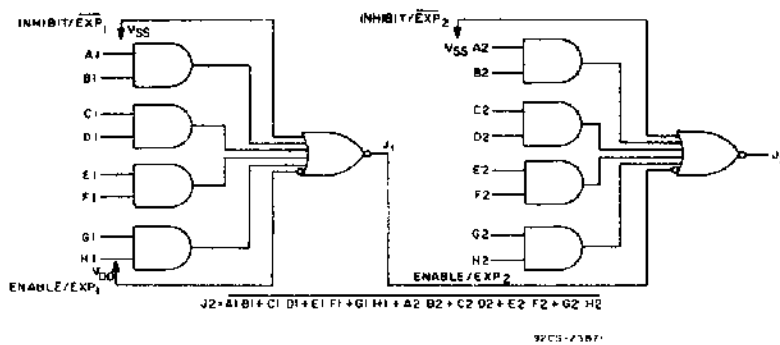


Fig. 10 - Two CD4086B's connected as an 8-wide 2-input A-O-I gate.

Fig. 10 above shows two CD4086B's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086B is fed directly to the ENABLE/EXP2 line of the second CD4086B. In a similar fashion, any

NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/EXP input with the same result.

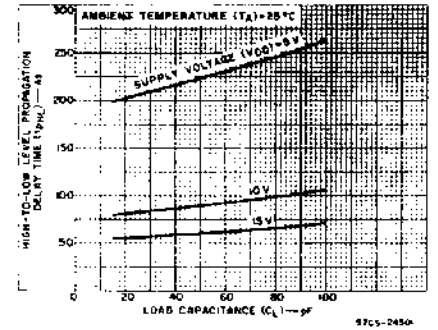


Fig. 11 - Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

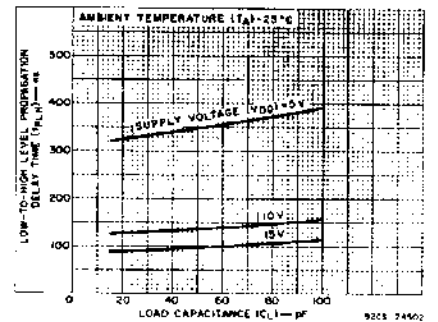


Fig. 12 - Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

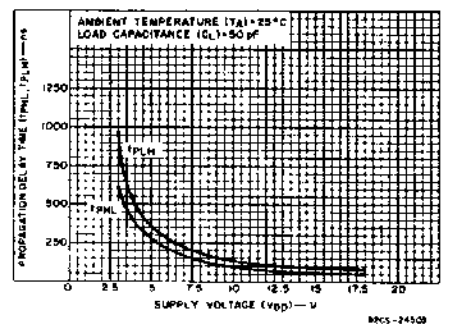


Fig. 13 - Typical DATA or ENABLE propagation delay time vs. supply voltage.

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DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ C$; Input $t_r, t_f = 20 ns$, $C_L = 50 pF$, $R_L = 200 k\Omega$

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS	
		V_{DD} (V)	TYP.		MAX.
Propagation Delay Time (Data): High-to-Low Level, t_{PHL}		5	225	450	ns
		10	90	180	
		15	60	120	
Low-to-High Level, t_{PLH}		5	310	620	ns
		10	125	250	
		15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level, $t_{PHL}(INH)$		5	150	300	ns
		10	60	120	
		15	40	80	
Low-to-High Level, $t_{PLH}(INH)$		5	250	500	ns
		10	100	200	
		15	70	140	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance C_{IN}	Any Input		5	7.5	pF

TEST CIRCUITS

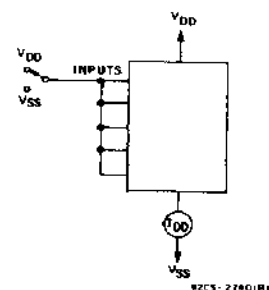


Fig. 14 – Quiescent device current.

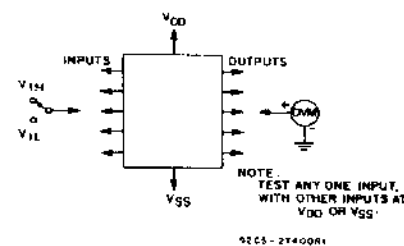
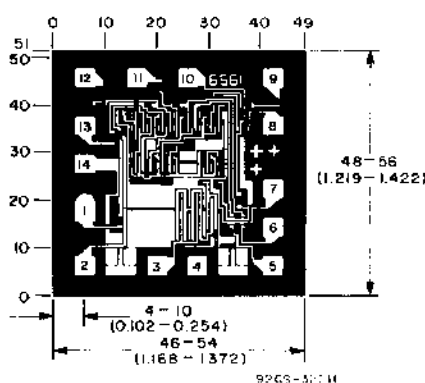


Fig. 15 – Input voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+15$ mils applicable to the nominal dimensions shown.

Dimensions and Pad Layout for the CD4086BH

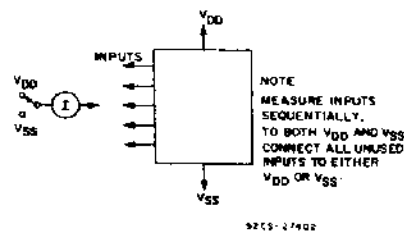


Fig. 16 – Input leakage current.