National Semiconductor

CD4073BM/CD4073BC
Double Buffered Triple 3-Input AND Gate
CD4075BM/CD4075BC
Double Buffered Triple 3-Input OR Gate

General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

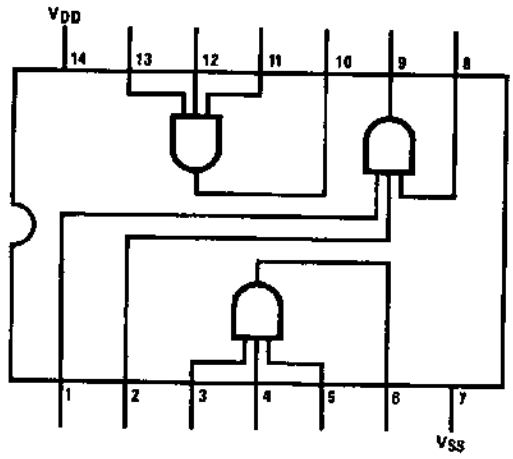
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams

Dual-In-Line Packages

CD4073 Triple 3-Input AND Gate



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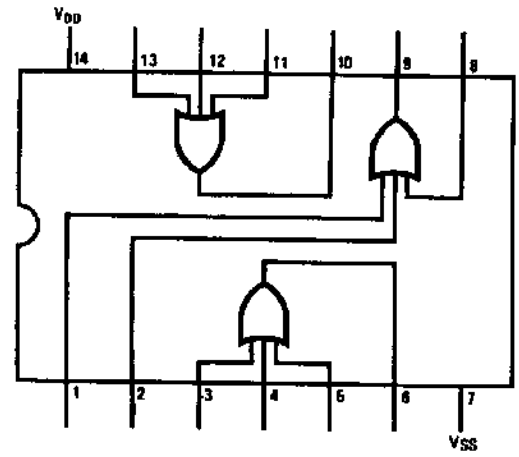
Top View

CD4075B Triple 3-Input OR Gate



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Top View

Order Number CD4073B* or CD4075B*

*Please look into Section 8, Appendix D for availability of various package types.

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Absolute Maximum Ratings (Notes 1 & 2)

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operation Conditions (Note 2)

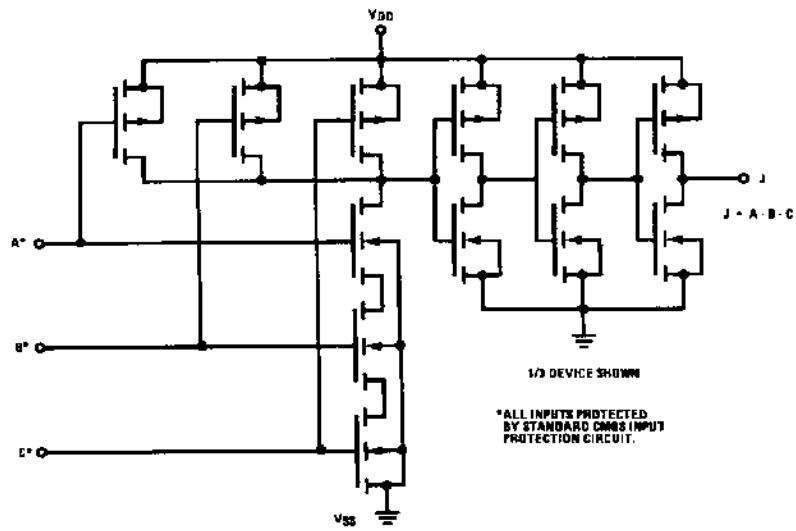
DC Supply Voltage (V_{DD})	$+5\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4073BM/CD4075BM	$-55°C$ to $+125°C$
CD4073BC/CD4075BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4073BM/CD4075BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		0.5		0.005	0.5		15	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ / $V_{DD} = 10V$ / $V_{DD} = 15V$; $\|I_O\| < 1\ \mu A$		0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ / $V_{DD} = 10V$ / $V_{DD} = 15V$; $\|I_O\| < 1\ \mu A$	4.95		4.95	5		4.95		V
			9.95		9.95	10		9.95		V
			14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ / $V_{DD} = 10V, V_O = 1.0V$ / $V_{DD} = 15V, V_O = 1.5V$; $\|I_O\| < 1\ \mu A$		1.5		2	1.5		1.5	V
				3.0		4	3.0		3.0	V
				4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$ / $V_{DD} = 10V, V_O = 9.0V$ / $V_{DD} = 15V, V_O = 13.5V$; $\|I_O\| < 1\ \mu A$	3.5		3.5	3		3.5		V
			7.0		7.0	6		7.0		V
			11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.2		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.2		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Schematic Diagram

CD4073BC



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DC Electrical Characteristics CD4073BC/CD4075BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.004	1		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.005	2		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V, $\lvert I_O \rvert$ < 1 μA		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V, $\lvert I_O \rvert$ < 1 μA		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V, $\lvert I_O \rvert$ < 1 μA		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V, $\lvert I_O \rvert$ < 1 μA	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V, $\lvert I_O \rvert$ < 1 μA	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V, $\lvert I_O \rvert$ < 1 μA	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.2		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

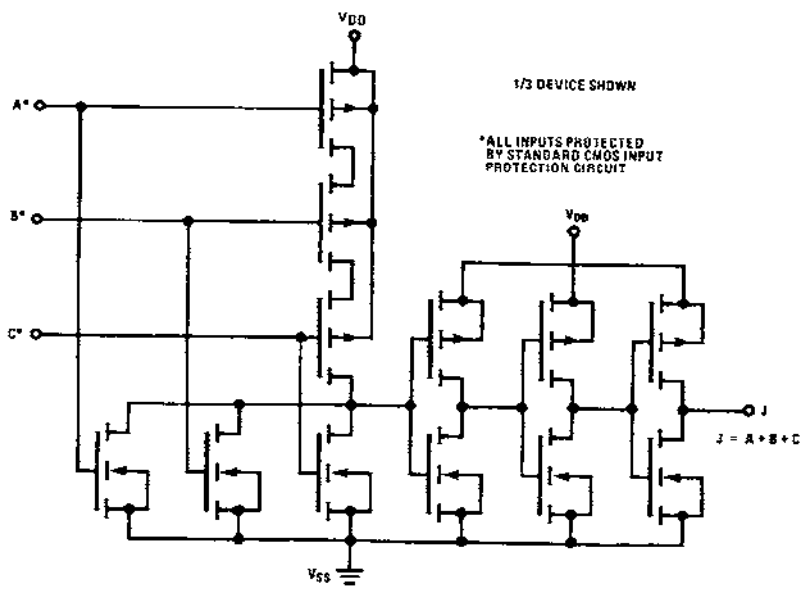
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified

Note 3: I_{OH} and I_{OL} are tested one output at a time

Schematic Diagram

CD4075BC



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AC Electrical Characteristics* CD4073BM/CD4073BC/CD4075BM/CD4075BC

T_A = 25°C, C_L = 50 pF, R_L = 200k unless otherwise specified

Symbol	Parameter	Conditions	CD4073BC CD4073BM			CD4075BC CD4075BM			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PHL}	Propagation Delay, High to Low Level	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		130 60 40	250 100 70		140 70 50	250 100 70	ns ns ns
t_{PLH}	Propagation Delay, Low to High Level	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		140 70 50	250 100 70		130 50 40	250 100 70	ns ns ns
t_{THL} t_{TLH}	Transition Time	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		90 50 40	200 100 80		90 50 40	200 100 80	ns ns ns
C_{IN}	Average Input Capacitance (Note 4)	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 5)	Any Gate		17			17		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.