QSpan (CA91L860B) & QSpan II (CA91L862A) Differences Summary

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1. Introduction

This document identifies the software and hardware changes between the QSpan II (CA91L862A) device and the QSpan (CA91L860B) device. This document is intended to be used for reference purposes and assumes the reader is familiar with the QSpan family of devices. It is the intent of this document to make the transition from QSpan to QSpan II an easier process for our customers. For more detail on the individual registers and their additional functionality, refer to the QSpan and QSpan II User Manual. The three sections Hardware, Software, and Backwards Compatibility will correspond to package differences (ie. new pins), QSpan II configuration (ie. new registers), functional differences (ie. anything relating to device operation).

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2. Hardware

The Hardware section will consist of package differences. For information on what functionality these new pins add to the QSpan II, please refer to the QSpan II User Manual. The new QSpan II pins are defined in Table 1 and the AC signalling characteristics are shown in Table 3. The redefined pin of QSpan II production part is defined in Table 2 and Chapter 4, note 4. Please note that for all inputs and bidirectional signals, there have been internal resistors added to allow these previous no-connect signals to be backwards compatible. If new designs do not want to use any new functionality, these signals can be left as no-connects.

Table 1: New Pin Descriptions in QSpan IIZ1

DP[3:0]	**Bidirectional**
Data Parity: provides the parity information for the data on D[31:0]. It is valid on the same clock as the data.	
ENUM#	**Open Drain Output**
Hot Swap Event Interrupt: notifies the PCI host that either a board has been inserted or is about to be extracted.	
EXT_GNT#[6:1]	**Output**
External Grant: used by the QSpan II to indicate to an external device that it has been granted access to the PCI bus	
EXT_REQ#[6:1]	**Bidirectional**
External Request: used by an external device to indicate to the QSpan II PCI bus arbiter that it wants ownership of the PCI bus. The QSpan II drives the unused EXT_REQ#[6:1] pins high when an external arbiter is used.	
$\overline{\text{HS\_HEALTHY}}$	**Input**
Hot Swap Healthy: QSpan II internally OR's this input with PCI reset (RST#) to determine when back-end power is stable.	
HS_LED	**Output**
Hot Swap LED Control: This signal is driven by QSpan II to control the status of the LED. The signal is driven low to turn on the LED during the hardware and software connection stages. The signal is tri-stated during normal operation to turn off the LED.	
HS_SWITCH	**Input**
Hot Swap Switch: QSpan II uses this input to monitor the state of the Hot Swap board ejector latch. A low value on this signal indicates that the ejector latch is open.	
PCI_ARB_EN	**Input**
PCI Arbiter Enable: If PCI_ARB_EN is sampled high at the negation of Reset, the QSpan II's PCI bus arbiter is enabled and will function as the PCI bus arbiter.	
PCI_DIS	**Input**
PCI Configuration Disable: This is a power-up option that makes the QSpan II hold off on ENUM# assertion and retry PCI configuration cycles to allow the Host processor to perform local configuration. QSpan II accepts PCI configuration cycles after the PCI_DIS bit is cleared in the MISC_CTL2 register.	
PME#	**Open Drain Output**
Power Management Event Interrupt: This signal is asserted to request a change in its current power management state and/or to indicate that a power management event has occurred.	
TEST1	**Input**
This is a manufacturing test input that should be left open. This pin has an internal pull-up resistor.	
TEST2	**Input**
This is a manufacturing test input that should be left open. This pin has an internal pull-down resistor.	
TEST3	**Input**
This is a manufacturing test input that should be left open. This pin has an internal pull-down resistor.	

Table 2: Redefined Pin Descriptions in QSpan II Production Part

VH (formerly VIO)	Power (V_{DD})
Highest Signalling Voltage: VH is connected to the highest voltage level that the QSpam II I/O's will observe on either the QBus or the PCI bus.	

Table 3: New Signal AC Characteristics

Pin Name	17 mm PBGA Ball #	27 mm PBGA Ball #	Type	Input Type	Output Type	Reset State	IOL (mA)	IOH (mA)	Interface	Signal Description
DP[0]	A5	C6	B	TTL	3S	Hi-Z	8	-8	QBus	Data Parity Lines
DP[1]	C5	B5								
DP[2]	B5	A4								
DP[3]	D4	C5								
ENUM#	G4	K1	O	-	OD	Hi-Z	8	-8	-	CompactPCI Hot Swap event output
EXT_GNT#[6:1]	See Manual	See Manual	O	PCI	3S	Hi-Z	-	-	PCI	External Grant
EXT_REQ#[6:1]	See Manual	See Manual	I	PCI	3S	Hi-Z	-	-	PCI	External Request
$\overline{\text{HS\_HEALTHY}}$	K4	N2	I	TTL (PD)	-	-	-	-	-	Hot Swap Healthy Signal
HS_LED	H2	L2	O	-	OD	Low	8	-8	-	LED control output for Hot Swap
HS_SWITCH	J2	L4	I	TTL (PD)	-	-	-	-	-	Switch input for Hot Swap
PCI_ARB_EN	C4	B4	I	TTL (PD)	-	-	-	-	PCI	Power up option to enable PCI Bus Arbiter
PCI_DIS	K3	M4	I	TTL (PD)	-	-	-	-	PCI	Power up option to disable PCI config accesses to QSpan II
PME#	J1	M2	O	-	OD	Hi-Z	8	-8	-	Power management event
TEST1	B12	B15	I	CMOS (PU)	-	-	-	-	-	Manufacturing Test Pin
TEST2	A14	D14	I	TTL (PD)	-	-	-	-	-	Manufacturing Test Pin
TEST3	C12	C15	I	TTL (PD)	-	-	-	-	-	Manufacturing Test Pin

3. Software

This section contains two tables. Table 4 explains new QSpan II register fields that were added to the existing QSpan registers. Table 5 represents all new registers and their fields within the QSpan II. The current part numbering scheme for the QSpan II has a Z or Z1 at the end of the part number that denotes the prototyping phase. The Z is the first prototype and Z1 is the second prototype of the QSpan II. When the QSpan IIZx becomes the production part, the Zx will be dropped from the part numbering scheme.

Table 4: Changed Registers

Register	Offset	Field	Bit(s)	QSpan IIZ1	QSpan IIZ	QSpan	Comment
PCI_ID	0x000	DID[15:0]	31:16	0x0862	0x0862	0x0860	Updated Device ID
PCI_CS	0x004	CAP_L	20	1	1	N/A	New field for VPD support
PCI_CLASS	0x008	RID[7:0]	7:0	0x01	0x00	0x02	Updated RID
PCI_BST0	0x018	PREF	3	0	0	N/A	Enable Prefetch Reads - loaded from EEPROM or QBus
PCI_BST1	0x01C	PREF	3	0	0	N/A	Enable Prefetch Reads - loaded from EEPROM or QBus
PCI_MISC1	0x03C	INT_PIN[0]	8	1	1	N/A	PCI Interrupt Pin. If equals 1 QSpan uses 1 PCI interrupt. If equals 0 QSpan uses no PCI interrupts.
PB_ERRCS	0x140	UNL_QSC	23	0	0	N/A	Unlock QBus Slave Channel
IDMA/DMA_CS	0x400	CHAIN	6	0	0	N/A	New field to select DMA mode
		DMA	5	0	0	N/A	New field to select DMA
INT_STAT	0x600	OFF_S	8	0	0	N/A	I2O - Outbound Free_List Full Status
		IPF_S	9	0	0	N/A	I2O - Inbound Free_List Full Status
		OFE_S	10	1	1	N/A	I2O - Outbound Free_List Empty Status
		IFE_S	11	1	1	N/A	I2O - Inbound Free_List Empty Status
		IPN_S	12	0	0	N/A	I2O - Inbound Post_List New Entry Interrupt Status
		OPNE_S	13	0	0	N/A	I2O - Outbound Post_List Not Empty Status
		PSC_IS	14	0	0	N/A	Power State Change Interrupt Status
		QDPE_S	15	0	N/A	N/A	QBus Data Parity Error Status
		MB0_IS	16	0	0	N/A	MailBox0 Interrupt Status
		MB1_IS	17	0	0	N/A	MailBox1 Interrupt Status
		MB2_IS	18	0	0	N/A	MailBox2 Interrupt Status
		MB3_IS	19	0	0	N/A	MailBox3 Interrupt Status

Register	Offset	Field	Bit(s)	QSpan IIZ1	QSpan IIZ	QSpan	Comment
INT_CTL	0x604	OFF_EN	8	0	0	N/A	I2O - Outbound Free_List Full Enable
		IPF_EN	9	0	0	N/A	I2O - Inbound Free_List Full Enable
		OFE_EN	10	0	0	N/A	I2O - Outbound Free_List Empty Enable
		IFE_EN	11	0	0	N/A	I2O - Inbound Free_List Empty Enable
		IPN_EN	12	0	0	N/A	I2O - Inbound Post_List New Entry Interrupt Enable
		OPNE_EN	13	0	0	N/A	I2O - Outbound Post_List Not Empty Enable
		PSC_EN	14	0	0	N/A	Power State Change Interrupt Enable
		QDPE_EN	15	0	N/A	N/A	QBus Data Parity Error Enable
		MB0_EN	16	0	0	N/A	MailBox0 Interrupt Enable
		MB1_EN	17	0	0	N/A	MailBox1 Interrupt Enable
		MB2_EN	18	0	0	N/A	MailBox2 Interrupt Enable
		MB3_EN	19	0	0	N/A	MailBox3 Interrupt Enable
INT_DIR	0x608	OFF_EN	8	0	0	N/A	I2O - Outbound Free_List Full Direction
		IPF_EN	9	0	0	N/A	I2O - Inbound Free_List Full Direction
		OFE_EN	10	0	0	N/A	I2O - Outbound Free_List Empty Direction
		IFE_EN	11	0	0	N/A	I2O - Inbound Free_List Empty Direction
		IPN_EN	12	0	0	N/A	I2O - Inbound Post_List New Entry Interrupt Direction
		OPNE_EN	13	1	1	N/A	I2O - Outbound Post_List Not Empty Direction
		PSC_EN	14	0	0	N/A	Power State Change Interrupt Direction
		QDPE_EN	15	0	N/A	N/A	QBus Data Parity Error Direction
		MB0_EN	16	0	0	N/A	MailBox0 Interrupt Direction
		MB1_EN	17	0	0	N/A	MailBox1 Interrupt Direction
		MB2_EN	18	0	0	N/A	MailBox2 Interrupt Direction
		MB3_EN	19	0	0	N/A	MailBox3 Interrupt Direction
QBSI0_CTL	0xF00	PREN	23	0	N/A	N/A	Prefetch Read Enable
QBSI1_CTL	0xF10	PREN	23	0	N/A	N/A	Prefetch Read Enable

Table 5: New Registers

Register	Offset	Field	Bit Location	QSpan IIZ1	QSpan IIZ	QSpan	Comment
I2O_BAR	0x010	BA	31-16	0	0	N/A	Exists when I2O_EN=1 in I2O_CS Register. PCI_BSM moves to 0x018
PCI_CP	0x034	CAP_PT	7-0	0xDC	0xDC	N/A	Capabilities Pointer
PCI_PMC	0x0DC	CAP_ID	7-0	0x01	0x01	N/A	Capability ID
		NXT_IP	15-8	0xE4	0xE4	N/A	Next Item Pointer
		PM_VER	18-16	001	001	N/A	Power Management Version
		PME_CLK	19	0	0	N/A	PME Clock
		APS	20	0	0	N/A	Auxillary Power Source
		DSI	21	0	0	N/A	Device Specific Initialization
		D1_SP	25	0	0	N/A	D1 Support
		D2_SP	26	0	0	N/A	D2 Support
		PME_SP	31-27	0	0	N/A	PME Support
PCI_PMCS	0x0E0	PWR_ST	1-0	0	0	N/A	Power State
		PME_EN	8	0	0	N/A	PME Enable
		PME_ST	15	0	0	N/A	PME Status
		P2P_BSE	23-16	0	0	N/A	PCI to PCI support extensions
CPCI_HS	0x0E4	CAP_ID	7-0	0x06	0x06	N/A	Capability ID
		NXT_IP	15-8	0	0	N/A	Next Item Pointer
		EIM	17	0	0	N/A	ENUM# Interrupt Mask
		LOO	19	0	0	N/A	LED On/Off
		EXT	22	0	0	N/A	ENUM# Status - Extraction
		INS	23	0	0	N/A	ENUM# Status - Insertion
PCI_VPD	0x0E8	CAP_ID	7-0	0x03	0x03	N/A	Capability ID
		NXT_IP	15-8	0	0	N/A	Next Item Pointer
		VPD_ADDR	23-16	0	0	N/A	VPD Address
		VPD_F	31	0	0	N/A	VPD Flag
VPD_DATA	0x0EC	VPD_DATA	31-0	0	0	N/A	VPD Data

Register	Offset	Field	Bit Location	QSpan IIZ1	QSpan IIZ	QSpan	Comment
I2O_CS	0x200	I2O_EN	0	0	0	N/A	I2O Enable
		RR_BP	1	0	0	N/A	Register Read of Bottom Pointer
		FIFO_SIZE	6-4	0	0	N/A	Specifies the size of the circular FIFO
		OP_F	8	0	0	N/A	Outbound Post List FIFO Full
		OF_F	9	0	0	N/A	Outbound Free List FIFO Full
		IP_F	10	0	0	N/A	Inbound Post List FIFO Full
		IF_F	11	0	0	N/A	Inbound Free List FIFO Full
		OP_E	12	1	1	N/A	Outbound Post List FIFO Empty
		OF_E	13	1	1	N/A	Outbound Free List FIFO Empty
		IP_E	14	1	1	N/A	Inbound Post List FIFO Empty
		IF_E	15	1	1	N/A	Inbound Free List FIFO Empty
		QIBA	31-20	0	0	N/A	QBus I2O Base Address
IIF_TP	0x204	IF_TP	19-2	0	0	N/A	Inbound Free List Top Pointer
		QIBA	31-20	0	0	N/A	QBus I2O Base Address (specified in I2O_CS)
IIF_BP	0x208	IF_BP	19-2	0	0	N/A	Inbound Free List Bottom Pointer
		QIBA	31-20	0	0	N/A	QBus I2O Base Address (specified in I2O_CS)
IIP_TP	0x20C	IP_TP	19-2	0	0	N/A	Inbound Post List Top Pointer
		QIBA	31-20	0	0	N/A	QBus I2O Base Address (specified in I2O_CS)
IIP_BP	0x210	IP_BP	19-2	0	0	N/A	Inbound Post List Bottom Pointer
		QIBA	31-20	0	0	N/A	QBus I2O Base Address (specified in I2O_CS)
IOF_TP	0x214	OF_TP	19-2	0	0	N/A	Outbound Free List top Pointer
		QIBA	31-20	0	0	N/A	QBus I2O Base Address (specified in I2O_CS)
IOF_BP	0x218	OF_BP	19-2	0	0	N/A	Outbound Free List Bottom Pointer
		QIBA	31-20	0	0	N/A	QBus I2O Base Address (specified in I2O_CS)
IOP_TP	0x21C	OP_TP	19-2	0	0	N/A	Outbound Post List Top Pointer
		QIBA	31-20	0	0	N/A	QBus I2O Base Address (specified in I2O_CS)
IOP_BP	0x220	OP_BP	19-2	0	0	N/A	Outbound Post List Bottom Pointer
		QIBA	31-20	0	0	N/A	QBus I2O Base Address (specified in I2O_CS)
DMA_QADD	0x40C	Q_ADDR	31-2	0	0	N/A	QBus Address for DMA Transfers

Register	Offset	Field	Bit Location	QSpan IIZ1	QSpan IIZ	QSpan	Comment
DMA_CS	0x410	STOP_STAT	6	0	0	N/A	DMA Stop Status
		STOP	7	0	0	N/A	DMA Stop
		CP_LOC	8	0	0	N/A	Command Packet Location
		MDBS	9	0	N/A	N/A	Maximum DMA Burst Size on QBus
		BRSTEN	14	0	0	N/A	QBus Burst Enable
		BURST_4	15	0	0	N/A	QBus Burst Four Data Phases
		Q_OFF	18-16	0	0	N/A	DMA QBus Off Counter
		IWM	23-20	0	0	N/A	Programmable I-FIFO Watermark
		INVEND	24	0	0	N/A	Invert Endianess
		DSIZE	26-25	0	0	N/A	QBus destination Port Size
		DIR	27	0	0	N/A	DMA Direction
		TC	31-28	0	0	N/A	QBus Transaction Code
DMA_CPP	0x414	CPP	31-4	0	0	N/A	DMA Command Packet Pointer
MISC_CTL2	0x808	QINT_PME	0	0	0	N/A	QINT Assertion in D3hot Power State Generates PME#
		PSC_QRST	1	0	0	N/A	Power State Change causes QBus Reset
		NOTO	2	0	N/A	N/A	No Transaction Ordering
		EEPROM_ACC	3	0	N/A	N/A	EEPROM Access after Power-up
		QBUS_PAR	4	0	N/A	N/A	QBus Parity Encoding
		QSC_PW	8	0	0	N/A	QBus Slave Channel Posted Write Optimization
		REG_AC	9	0	0	N/A	Register Access Control
		PRCNT2	15:10	000001	N/A	N/A	Prefetch Read Byte Count 2
		PR_SING	16	0	0	N/A	QBus Prefetch Single Data Phase
		BURST_4	17	0	0	N/A	QBus Burst four Data Phases
		TA_BE_EN	18	0	0	N/A	PCI Target Abort - Bus Error mapping Enable
		PTC_PD	19	0	N/A	N/A	PCI Target Channel Prefetch Disconnect
		MAX_RTRY	21:20	0	N/A	N/A	Max. # of retries by QSpan II master on PCI
		KEEP_BB	22	0	N/A	N/A	Keep /BB asserted for back-to-back cycles
		PTB_IB	23	0	N/A	N/A	PCI Target Channel Prefetch Count Image Based
		PCI_DIS	31	0	0	N/A	PCI Access Disabled
PARB_CTL	0x810	BM_PARK	2-0	0	N/A	N/A	Select Master for PCI Bus parking
		PARK	3	0	N/A	N/A	PCI Bus parking scheme
		PARB_EN	7	Power-up option	N/A	N/A	PCI Bus Arbiter Enable
		QS_PRI	8	0	N/A	N/A	Arbitration Level for QSpan
		Mx_PRI	15-9	0	N/A	N/A	Arbitration level for PCI master device x.

Register	Offset	Field	Bit Location	QSpan IIZ1	QSpan IIZ	QSpan	Comment
I2O_OPIS	0x030	OP_ISR	3	0	0	N/A	Outbound Post List Interrupt Service Request
I2O_OPIM	0x034	OP_IM	3	1	1	N/A	Outbound Post List Interrupt Mask
I2O_INQ	0x040	IN_Q	31-0	0	0	N/A	I2O Inbound Queue
I2O_OUTQ	0x044	OUT_Q	31-0	0	0	N/A	I2O Outbound Queue

4. Backwards Compatibility

This section deals with potential operability issues that may be encountered or avoided due to functionality changes. Please find the description of the changes below.

1. $\overline{BR}$ Negation During Burst Transfers

This compatibility issue will only affect your application if an external arbiter has been implemented on the QBus and the $\overline{BR}$ signal is used to decode burst transfers in the arbiter logic. For QSpan (CA91L860B, CA91C860B) burst transfers the $\overline{BR}$ signal will be negated from the same rising clock edge as the negation of $\overline{BB}$. However, for QSpan II (CA91L862A) burst transfers the $\overline{BR}$ signal will be negated from the rising clock edge that samples the $\overline{BG}$ signal low.

2. $\overline{BR}$ During Reset

This issue will only affect your application if an external arbiter is being implemented on the QBus. The QSpan (CA91L860B, CA91C860B) will drive $\overline{BR}$ high while being held in reset. The QSpan II (CA91L862A) will tristate $\overline{BR}$ while being held in reset and drive $\overline{BR}$ high two clock cycles after reset has negated. The arbiter should not be designed to sample $\overline{BR}$ until two clock cycles after the negation of reset, otherwise $\overline{BR}$ may be sampled low resulting in the arbiter asserting $\overline{BG}$ to the QSpan II (CA91L862A) and hanging the system.

3. QDPE_S Bit Set in the INT_STAT (0x600) Register

The QSpan IIZ1 (CA91L862A-xxxxZ1) has the ability to monitor QBus data parity. The DP[3:0] lines were defined as no connects (N/C) in all previous revisions of the QSpan (CA91L860B) and QSpan II (CA91C862A-xxxxZ). If data parity support is not implemented when migrating to the QSpan IIZ1 (CA91L862A-xxxxZ1) the QDPE_S bit (bit 15) will be set when data is transferred through the QSpan IIZ1 (CA91L862A-xxxxZ1). Therefore, the applications interrupt service routine (ISR) must ignore the QDPE_S bit in the INT_STAT register.

4. Redefinition of VIO to VH pin.

The QSpan (CA91L860B-xxCE) and QSpan IIZ/Z1 (CA91L862A-xxCEZx) define pin R3 as VIO. Pin R3 has been redefined in the QSpan II production part (CA91L862A-xxCE) as VH. This change may impact some board designs.

The QSpan/QSpan IIZ/QSpan IIZ1 defines VIO as an input pin. The VIO pin is used to determine the PCI signalling characteristics. This implementation restricts the power up sequencing of the device. If 5V is applied to the VIO pin, then the 3.3V power ramp must occur before the 5V power to ensure the current specification for the VIO pin is not exceeded. The current may be limited to VIO through an external series resistor.

The QSpan II production part defines VH (Highest I/O voltage) as a power pin. This implementation removes the restriction on power sequencing. VH must be connected to the highest voltage level that the QSpan II I/O's will observe on either the QBus or the PCI Bus (see Table 6). The QSpan II production part contains Universal PCI Buffers. As a result, the signalling characteristics of the QSpan II production part will operate in both a 5V and 3.3V signalling environment.

Table 6: Voltage required to be applied to VH

PCI Bus Voltage (V)	QBus Voltage (V)	VH Voltage (V)
3.3	3.3	3.3
5	5	5
3.3	5	5
5	3.3	5
VIO*	3.3	VIO*
VIO*	5	5

*VIO denotes the signal connection to the PCI bus connector for Universal Signalling.

The transition to the QSpan II production part will require you to review the current board design. This may require a change to your assembly instructions/BOM (ie. requirement to change resistor value) or worst case require a change to the PCB (or strap added) The key areas to review will be:

- the value of the current limiting resistor on VIO
- the voltage that is applied to VH/VIO pin on QSpan
- the highest I/O voltage level the QSpan II production part will observe

Please see Table 7 for the full details on the required actions for each possible design implementation. The yellow rows within Table 2 indicate the majority of designs that will be impacted, provided the previously defined requirements for VIO (R3 on device) were implemented.

Table 7: Implications of VIO/VH redefinition.

Current VIO Connection	PCI Bus Voltage (V)	QBus Voltage (V)	Required Action for VH Connection
Directly to 3.3V	3.3	3.3	Leave as is.
	3.3	5	Connect VH directly to 5V
	5	3.3	Connect VH directly to 5V
	5	5	Connect VH directly to 5V
	VIO*	3.3	Connect VH directly to VIO*
	VIO*	5	Connect VH directly to 5V
Series resistor to 3.3V	3.3	3.3	Replace with 0 ohm resistor
	3.3	5	Remove the resistor Connect VH directly to 5V
	5	3.3	Replace with 0 ohm resistor Connect VH directly to 5V
	5	5	Replace with 0 ohm resistor Connect VH directly to 5V
	VIO*	3.3	Replace with 0 ohm resistor Connect VH directly to VIO*
	VIO*	5	Remove the resistor Connect VH directly to 5V
Directly to 5V	3.3	3.3	Connect VH directly to 3.3V
	3.3	5	Leave as is.
	5	3.3	Leave as is.
	5	5	Leave as is.
	VIO*	3.3	Connect VH directly to VIO*
	VIO*	5	Leave as is.
Series resistor to 5V	3.3	3.3	Replace with 0 ohm resistor Connect VH directly to 3.3V
	3.3	5	Replace with 0 ohm resistor
	5	3.3	Replace with 0 ohm resistor
	5	5	Replace with 0 ohm resistor
	VIO*	3.3	Replace with 0 ohm resistor Connect VH directly to VIO*
	VIO*	5	Replace with 0 ohm resistor
Directly to VIO*	3.3	3.3	Connect VH directly to VIO*
	3.3	5	Connect VH directly to 5V
	5	3.3	Connect VH directly to 5V
	5	5	Connect VH directly to 5V
	VIO*	3.3	Leave as is.
	VIO*	5	Connect VH directly to 5V

Current VIO Connection	PCI Bus Voltage (V)	QBus Voltage (V)	Required Action for VH Connection
Series resistor to VIO*	3.3	3.3	Replace with 0 ohm resistor Connect VH directly to VIO*
	3.3	5	Replace with 0 ohm resistor Connect VH directly to 5V
	5	3.3	Replace with 0 ohm resistor Connect VH directly to 5V
	5	5	Replace with 0 ohm resistor Connect VH directly to 5V
	VIO*	3.3	Replace with 0 ohm resistor
	VIO*	5	Replace with 0 ohm resistor Connect VH directly to 5V

*VIO denotes the signal connection to the PCI bus connector for Universal Signalling.