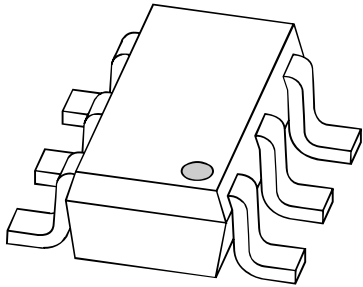


# DATA SHEET



## **BZA462A**

**Quadruple ESD transient voltage  
suppressor**

Product specification  
Supersedes data of 1998 Oct 30

1999 May 25

# Quadruple ESD transient voltage suppressor

# BZA462A

### FEATURES

- ESD rating >15 kV, according to IEC1000-4-2
- SOT457 surface mount package
- Common anode configuration
- Non-clamping range -0.5 to 6.2 V
- Maximum reverse peak power dissipation:  
24 W at  $t_p = 1$  ms
- Maximum clamping voltage at peak pulse current:  
9 V at  $I_{ZSM} = 2.66$  A.

### APPLICATIONS

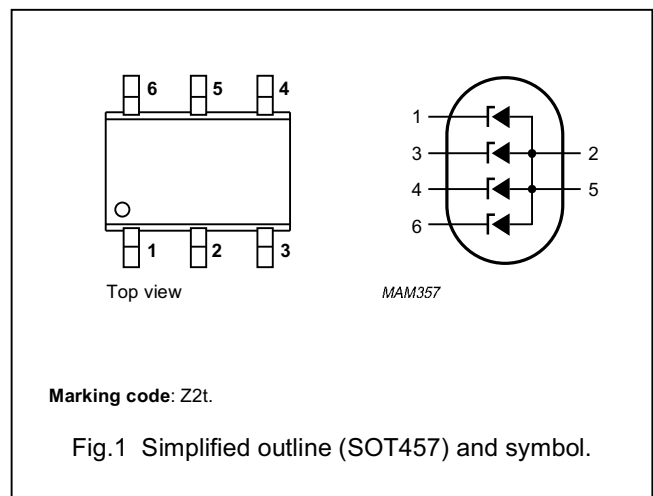
- Computers and peripherals
- Audio and video equipment
- Communication systems
- Medical equipment.

### DESCRIPTION

Monolithic transient voltage suppressor diode in a six lead SOT457 (SC-74) package for 4-bit wide ESD transient suppression at 6.2 V level.

### PINNING

PIN	DESCRIPTION
1	cathode 1
2	common
3	cathode 2
4	cathode 3
5	common
6	cathode 4



### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per diode</b>					
$I_Z$	working current	$T_s = 60$ °C; note 1	-	note 2	mA
$I_F$	continuous forward current	$T_s = 60$ °C	-	100	mA
$I_{FSM}$	non-repetitive peak forward current	$t_p = 1$ ms; square pulse	-	3.75	A
$I_{ZSM}$	non-repetitive peak reverse current	$t_p = 1$ ms; square pulse; see Fig.2	-	2.66	A
$P_{tot}$	total power dissipation	$T_s = 60$ °C; see Fig.3	-	720	mW
$P_{ZSM}$	non repetitive peak reverse power dissipation	square pulse; $t_p = 1$ ms; see Fig.4	-	24	W
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-65	+150	°C

### Notes

1.  $T_s$  is the temperature at the soldering point of the anode pin.
2. DC working current limited by  $P_{tot\ max}$ .

# Quadruple ESD transient voltage suppressor

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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	one or more diodes loaded	125	K/W

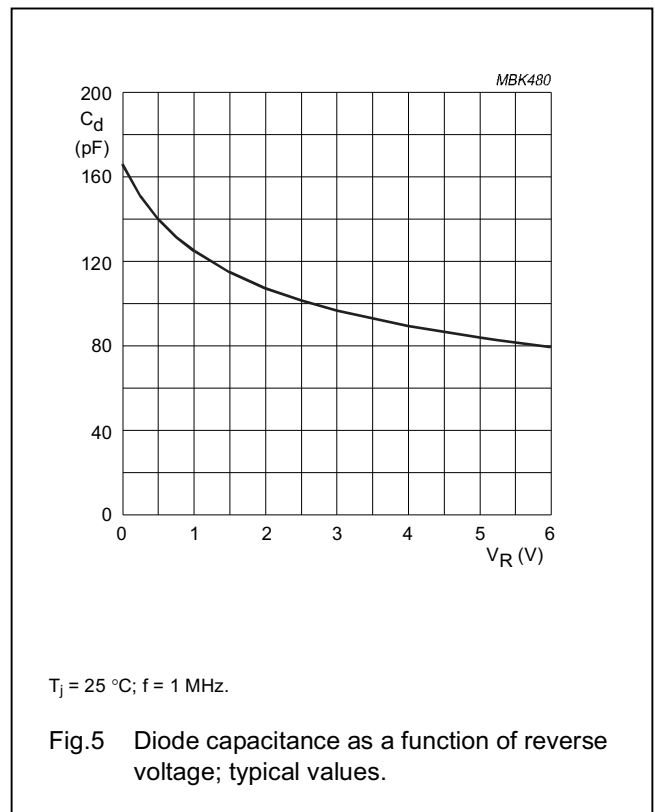
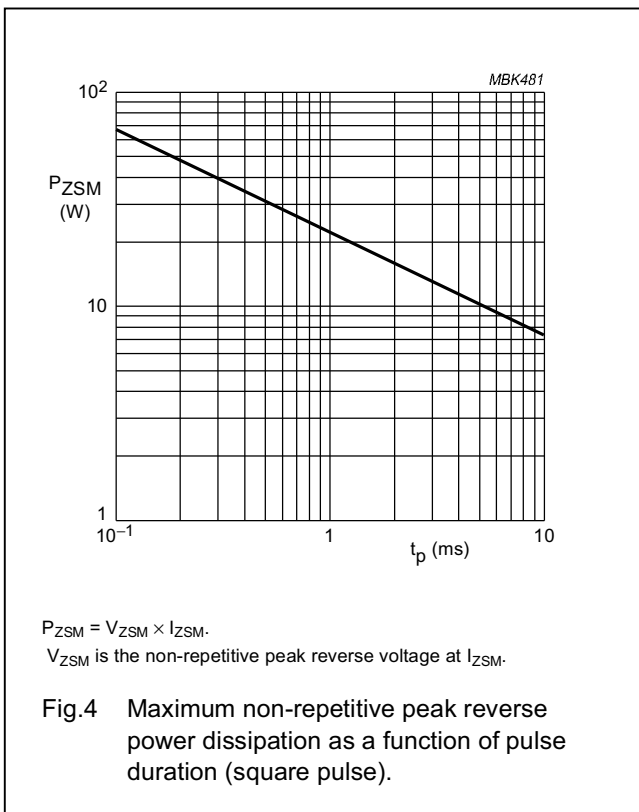
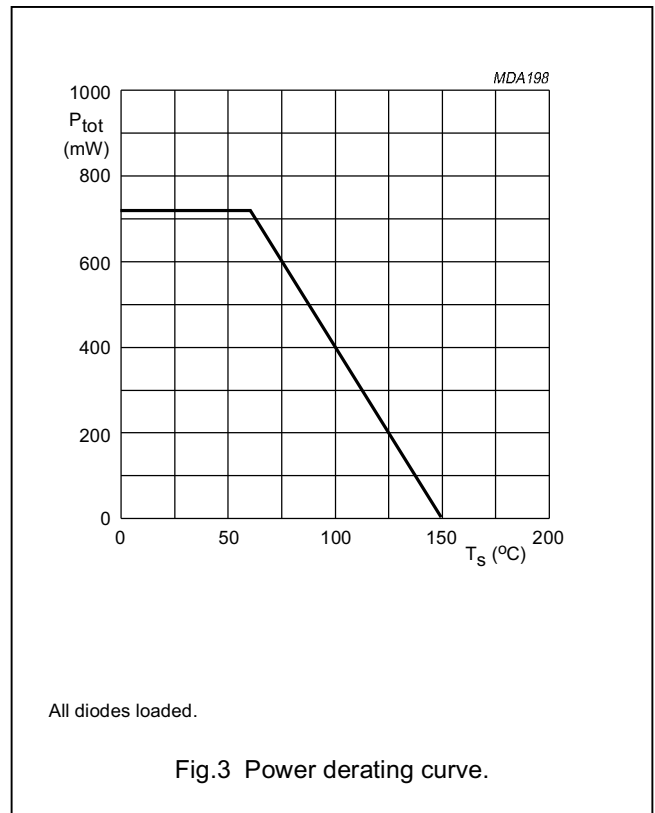
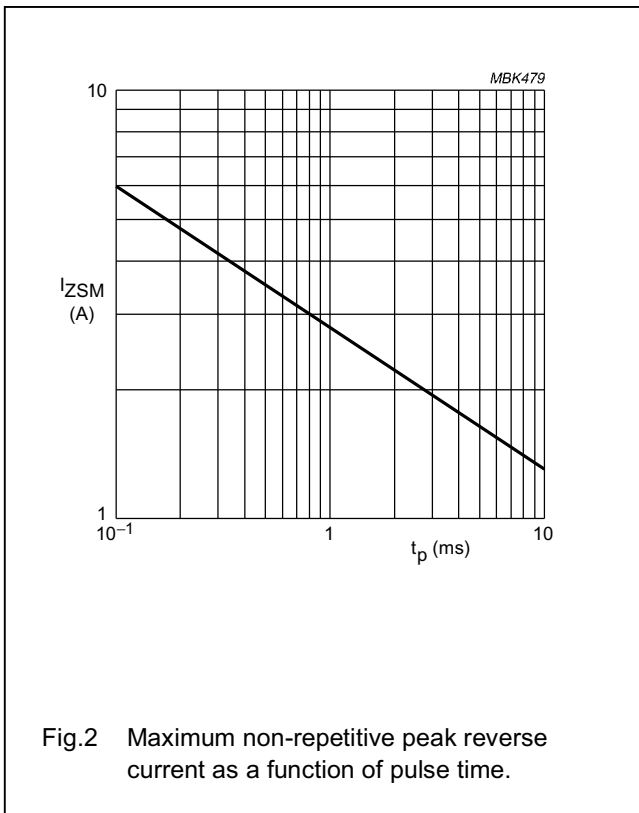
## ELECTRICAL CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per diode</b>						
$V_Z$	working voltage	$I_Z = 1\text{ mA}$	5.89	6.2	6.51	V
$V_F$	forward voltage	$I_F = 200\text{ mA}$	–	–	1.3	V
$V_{ZSM}$	non-repetitive peak reverse voltage	$I_{ZSM} = 3.5\text{ A}; t_p = 1\text{ ms}$	–	–	9	V
$I_R$	reverse current	$V_R = 4\text{ V}$	–	–	700	nA
$r_{dif}$	differential resistance	$I_Z = 1\text{ mA}$	–	–	300	$\Omega$
$S_Z$	temperature coefficient of working voltage	$I_Z = 5\text{ mA}$	–	1.2	–	mV/K
$C_d$	diode capacitance	see Fig.5				
		$V_R = 0; f = 1\text{ MHz}$	–	–	200	pF
		$V_R = 4\text{ V}; f = 1\text{ MHz}$	–	–	110	pF

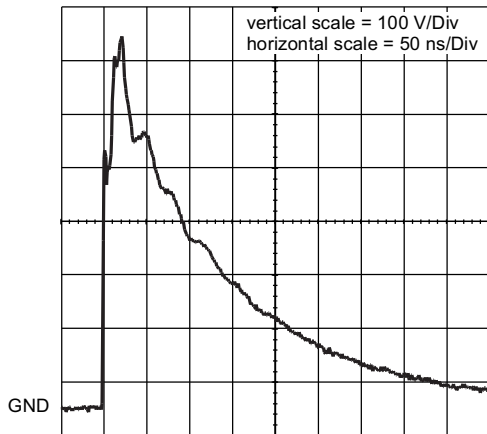
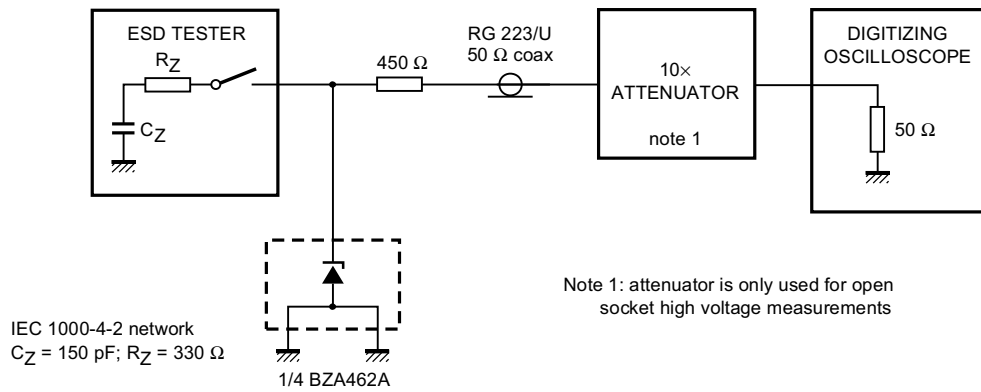
Quadruple ESD transient voltage suppressor

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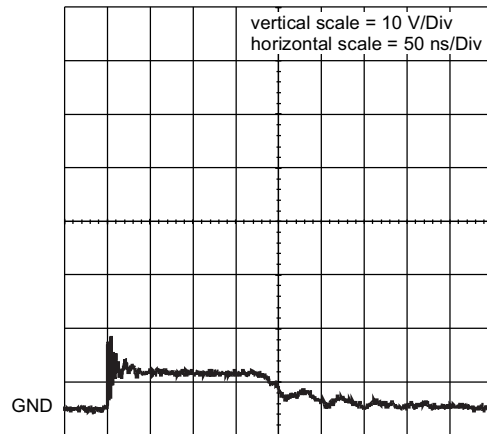


Quadruple ESD transient voltage suppressor

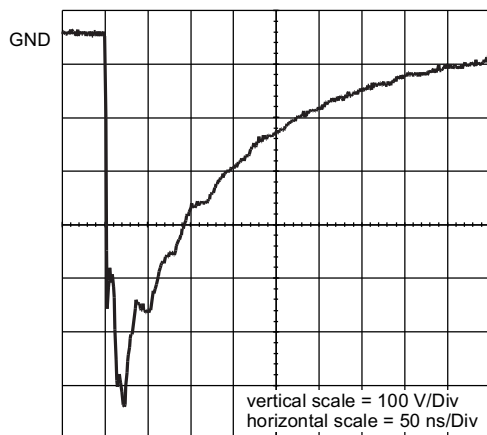
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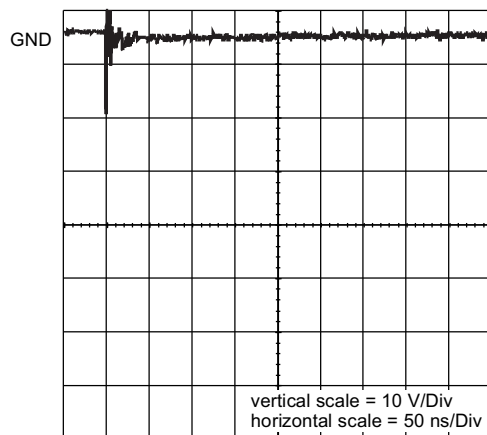
unclamped +1 kV ESD voltage waveform (IEC 1000-4-2 network)



clamped +1 kV ESD voltage waveform (IEC 1000-4-2 network)



unclamped -1 kV ESD voltage waveform (IEC 1000-4-2 network)



clamped -1 kV ESD voltage waveform (IEC 1000-4-2 network)

MBK478

Fig.6 ESD clamping test set-up and waveforms.

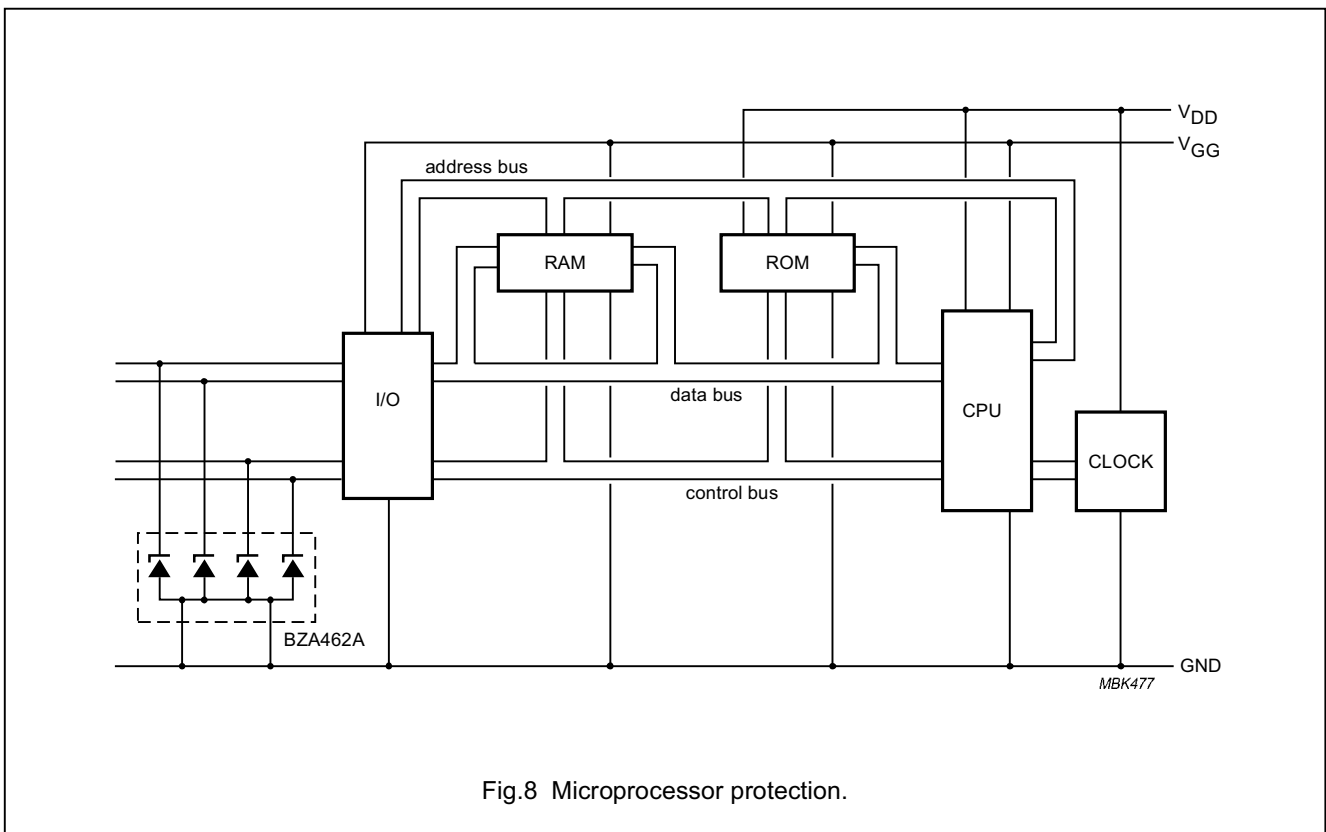
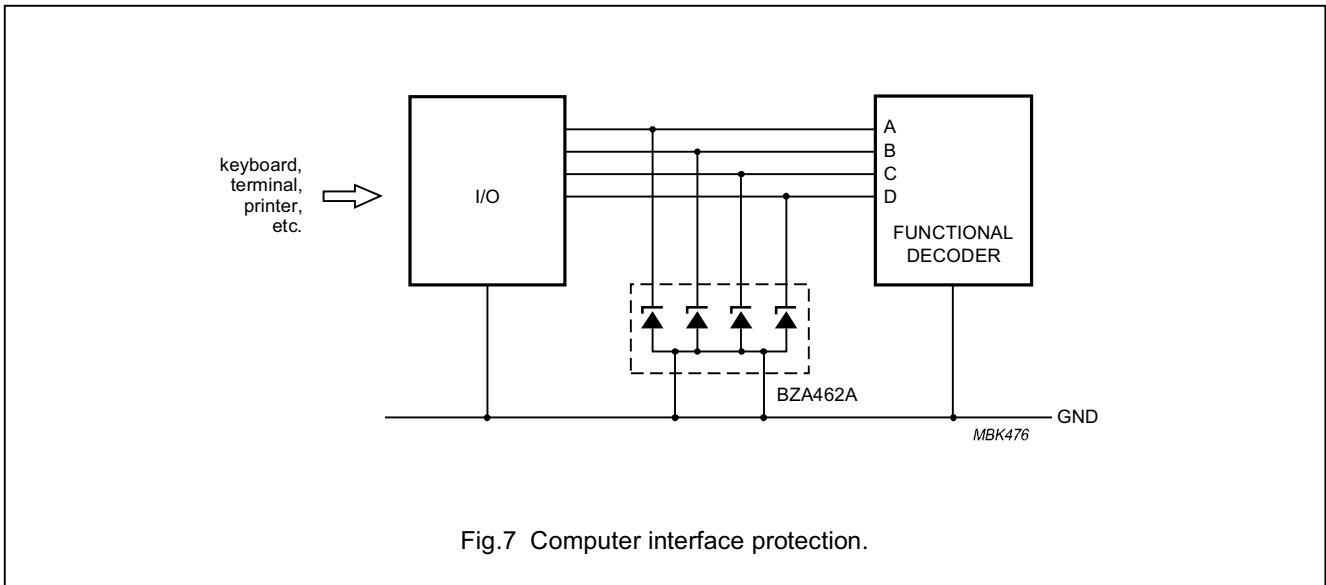
# Quadruple ESD transient voltage suppressor

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## APPLICATION INFORMATION

### Typical common anode application

A quadruple transient suppressor in a SOT457 package makes it possible to protect four separate lines using only one package. Two simplified examples are shown in Figs 7 and 8.



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## Quadruple ESD transient voltage suppressor

## BZA462A

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### Device placement and printed-circuit board layout

Circuit board layout is of extreme importance in the suppression of transients. The clamping voltage of the BZA462A is determined by the peak transient current and the rate of rise of that current ( $di/dt$ ). Since parasitic inductances can further add to the clamping voltage ( $V = L di/dt$ ) the series conductor lengths on the printed-circuit board should be kept to a minimum. This includes the lead length of the suppression element.

In addition to minimizing conductor length the following printed-circuit board layout guidelines are recommended:

1. Place the suppression element close to the input terminals or connectors.
2. Keep parallel signal paths to a minimum.
3. Avoid running protection conductors in parallel with unprotected conductors.
4. Minimize all printed-circuit board loop areas including power and ground loops.
5. Minimize the length of the transient return path to ground.
6. Avoid using shared transient return paths to a common ground point.

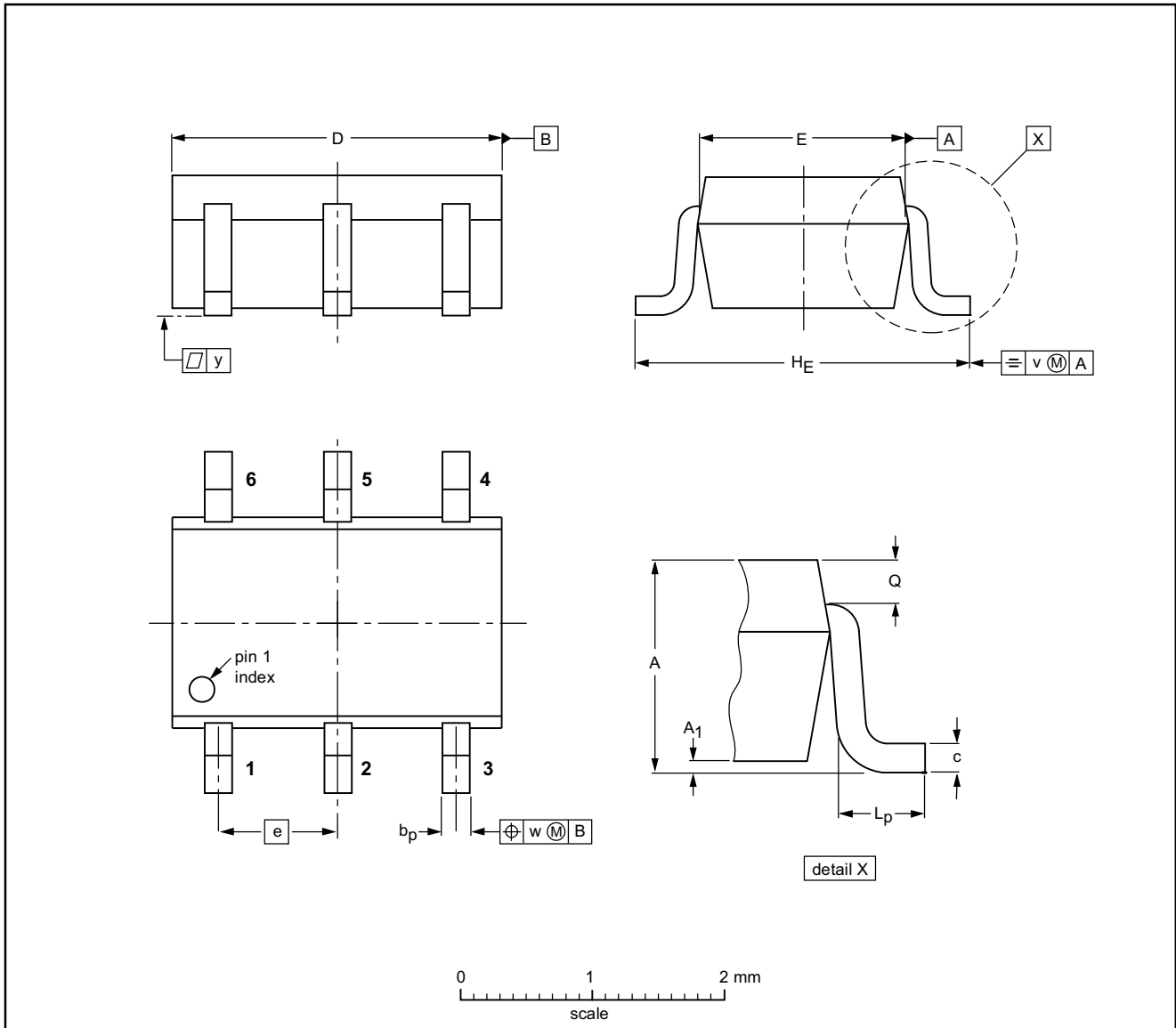
# Quadruple ESD transient voltage suppressor

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## PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT457



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	c	D	E	e	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			97-02-28



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**Quadruple ESD transient voltage suppressor**
**BZA462A****DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
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**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
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**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
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**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
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**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
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**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
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**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
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**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
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Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
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**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
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**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
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**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
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**Philippines:** Philips Semiconductors Philippines Inc.,  
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