N-channel depletion mode vertical D-MOS transistor

BSP124

FEATURES

- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel depletion mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
I_D	DC drain current		–	250	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	−1.65	−0.75	V

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

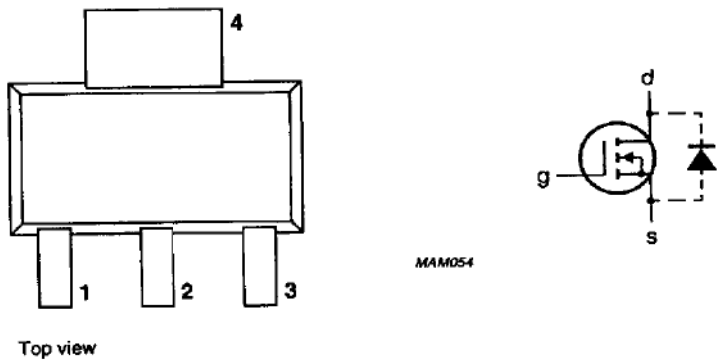

Fig.1 Simplified outline and symbol.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 mm².

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = –3 V	250	–	V
I_{DSX}	drain-source cut-off leakage current	V_{DS} = 200 V; V_{GS} = –3 V	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	100	nA
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	–1.65	–0.75	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = 3 V	–1.4	–0.6	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
		I_D = 250 mA; V_{GS} = 5 V	–	12	Ω
I_{DSS}	drain current	V_{DS} = 25 V; V_{GS} = 0	70	–	mA
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	15	pF
Switching times (see Figs 2 and 3)					
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = –3 to +5 V	–	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = +5 to –3 V	–	30	ns

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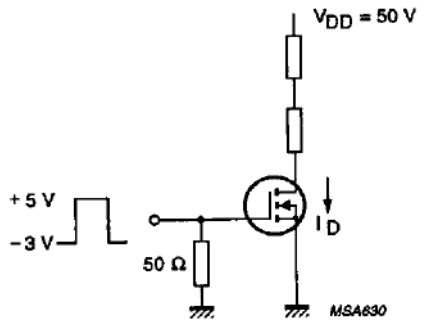


Fig.2 Switching times test circuit.

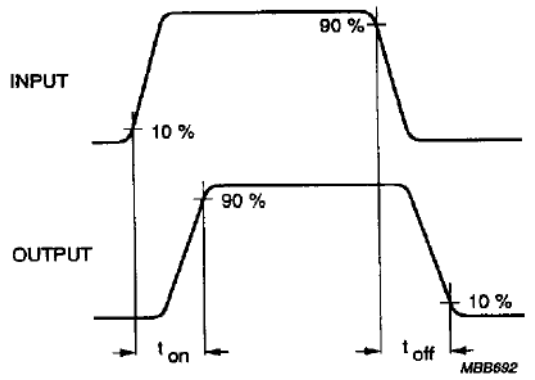


Fig.3 Input and output waveforms.

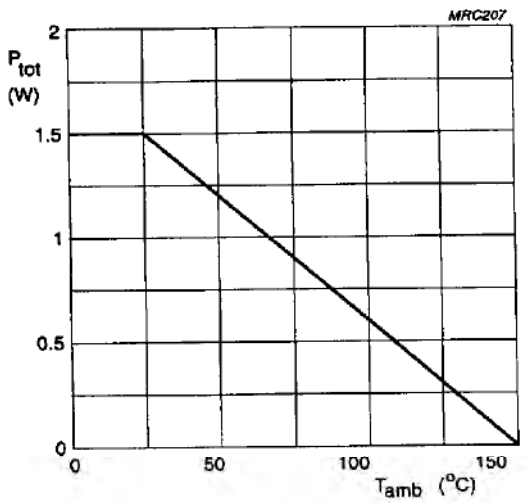
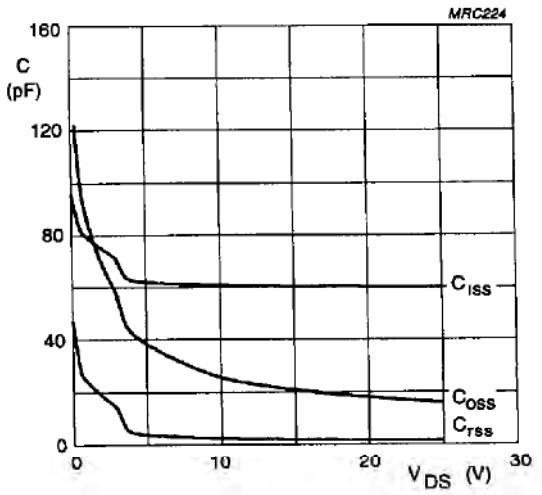


Fig.4 Power derating curve.



V_{GS} = −3 V; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.

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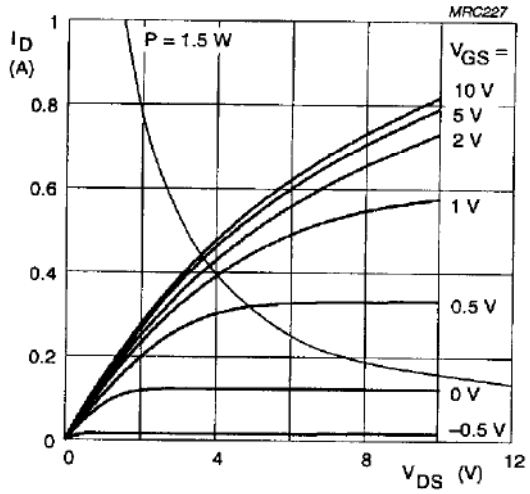
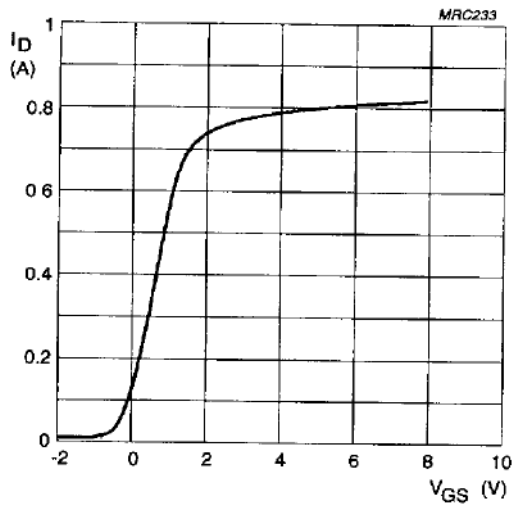


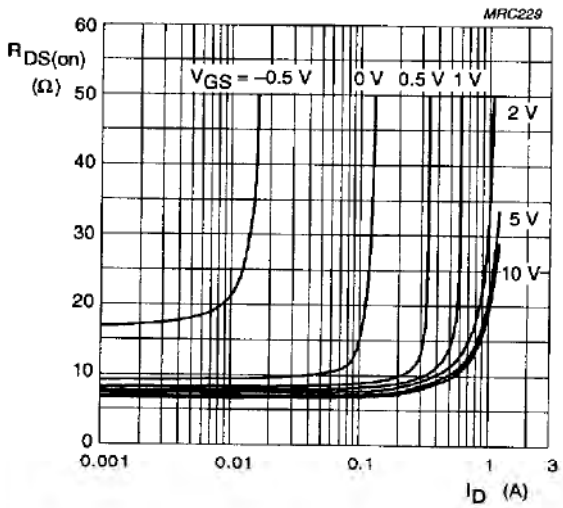
T_j = 25 °C.

Fig.6 Typical output characteristics.



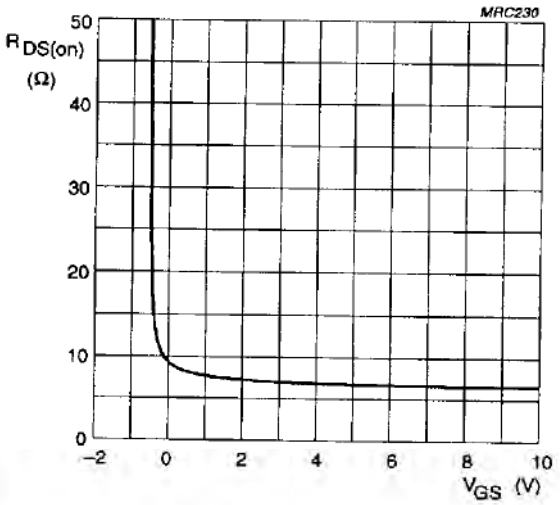
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



I_D = 10 mA; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

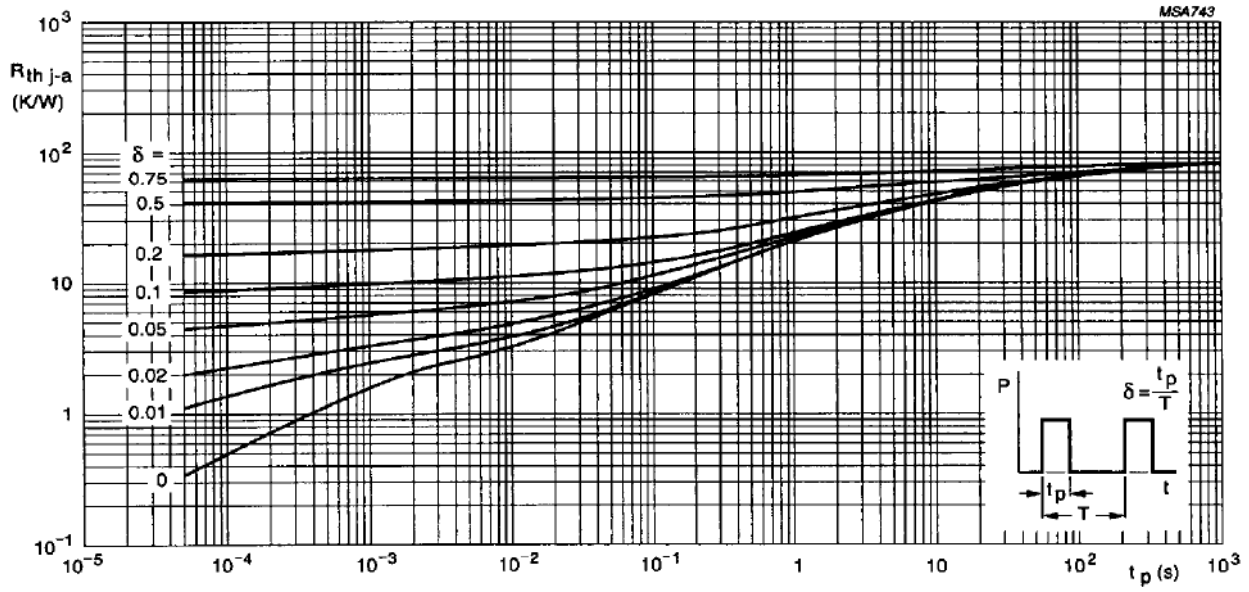
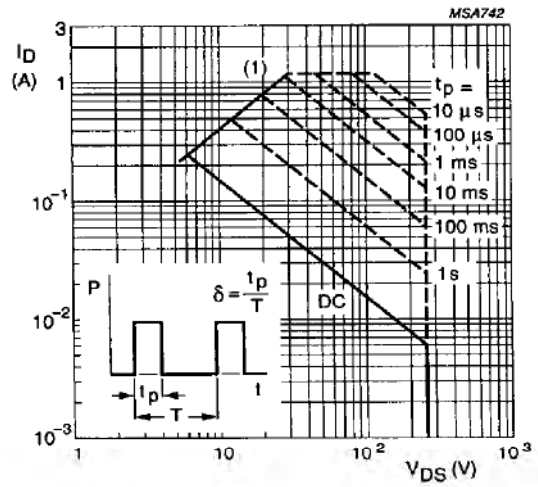


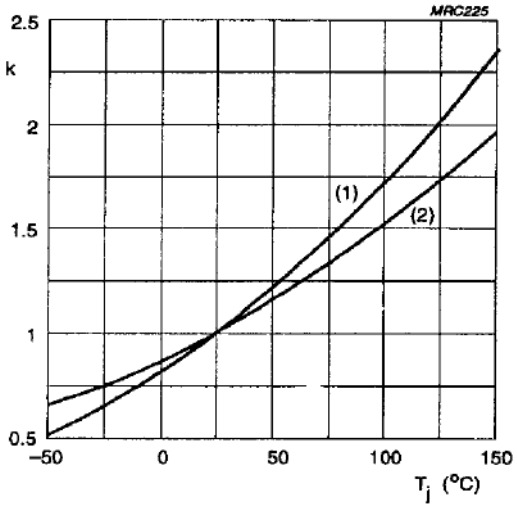
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



δ = 0.01; T_{amb} = 25 °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



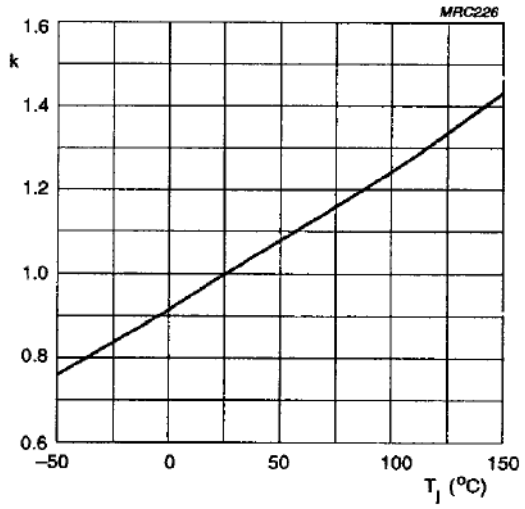
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$;

(1) I_D = 250 mA; V_{GS} = 5 V.

(2) I_D = 20 mA; V_{GS} = 0.

Fig. 12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Typical $V_{GS(th)}$ at I_D = 1 mA; V_{DS} = 3 V.

Fig. 13 Temperature coefficient of gate-source threshold voltage.