Preliminary Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt468

200 MHz Monolithic CMOS 256 x 24 Color Palette RAMDAC™

Distinguishing Features

- 200, 170 MHz Operation
- 8:1 Multiplexed Pixel Ports
- 256 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- Pixel Panning Support
- On-Chip User-Definable Cursor
- RS-343A Compatible Outputs
- Programmable Setup (0 or 7.5 IRE)
- X Windows Support for Cursor
- Standard MPU Interface
- 145-pin PGA Package
- +5 V CMOS Monolithic Construction

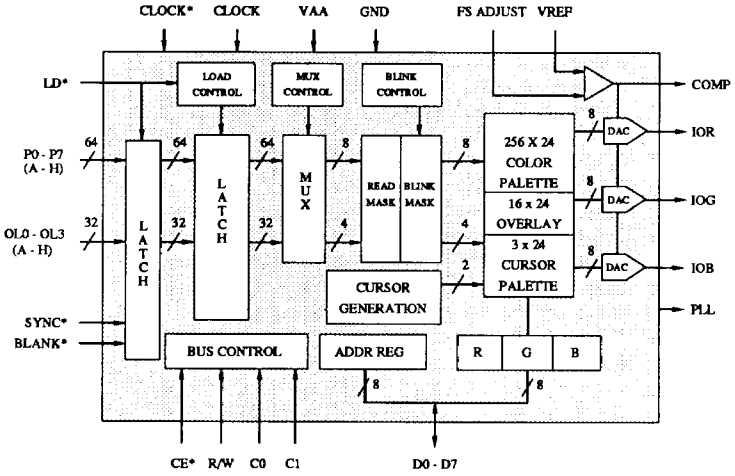
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439

Functional Block Diagram



Product Description

The Bt468 triple 8-bit RAMDAC is designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enables TTL-compatible interfacing to the frame buffer, while maintaining the 200 MHz video data rates required for sophisticated color graphics.

On-chip features include a 256 x 24 color palette RAM, 16 x 24 overlay color palette RAM, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), and pixel panning support.

The Bt468 has an on-chip three-color 64 x 64 pixel cursor and a three-color full screen (or full window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with sub-pixel resolution.

The Bt468 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly terminated 50 Ω or 75 Ω coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt468 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

When accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU. ADDR12–ADDR15 are always a logical zero. ADDR0 and ADDR8 correspond to D0.

ADDR0–15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–15)
$0000–$00FF	10	reserved
$0100	10	overlay color 0*
:	10	:
$010F	10	overlay color 15*
$0181	10	cursor color register 1*
:	:	cursor color register 2*
$0183	10	cursor color register 3*
$0200	10	ID register ($4F)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0204	10	pixel read mask register
$0205	10	reserved ($00)
$0206	10	pixel blink mask register
$0207	10	reserved ($00)
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	reserved ($00)
$020B	10	test register
$020C	10	red output signature register
$020D	10	green output signature register
$020E	10	blue output signature register
$0220	10	revision register
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400–$07FF	10	cursor RAM
$0000–$00FF	11	color palette RAM*

*Indicates requires three read/write cycles—RGB.

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Additional Information

Although the color palette RAM, overlay RAM, and cursor color registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers and cursor RAM is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and cursor RAM, the address register increments following a read or write cycle.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt468.

Single-Channel RAMDAC Operation

The Bt468 may be configured (via command register_2) to be a single-channel RAMDAC, enabling three Bt468s to be used in parallel for a 24-bit true-color system. The Bt468s share a common 8-bit data bus (D0–D7).

Each Bt468 must be configured to be either a red, green, or blue RAMDAC via command register_2. Only the green channel (IOG) of each RAMDAC is used; the IOR and IOB outputs should be connected to GND, either directly or through a resistor up to 75 Ω.

To load the color palettes, the MPU performs the normal (red, green, blue) write cycles to all three RAMDACs simultaneously. The red Bt468 loads color data only during the the red write cycle, the green Bt468 loads color data only during the green write cycle, and the blue Bt468 loads color data only during the blue write cycle.

To read the color palettes, the MPU performs the normal (red, green, blue) read cycles from all three RAMDACs simultaneously. The red Bt468 outputs color data only during the the red read cycle, the green Bt468 outputs color data only during the green read cycle, and the blue Bt468 outputs color data only during the blue read cycle.

External circuitry must decode when the MPU is reading or writing to the color palettes and assert CE* to all three Bt468s simultaneously.

4

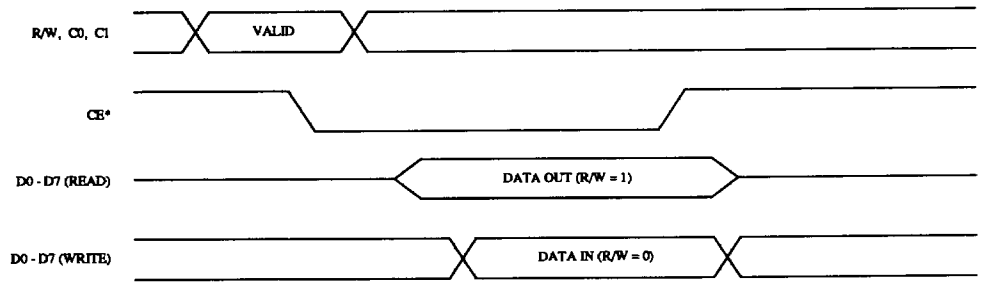

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt468 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for eight consecutive pixels are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with eight pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

Typically, the Bt468 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, etc., until all eight pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase-shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by eight, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than six, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

Only one rising edge of LD* should occur every eight clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

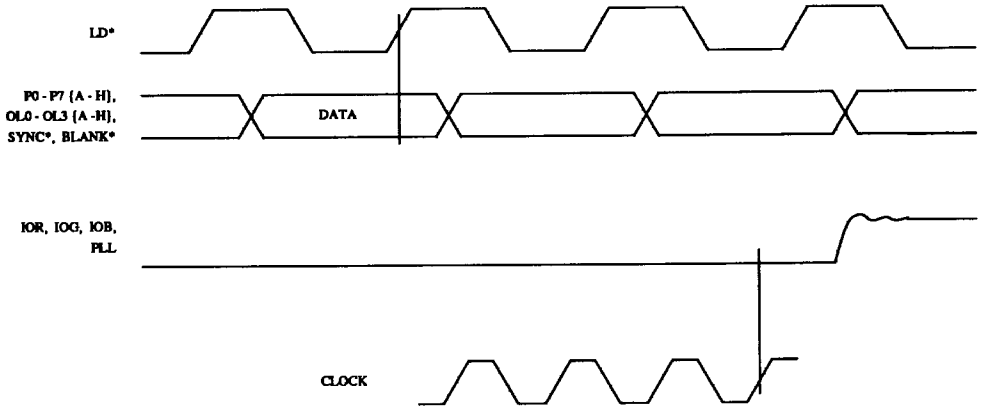

Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Read and Blink Masking

Each clock cycle, 8 bits of color information (P0–P7) and 4 bits of overlay information (OL0–OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt468 monitors the SYNC* and BLANK* input to determine vertical retrace intervals (any BLANK* pulse longer than 256 LD* cycles).

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 2 illustrates the truth table used for color selection.

Pixel Panning

To support pixel panning, command register_1 specifies by how many clock cycles to pan.

If 0-pixel panning is specified, pixel {A} is output first, followed by pixel {B}, etc., until all eight pixels have been output, at which point the cycle repeats.

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval, and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B} through {H} will be output during the blanking interval, and will not be seen on the display screen.

The process is similar for panning by two to seven pixels.

Note that when a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt468 during the first LD* cycle that BLANK* is a logical zero.

The P0–P7 and OL0–OL3 inputs are all panned. Cursor position is also panned. If the user desires to keep the cursor position the same relative to the edge of the display, the X register of the cursor position should be updated at the same time the pixel panning register is updated.

Panning is done by delaying the SYNC* and BLANK* signals an additional one to seven clock cycles.

Circuit Description (continued)

On-Chip Cursor Operation

The Bt468 has an on-chip, three-color, 64 x 64 pixel, user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. Cursor positioning is done via the cursor (x,y) register. Note that the Bt468 expects (x) to increase going right, and (y) to increase going down, as seen on the display screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the first falling edge of SYNC* that is after a vertical sync has been detected. Vertical sync is detected as the second falling edge during blank.

The resetting of the Bt468 to an eight-cycle pipeline delay is required for proper cursor pixel alignment.

Three Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides 2 bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

(0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each "plane" of cursor information may also be independently enabled or disabled for display via the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM. Either the cursor color registers, color palette RAM, or overlay RAM provides 24 bits of color information during the appropriate clock cycle, depending on the cursor pattern values.

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the 31st column of the 64 x 64 array (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the 31st row of the 64 x 64 array (assuming the rows start with 0 for the top-most pixel and increment to 63). (See Figure 3.)

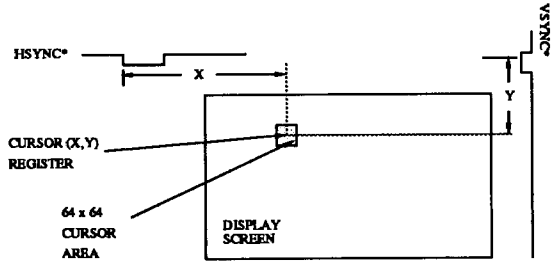

Figure 3. Cursor Positioning.

Circuit Description (continued)

Cross Hair Cursor

Cursor positioning for the three-color cross hair cursor is also done through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than one pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) is used to specify the color of the cross hair cursor.

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is limited to being displayed within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, **it is the responsibility of the software to ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.**

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000 and the window width and height registers should contain $0FFF. (See Figure 4.)

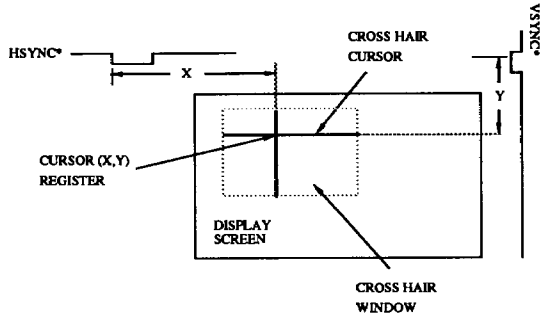

Figure 4. Cross Hair Cursor Positioning.

Circuit Description (continued)

Dual Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors. Both cursor planes utilize the same cursor (x,y) registers.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical direction, it will be one pixel off from being truly centered about the cross hair cursor.

Figure 5 illustrates displaying the dual cursors.

In the 64 x 64 pixel area in which the user-definable cursor would be displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair cursor information. Thus, the color of the displayed cursor will be dependent on the cursor pattern, whether they are logically ORed or XORed, and the individual cursor display enable and blink enable bits.

Figure 6 shows the equivalent cursor generation circuitry.

The resetting of the Bt468 to an eight cycle pipeline delay is required for proper cursor pixel alignment.

X Windows Cursor Mode

In the X Windows mode, plane1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3. The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Refer to Figure 9 as to the organization of the cursor RAM while in the X Windows mode.

Note that if the cursor is configured for X Windows mode, the cross hair cursor will not be displayed.

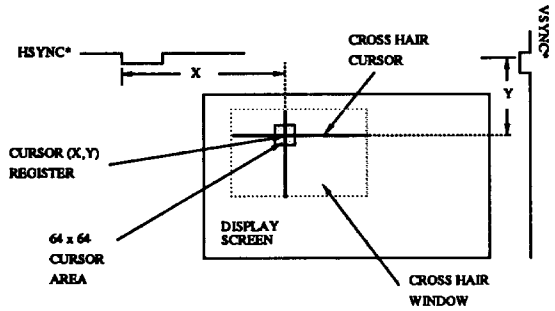

Figure 5. Dual Cursor Positioning.

Circuit Description (continued)

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 7 and 8. Command register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The Bt468 can drive either doubly terminated 50 Ω or 75 Ω coax directly. If a 50 Ω double termination is used, then a typical RSET value is 348 Ω for a 7.5 IRE blanking pedestal or 332 Ω for a 0 IRE blanking pedestal. For a 75 Ω double termination, a typical RSET is 523 Ω for a 7.5 IRE blanking pedestal and 495 Ω for a 0 IRE blanking pedestal.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 3 and 4 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt468 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

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Cursor1, Cursor0	CR05	OL0–OL3	P0–P7	Addressed by frame buffer
11	x	$x	$xx	cursor color 3
10	x	$x	$xx	cursor color 2
01	x	$x	$xx	cursor color 1
00	x	$F	$xx	overlay color 15
:	:	:	:	:
00	x	$1	$xx	overlay color 1
00	1	$0	$xx	overlay color 0
00	0	$0	$00	RAM location $00
00	0	$0	$01	RAM location $01
:	:	:	:	:
00	0	$0	$FF	RAM location $FF

Note: Refer to Figure 6 for generation of Cursor1 and Cursor0 control bits.

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

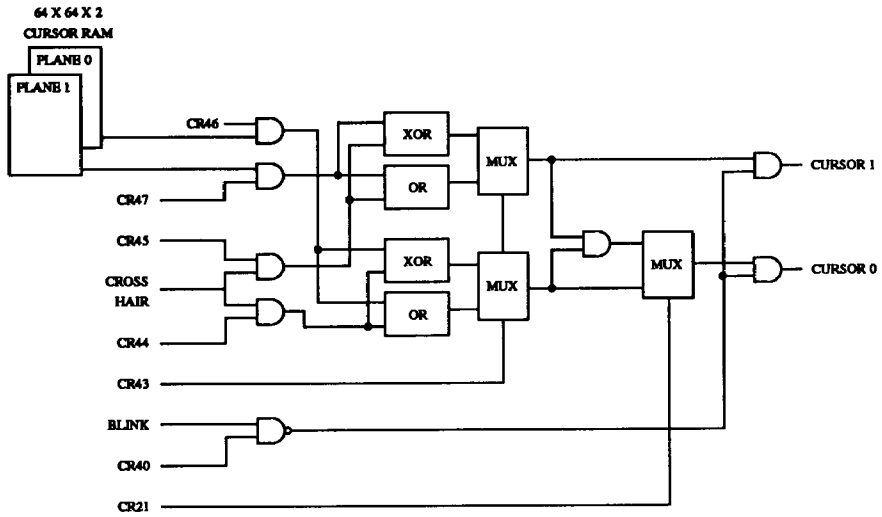
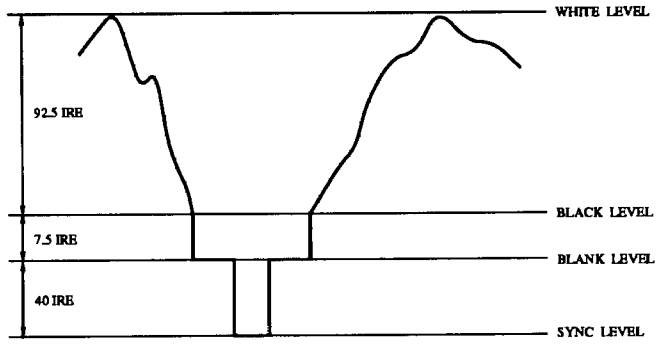


Figure 6. Cursor Control Circuitry.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
28.56	0.714	40.00	1.000
2.16	0.054	13.6	0.340
0.00	0.000	11.44	0.286
		0.00	0.000



Note: 50 Ω doubly terminated load, RSET = 348 Ω, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 7. Composite Video Output Waveform (SETUP = 7.5 IRE).

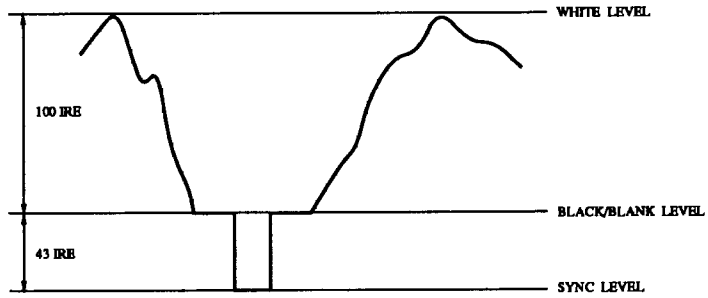
Description	IOG (mA)	IOR, IOB (mA)	CSYNC*	BLANK*	DAC Input Data
WHITE	40	28.56	1	1	$FF
DATA	data + 13.6	data + 2.16	1	1	data
DATA - SYNC	data + 2.16	data + 2.16	0	1	data
BLACK	13.6	2.16	1	1	$00
BLACK - SYNC	2.16	2.16	0	1	$00
BLANK	11.44	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 40 mA. RSET = 348 Ω, VREF = 1.235 V.

Table 3. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
27.90	0.698	40.00	1.000
0.00	0.000	12.08	0.302
		0.00	0.000



Note: 50 Ω doubly terminated load, RSET = 332 Ω, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 8. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOG (mA)	IOR, IOB (mA)	CSYNC*	BLANK*	DAC Input Data
WHITE	40	27.9	1	1	$FF
DATA	data + 12.1	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	12.1	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	12.1	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 40 mA. RSET = 332 Ω, VREF = 1.235 V.

Table 4. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07 reserved (logical one)

CR06 reserved (logical zero)

CR05 Overlay 0 enable

(0) use color palette RAM
(1) use overlay color 0

When in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0. See Table 2.

CR04 reserved (logical zero)

CR03, CR02 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).

CR01, CR00 reserved (logical zero)

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17–CR15 Pan select

(000) 0 pixels {pixel A}
(001) 1 pixel {pixel B}
(010) 2 pixels {pixel C}
(011) 3 pixels {pixel D}
(100) 4 pixels {pixel E}
(101) 5 pixels {pixel F}
(110) 6 pixels {pixel G}
(111) 7 pixels {pixel H}

These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, etc.

CR14–CR10 reserved (logical zero)

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync Enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto the IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt468 using three write cycles (red, green, and blue), and color data is output using three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt468 to emulate a single-channel RAMDAC using only the green channel (IOG).
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* for generating PLL information.
CR22	reserved (logical zero)	
CR21	X Windows cursor select (0) normal cursor (1) X Windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X Windows compatible mode (logical one).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt468, the value read by the MPU will be $4F. Data written to this register is ignored.

Pixel Read Mask Register

The 8-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0.

Pixel Blink Mask Register

The 8-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–H}) and D3 corresponds to overlay plane 3 (OL3 {A–H}). Bits D0–D3 are logically ANDed with the corresponding overlay plane input. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–H}) and D3 corresponds to overlay plane 3 (OL3 {A–H}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Revision Register (Revision B only)

This 8-bit is a read-only register, specifying the revision of the Bt468. The four most significant bits signify the revision letter B, in hexidecimal form. The four least significant bits do not represent any value and should be ignored. Data written to this register is ignored.

Since Revision A device does not have a revision register, address $0220 will contain the last data read to or written from the internal bus.

Internal Registers (continued)

Red, Green, and Blue Output Signature Registers

Signature Operation

These three 8-bit signature registers (one each for red, green, and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. Refer to the Application Information test register section for more information.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–E) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Internal Registers (continued)

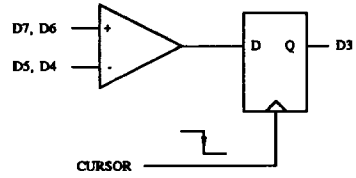
Test Register

This 8-bit register is used for testing the Bt468. D0–D2 are used to specify which pixel input to use, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	pixel F
110	pixel G
111	pixel H

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result



D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The table above lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3–D7 must be a logical zero.

Internal Registers (continued)

Cursor Command Register

This command register is used to control various cursor functions of the Bt468. It is not initialized, and may be written to or read by the MPU at any time. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	Cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	Cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Note that plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is one, three, five, or seven pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	This bit specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register_0.

Internal Registers (continued)

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window, or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized and may be written to or read by the MPU at any time. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H–72

where H = number of pixels between the first rising edge of CLOCK following the falling edge of SYNC* to active video.

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where V = number of scan lines from the first falling edge of SYNC* that is two or more clock cycles after vertical sync to active video.

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

Internal Registers (continued)

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized and may be written to or read by the MPU at any time. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H–40

where H = number of pixels between the first rising edge of CLOCK following the falling edge of SYNC* to active video.

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where V = number of scan lines from the first falling edge of SYNC* that is two or more clock cycles after vertical sync to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair is implemented by loading the window (x,y) registers with $0000 and the window width and height registers with $0FFF.

Internal Registers (continued)

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized and may be written to or read by the MPU at any time. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4–D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 16 pixels more than the value specified by the window width register. The actual window height is 16 pixels more than the value specified by the window height register. Therefore, the minimum window width is 16 pixels, and the minimum window height is 16 pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

Internal Registers (continued)

Cursor RAM

This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window, and is not initialized. The cursor RAM should not be written to by the MPU during the horizontal sync time and for the two LD* cycles after the end of the horizontal sync. The cursor RAM may otherwise be written to or read by the MPU at any time without contention.

If writing to the cursor RAM asynchronously to horizontal sync, it is recommended that the cursor be positioned off-screen in the Y direction (write to the cursor (y) registers and wait for the vertical sync interval to move the cursor off-screen), write to the cursor RAM, then reposition the cursor back to the original position. An alternative is to perform a write then read sequence, and if the correct cursor RAM data was not written, perform another write then read sequence. Since the contention occurs only during horizontal sync at the Y locations coincident with the cursor, the second write/read sequence bypasses the window of time when cursor RAM is in contention.

During MPU accesses to the cursor RAM, the address register is used to address the cursor RAM. Figure 9 illustrates the internal format of the cursor RAM, as it appears on the display screen. Addressing starts at location $400 as shown in Table 1.

Note that in the X Windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

Note: in both modes of operation, plane1 = D7, D5, D3, D1; plane0 = D6, D4, D2, D0.

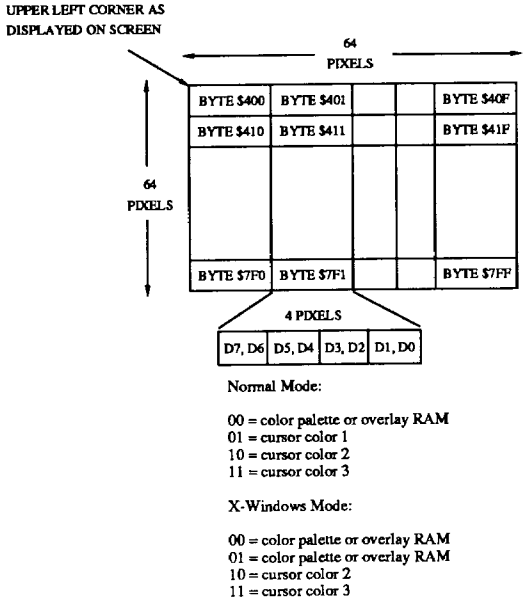


Figure 9. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 3 and 4. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 7 and 8). SYNC* does not override any other control or data input, as shown in Tables 3 and 4; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P7 {A–H}, OL0–OL3 {A–H}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is 1/8 of CLOCK, may be phase-independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.
P0–P7 {A–H}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 2). Eight consecutive pixels (8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all eight pixels have been output, at which point the cycle repeats.
OL0–OL3 {A–H}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and, in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as illustrated in Table 2. When accessing the overlay palette RAM, the P0–P7 {A–H} inputs are ignored. Overlay information (up to four bits per pixel) for eight consecutive pixels are input through this port. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 50 Ω coaxial cable (Figure 10). All outputs, whether used or not, should have the same output load.
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt468s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 10). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. Refer to PC Board Layout Considerations for critical layout criteria.

Pin Descriptions (continued)

Pin Name	Description
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 10). Note that the IRE relationships in Figures 7 and 8 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = K1 * VREF (V) / IOG (mA) The full scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω) where K1 and K2 are defined as:

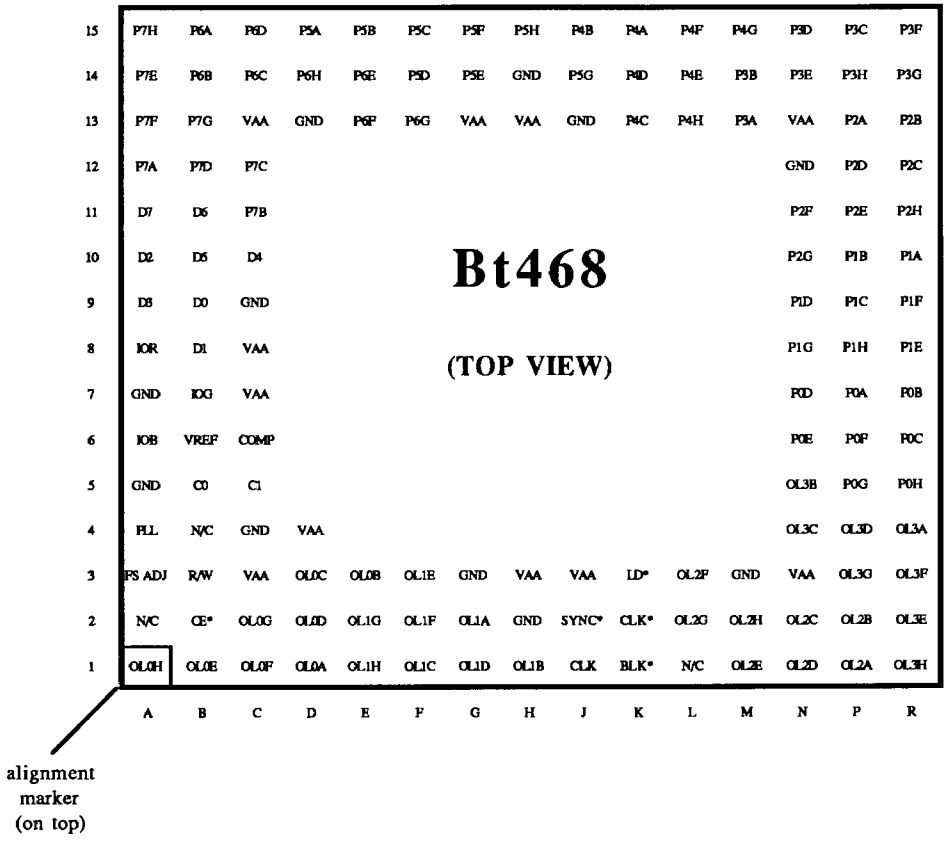
Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 10, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 10. IF VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)

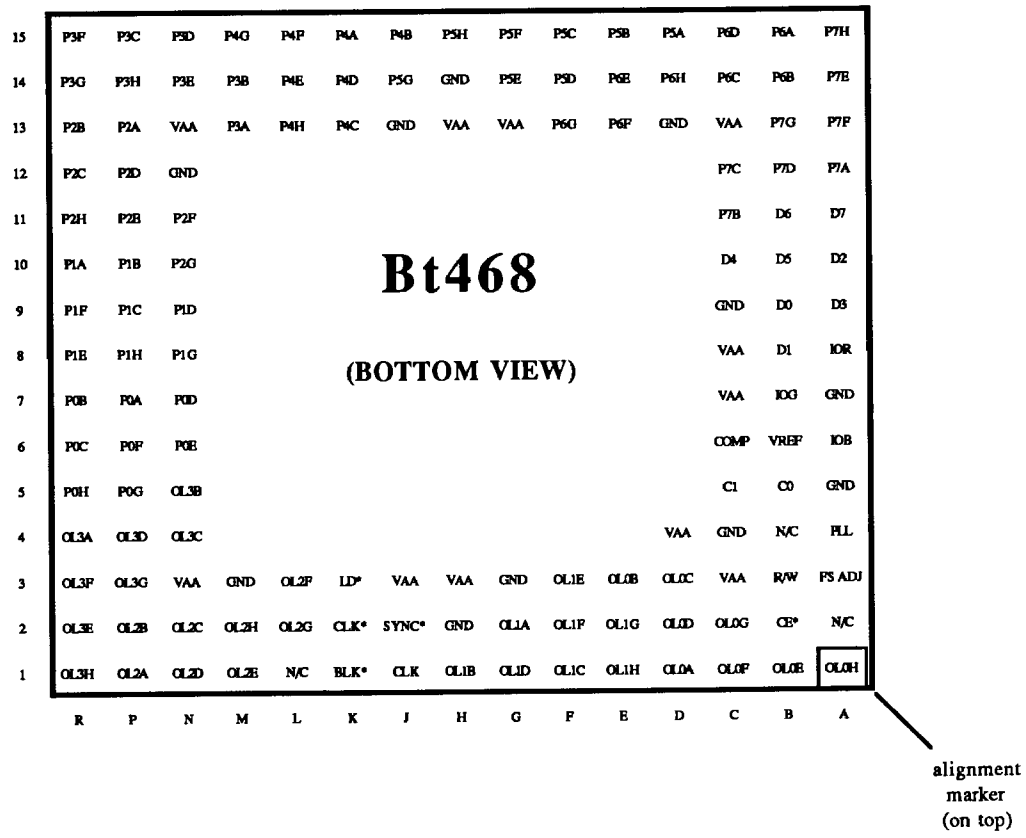
Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	K1	P5A	D15	OL2A	P1
SYNC*	J2	P5B	E15	OL2B	P2
LD*	K3	P5C	F15	OL2C	N2
CLOCK	J1	P5D	F14	OL2D	N1
CLOCK*	K2	P5E	G14	OL2E	M1
		P5F	G15	OL2F	L3
P0A	P7	P5G	J14	OL2G	L2
P0B	R7	P5H	H15	OL2H	M2
P0C	R6				
P0D	N7	P6A	B15	OL3A	R4
P0E	N6	P6B	B14	OL3B	N5
P0F	P6	P6C	C14	OL3C	N4
P0G	P5	P6D	C15	OL3D	P4
P0H	R5	P6E	E14	OL3E	R2
		P6F	E13	OL3F	R3
P1A	R10	P6G	F13	OL3G	P3
P1B	P10	P6H	D14	OL3H	R1
P1C	P9				
P1D	N9	P7A	A12	D0	B9
P1E	R8	P7B	C11	D1	B8
P1F	R9	P7C	C12	D2	A10
P1G	N8	P7D	B12	D3	A9
P1H	P8	P7E	A14	D4	C10
		P7F	A13	D5	B10
P2A	P13	P7G	B13	D6	B11
P2B	R13	P7H	A15	D7	A11
P2C	R12				
P2D	P12	OL0A	D1	VAA	C3
P2E	P11	OL0B	E3	VAA	C7
P2F	N11	OL0C	D3	VAA	C8
P2G	N10	OL0D	D2	VAA	C13
P2H	R11	OL0E	B1	VAA	D4
		OL0F	C1	VAA	G13
P3A	M13	OL0G	C2	VAA	H3
P3B	M14	OL0H	A1	VAA	H13
P3C	P15			VAA	J3
P3D	N15	OL1A	G2	VAA	N3
P3E	N14	OL1B	H1	VAA	N13
P3F	R15	OL1C	F1		
P3G	R14	OL1D	G1	GND	A5
P3H	P14	OL1E	F3	GND	A7
		OL1F	F2	GND	C4
P4A	K15	OL1G	E2	GND	C9
P4B	J15	OL1H	E1	GND	D13
P4C	K13			GND	G3
P4D	K14	IOR	A8	GND	H2
P4E	L14	IOG	B7	GND	H14
P4F	L15	IOB	A6	GND	J13
P4G	M15	PLL	A4	GND	M3
P4H	L13			GND	N12
		CE*	B2		
COMP	C6	R/W	B3	reserved	A2
FS ADJUST	A3	C0	B5	reserved	B4
VREF	B6	C1	C5	reserved	L1

Pin Descriptions (continued)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
15	P7H	P6A	P6D	P5A	P5B	P5C	P5F	P5H	P4B	P4A	P4F	P4G	P3D	P3C	P3F
14	P7E	P6B	P6C	P6H	P6E	P5D	P5E	GND	P5G	P4D	P4E	P3B	P3E	P3H	P3G
13	P7F	P7G	VAA	GND	P6F	P6G	VAA	VAA	GND	P4C	P4H	P3A	VAA	P2A	P2B
12	P7A	P7D	P7C										GND	P2D	P2C
11	D7	D6	P7B										P2F	P2E	P2H
10	D2	D5	D4										P2G	P1B	P1A
9	D3	D0	GND										P1D	P1C	P1F
8	IOR	D1	VAA										P1G	P1H	P1E
7	GND	IOG	VAA										P0D	P0A	P0B
6	IOB	VREF	COMP										P0E	P0F	P0C
5	GND	C0	C1										OL3B	P0G	P0H
4	PLL	N/C	GND	VAA									OL3C	OL3D	OL3A
3	PS ADJ	R/W	VAA	OL0C	OL0B	OL1E	GND	VAA	VAA	LD*	OL2F	GND	VAA	OL3G	OL3F
2	N/C	CE*	OL0G	OL0D	OL1G	OL1F	OL1A	GND	SYNC*	CLK*	OL2G	OL2H	OL2C	OL2B	OL3E
1	OL0H	OL0E	OL0F	OL0A	OL1H	OL1C	OL1D	OL1B	CLK	BLK*	N/C	OL2E	OL2D	OL2A	OL3H

Pin Descriptions (continued)



	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
15	P3F	P3C	P3D	P4G	P4F	P4A	P4B	P5H	P5F	P5C	P5B	P5A	P6D	P6A	P7H
14	P3G	P3H	P3E	P3B	P4E	P4D	P5G	GND	P5E	P5D	P6E	P6H	P6C	P6B	P7E
13	P2B	P2A	VAA	P3A	P4H	P4C	GND	VAA	VAA	P6G	P6F	GND	VAA	P7G	P7F
12	P2C	P2D	GND										P7C	P7D	P7A
11	P2H	P2E	P2F										P7B	D6	D7
10	P1A	P1B	P2G										D4	D5	D2
9	P1F	P1C	P1D										GND	D0	D3
8	P1E	P1H	P1G										VAA	D1	IOR
7	P0B	P0A	P0D										VAA	IOG	GND
6	P0C	P0F	P0E										COMP	VREF	IOB
5	P0H	P0G	OL3B										C1	C0	GND
4	OL3A	OL3D	OL3C									VAA	GND	N/C	PLL
3	OL3F	OL3G	VAA	GND	OL2F	LD*	VAA	VAA	GND	OL1E	OL0B	OL0C	VAA	R/W	PS ADJ
2	OL3E	OL2B	OL2C	OL2H	OL2G	CLK*	SYNC*	GND	OL1A	OL1F	OL1G	OL0D	OL0G	CB*	N/C
1	OL3H	OL2A	OL2D	OL2E	N/C	BLK*	CLK	OL1B	OL1D	OL1C	OL1H	OL0A	OL0F	OL0E	OL0H

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt468 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a six-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably the analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt468 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt468.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 10. Another isolated ground plane is used for the GND pins of the Bt468 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt468 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 10. This bead should be located within 3 inches of the Bt468 and provides resistance to switching currents, acting as a low pass filter at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors have minimum inductance and are preferred. Radial lead ceramic capacitors may be substituted for chip capacitors. Axial lead capacitors are not recommended because of self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of the six groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt468 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt468 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt468 to minimize reflections. Unused analog outputs should be connected to GND.

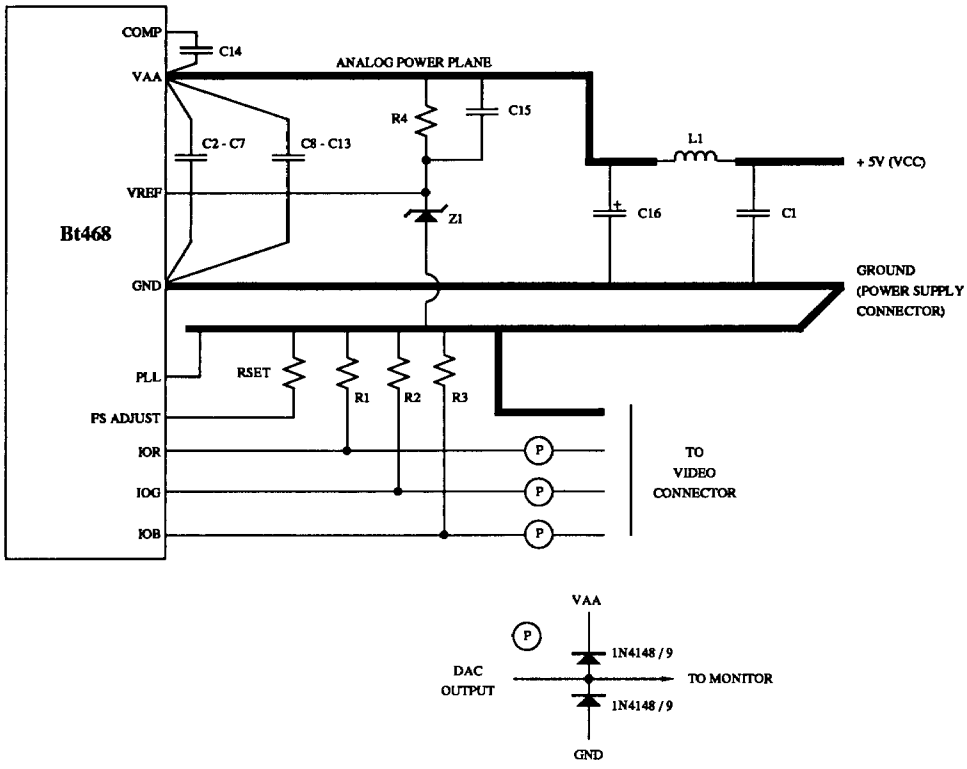
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt468 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 10 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1–C7, C14, C15	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C8–C13	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C16	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	50 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	348 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt468.

Figure 10. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt468 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND). The termination resistors should be as close as possible to the Bt468.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt468 will not function using a single-ended clock with CLOCK* connected to ground.

170 MHz and greater applications require robust ECL clock signals with strong pull-down (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

Typically, LD* is generated by dividing CLOCK by eight and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt468 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt468, and sets the pipeline delay of the Bt468 to eight clock cycles. Figure 11 illustrates using the Bt438 with the Bt468.

When using a single Bt468, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

Using Multiple Bt468s

For display applications where up to four Bt468s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt468, synchronizes them to sub-pixel resolution, and sets the pipeline delay of the Bt468 to eight clock cycles. Figure 12 illustrates using the Bt439 with the Bt468.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt468, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt468s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt468s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

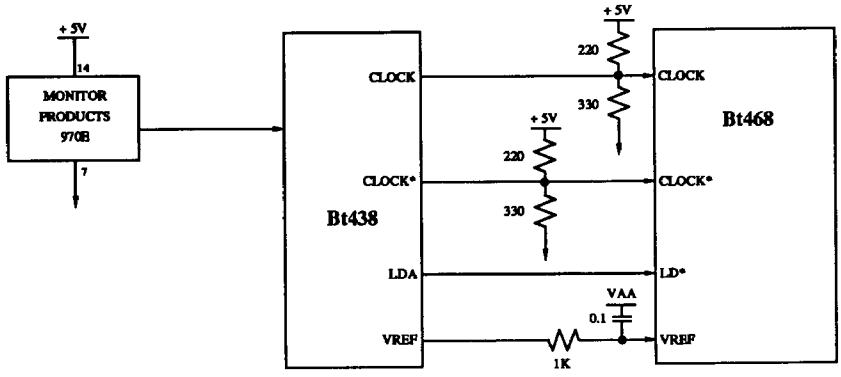


Figure 11. Generating the Bt468 Clock Signals.

Application Information (continued)

If sub-pixel synchronization of multiple Bt468s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt468s are connected together, and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The designer must take care to minimize skew on the CLOCK and CLOCK* lines. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω). When using multiple Bt468s, each Bt468 should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Each Bt468 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Setting the Pipeline Delay

The pipeline delay of the Bt468, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt468 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt468.

To reset the Bt468, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for **at least** three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

In order to assure that the Bt468 has the proper configuration, all of the command registers must be initialized prior to a fixed pipeline reset. Because of this requirement, the power up which occurs prior to initialization of the command registers cannot be used to assure the fixed pipeline. An additional reset is required after command register writes.

The resetting of the Bt468 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt468s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

Resetting the Bt468 to an eight clock cycle pipeline delay is required for proper cursor pixel alignment.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information (continued)

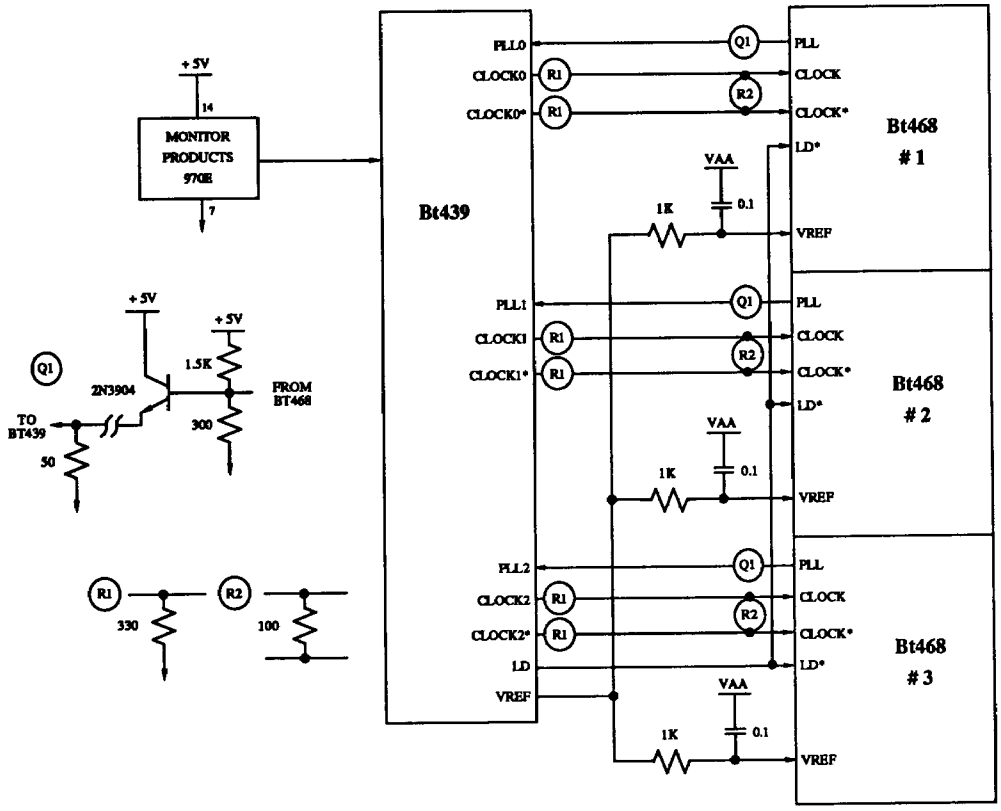


Figure 12. Generating the Clock Signals for Multiple Bt468s.

Application Information (continued)

Test Features of the Bt468

The Bt468 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Register (Signature Mode)

The signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color, and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as the three on-chip DACs.

The SARs act as a 24-bit wide Linear Feedback Shift Register on each succeeding pixel that is latched. It is important to note that the SARs only latch one pixel per "load group." Thus the SARs are operating on only every eighth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, D, E, F, G, or H) is latched for generating new signatures by setting bits D0–D2 in the Test Register.

The Bt468 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt468 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit "seed" value into the SARs. Then, a known pixel stream will be input to the chip, say one scan-line or one frame buffer worth of pixels. Then, at the succeeding blank state, the resultant 24-bit signature can be read out by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

The above process would be repeated with all different pixel phases—A, B, C, etc.,—being selected.

It is not simple to specify the algorithm which desceibes the linear feedback shift operation used in the Bt468. The linear feedback configuration is shown in Figure 13. Note that each register internally uses XORs at each input bit (D_n) with the output (result) by one least significant bit (Q_{n-1}).

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to "known-good" parts. Note that a good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed and the succeeding pixel stream fed to the SARs.

Signature Register (Data Strobe Mode)

Setting command bit CR20 to "1" puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs simply capture and hold the respective pixel phase that is selected.

Any MPU data written to the SARs is ignored. One use, however, is to directly check each pixel color value that is strobed into the SARs. To read out a captured color in the middle of a pixel stream, the user should first freeze all inputs to the Bt468. The levels of most inputs do not matter EXCEPT that CLOCK should be high, and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively.

In general, the color read out will correspond to a pixel latched on the previous load. However, due to the pipelined data path, the color may come from an earlier load cycle. To read successive pixels, toggle LD*, pulse the CLOCK pins according to the mux state (eight periods), then hold all pixel-related inputs and perform the three MPU reads as described. This overall process is best done on a sophisticated VLSI semiconductor Tester.

Application Information (continued)

Analog Comparator

The other dedicated test structure in the Bt468 is the analog output comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the Test Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Test Register on each of the 64 scan lines of the 64 x 64 user-defined cursor block (the 64 x 64 cursor must be enabled for display). On each of these 64 scan lines, the capture occurs over one LD* period that corresponds to the cursor (x) position, set by the 12-bit cursor (x) register.

To obtain a meaningful comparison, the cursor should be located on the visible screen. There is no significance to the cursor pattern data in the cursor RAM. For a visual reference, the capture point actually occurs over the left-most edge of the 64 x 64 cursor block.

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. In this case, the cursor (x) position should be set to well over 500 pixels to ensure an adequate supply of pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, up until capture.

Typically, users will create screen-wide test bands of various colors. Various comparison cases are set up by moving the cursor up and down (by changing the 12-bit cursor (y) register) over these bands. For each test, the result is obtained by reading Test Register bit D3.

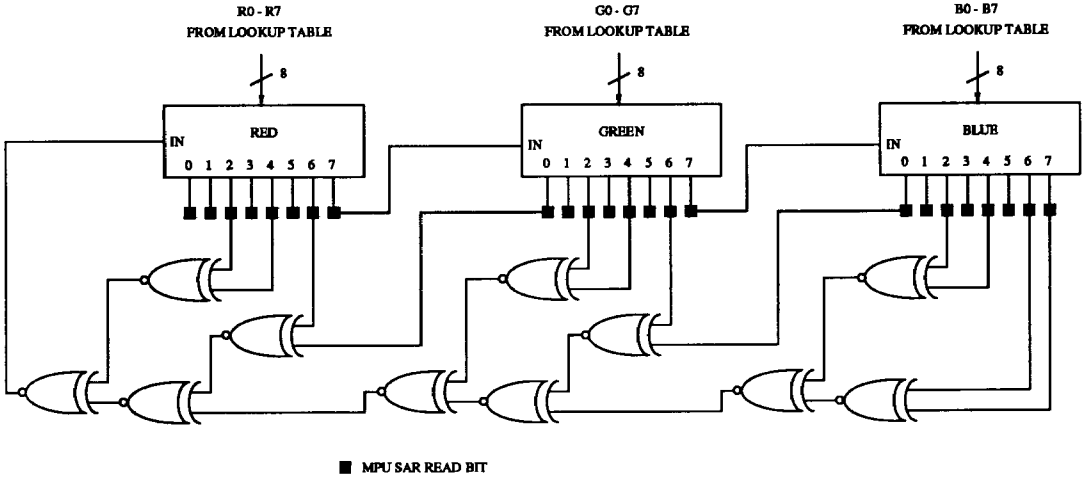


Figure 13. Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt468

Following a power-on sequence, the Bt468 must be initialized. This sequence will configure the Bt468 as follows:

8:1 multiplexed operation
no overlays, no blinking, no panning
64 x 64 block cursor, no cross hair cursor
sync enabled on IOG, 7.5 IRE blanking pedestal

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $00 to command register_1	10
Write $C0 to command register_2	10
Write $FF to pixel read mask register	10
Write $00 to reserved location	10
Write $00 to pixel blink mask register	10
Write $00 to reserved location	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to reserved location	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern

Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $00)	11
Write green data to RAM (location $00)	11
Write blue data to RAM (location $00)	11
Write red data to RAM (location $01)	11
Write green data to RAM (location $01)	11
Write blue data to RAM (location $01)	11
:	:
Write red data to RAM (location $FF)	11
Write green data to RAM (location $FF)	11
Write blue data to RAM (location $FF)	11

Overlay Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization

Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		25		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		348		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	Volts
Voltage on any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND – 0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Input Differntial Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		26.56	28.56	30.56	mA
White Level Relative to Black		25.08	26.40	27.72	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		1.48	2.16	2.84	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		9.44	11.44	13.44	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			103.5		µA
DAC-to-DAC Matching				5	%
Output Compliance	VOC	-0.5		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance	CAOUT		13	20	pF
(f = 1 MHz, IOUT = 0 mA)					
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		9	11.44	14	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		-1.0		+2.5	Volts
Output Impedance			50		kΩ
Output Capacitance			10		pF
(f = 1 MHz, PLL = 0 mA)					
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio	PSRR		0.5		%/% ΔVAA
(COMP = 0.1 µF, f = 1 kHz)					

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 348 Ω, VREF = 1.235 V. SETUP = 7.5 IRE with 50 Ω double termination. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	200 MHz Devices Min	200 MHz Devices Typ	200 MHz Devices Max	170 MHz Devices Min	170 MHz Devices Typ	170 MHz Devices Max	Units
Clock Rate	Fmax			200			170	MHz
LD* Rate	LDmax			25			21.25	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	10			10			ns
CE* Low Time	3	45			45			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			45			45	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	20			20			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	5			5.88			ns
Clock Pulse Width High Time	13	2.2			2.5			ns
Clock Pulse Width Low Time	14	2.2			2.5			ns
LD* Cycle Time	15	40			47			ns
LD* Pulse Width High Time	16	15			20			ns
LD* Pulse Width Low Time	17	15			20			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		1			1		ns
Analog Output Settling Time	20			tbd			tbd	ns
Clock and Data Feedthrough*			tbd			tbd		dB
Glitch Impulse*			50			50		pV - sec
DAC to DAC Crosstalk			tbd			tbd		dB
Analog Output Skew			0	1		0	1	ns
Pipeline Delay		6		13	6		13	Clocks
VAA Supply Current**	IAA		450	tbd		430	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 348 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 15. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0 V, TA = 25° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms

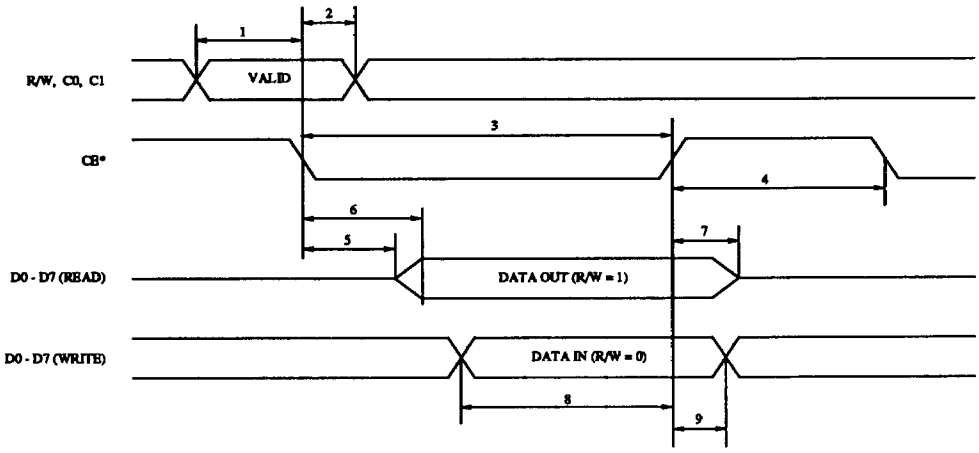
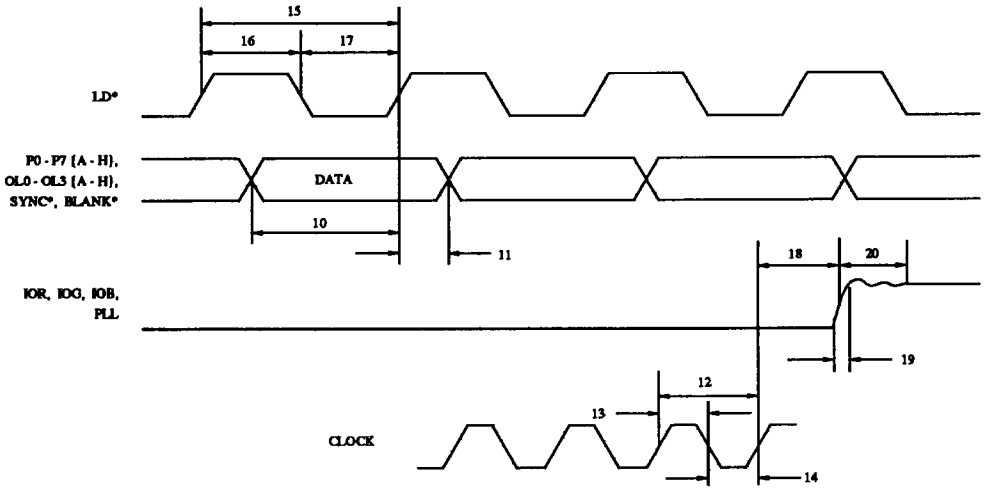


Figure 14. MPU Read/Write Timing Dimensions.



Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 15. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt468KG200	200 MHz	145-pin Ceramic PGA	0° to +70° C
Bt468KG170	170 MHz	145-pin Ceramic PGA	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
B	Full datasheet.
C	Cursor position panning, RSET value changed to match 50 Ω termination. Analog output DC parametrics.
D	Added double reset, modified PLL feedback circuitry.