Features

- **Serial Peripheral Interface (SPI) Compatible**
- **Supports SPI Modes 0 (0,0) and 3 (1,1)**
  - **Datasheet Describes 0 Operation**
- **20 MHz Clock Rate**
- **Byte Mode and 128-byte Page Mode for Program Operations**
- **Sector Architecture:**
  - **Two Sectors with 32K Bytes Each**
  - **256 Pages per Sector**
- **Product Identification Mode**
- **Low-voltage Operation**
  - **2.7 (V_{CC} = 2.7 to 3.6V)**
- **Sector Write Protection**
- **Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for both Hardware and Software Data Protection**
- **Self-timed Program Cycle (75 µs/byte typical)**
- **Self-timed Sector Erase Cycle (1 second/sector typical)**
- **Single Cycle Reprogramming (Erase and Program) for Status Register**
- **High Reliability**
  - **Endurance: 10,000 Write Cycles Typical**
- **8-lead JEDEC SOIC and 8-lead SAP Packages**

Description

The AT25F512A provides 524,288 bits of serial reprogrammable Flash memory organized as 65,536 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25F512A is available in a space-saving 8-lead JEDEC SOIC and 8-lead SAP packages.

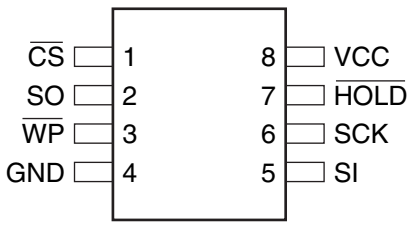
The AT25F512A is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All write cycles are completely self-timed.

Block write protection for the entire memory array is enabled by programming the status register. Separate write enable and write disable instructions are provided for additional data protection. Hardware data protection is provided via the Write Protect ($\overline{WP}$) pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

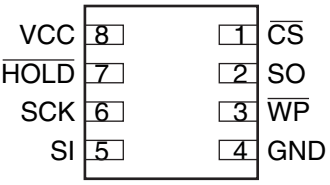
Table 1. Pin Configuration

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

8-lead SOIC



8-lead SAP



Bottom View

SPI Bus Serial Flash, High Speed, SPI Mode 0 & 3

512K (65,536 x 8)

AT25F512A

Preliminary

Recommended for New Designs

Absolute Maximum Ratings*

Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +5.0V
Maximum Operating Voltage	4.2V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram

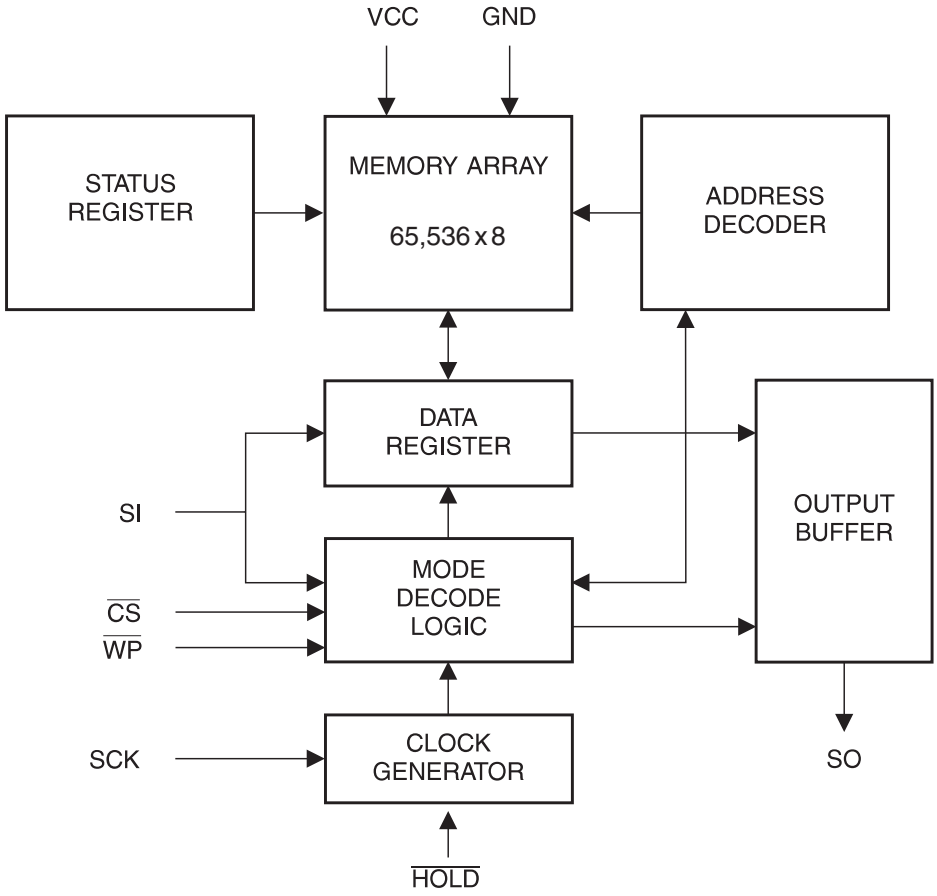


Table 2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 20 MHz, V_{CC} = +3.6V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 3. DC Characteristics[1]

Applicable over recommended operating range from: T_{AI} = –40 to +85°C, V_{CC} = +2.7 to +3.6V, T_{AC} = 0 to +70°C, V_{CC} = +2.7 to +3.6V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			2.7		3.6	V
I_{CC1}	Supply Current	V_{CC} = 3.6V at 20 MHz, SO = Open Read			10.0	15.0	mA
I_{CC2}	Supply Current	V_{CC} = 3.6V at 20 MHz, SO = Open Write			25.0	35.0	mA
I_{SB}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}; SCK, SI, $\overline{WP}$, $\overline{HOLD}$ = 0V or V_{CC}			2.0	10.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V or V_{CC}		–3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V or V_{CC}, T_{AI} = –40°C to 85°C		–3.0		3.0	µA
V_{IL}[2]	Input Low Voltage			–0.6		V_{CC} x 0.3	V
V_{IH}[2]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH}	Output High Voltage		I_{OH} = –100 µA	V_{CC} – 0.2			V

Note: 1. Preliminary – subject to change

2. V_{IL} and V_{IH} max are reference only and are not tested.

Table 4. AC Characteristics[1]

Applicable over recommended operating range from T_{AI} = –40 to +85°C, V_{CC} = +2.7 to +3.6V
C_L = 1 TTL Gate and 30 pF (unless otherwise noted).

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Clock Frequency	0		20	MHz
t_{RI}	Input Rise Time			20	ns
t_{FI}	Input Fall Time			20	ns
t_{WH}	SCK High Time	20			ns
t_{WL}	SCK Low Time	20			ns
t_{CS}	$\overline{CS}$ High Time	25			ns
t_{CSS}	$\overline{CS}$ Setup Time	25			ns
t_{CSH}	$\overline{CS}$ Hold Time	25			ns
t_{SU}	Data In Setup Time	5			ns
t_H	Data In Hold Time	5			ns
t_{HD}	$\overline{Hold}$ Setup Time	15			ns
t_{CD}	$\overline{Hold}$ Time	15			ns
t_V	Output Valid			20	ns
t_{HO}	Output Hold Time	0			ns
t_{LZ}	$\overline{Hold}$ to Output Low Z			200	ns
t_{HZ}	$\overline{Hold}$ to Output High Z			200	ns
t_{DIS}	Output Disable Time			100	ns
t_{EC}	Erase Cycle Time per Sector			1.1	s
t_{SR}	Status Register Write Cycle Time			60	ms
t_{BPC}	Byte Program Cycle Time[2]		75	100	µs
Endurance[3]			10K		Write Cycles[4]

Notes:
1. Preliminary – subject to change
2. The programming time for n bytes will be equal to n x t_{BPC}.
3. This parameter is characterized at 3.0V, 25°C and is not 100% tested.
4. One write cycle consists of erasing a sector, followed by programming the same sector.

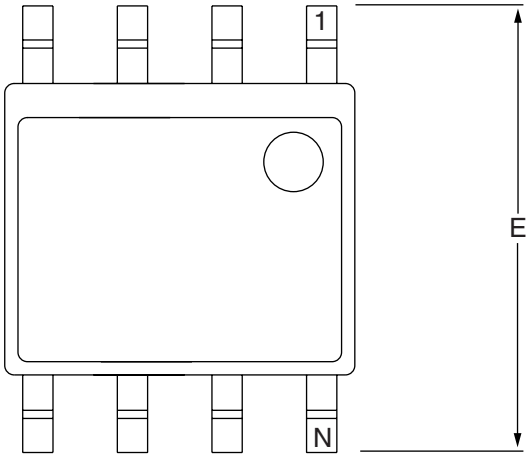
Ordering Information

Ordering Code	Package	Operation Range
AT25F512AN-10SU-2.7	8S1	Lead-free/Halogen-free Industrial
AT25F512AY4-10YU-2.7	8Y4	(–40 to 85°C)

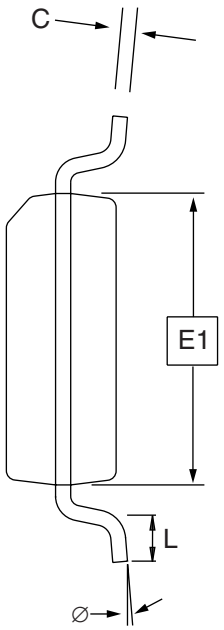
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8Y4	8-lead, 6.00 mm x 4.90 mm Body, Dual Footprint, Non-leaded, Small Array Package (SAP)
Options	
–2.7	Low-voltage (2.7 to 3.6V)

Packaging Information

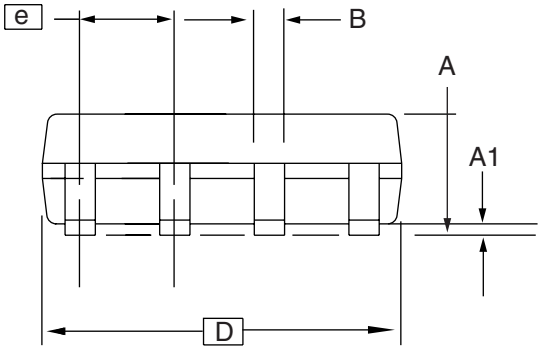
8S1 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B