ON Semiconductor®

ASM3P2111B

Peak EMI Reducing Solution

Features

- Generates an EMI optimized clock at the output.
- Input frequency: 25MHz.
- Frequency outputs:
  - o 60MHz (unmodulated)
  - o 2 x 48MHz (unmodulated)
  - o 66.6MHz (modulated): -1.7% down spread
- Modulation rate: 30KHz.
- Supply voltage range: 3.3V ± 0.3V.
- Available in 8-pin SOIC Package.
- RoHS Compliant

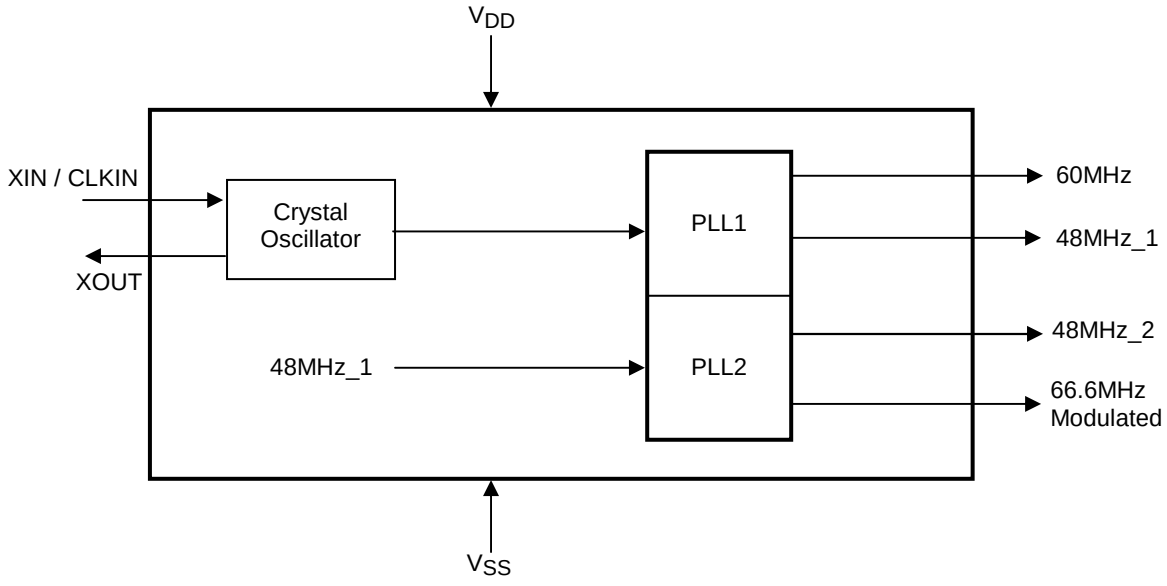
Product Description

The ASM3P2111B is a versatile spread spectrum frequency modulator that reduces electromagnetic interference (EMI) at the clock source. The ASM3P2111B allows significant system cost savings by reducing the number of circuit board layers and shielding that are required to pass EMI regulations. The ASM3P2111B modulates the output of PLL in order to spread the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation.

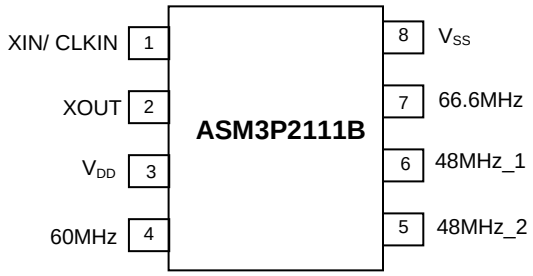
Applications

ASM3P2111B is targeted towards EMI management for high speed digital applications such as PC peripheral devices, consumer electronics and embedded controller systems.

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
1	XIN / CLKIN	I	Connection to crystal
2	XOUT	O	Connection to crystal
3	V_{DD}	P	Power supply for the analog and digital blocks (+3.3V)
4	60MHz	O	Clock output-1 60MHz un-modulated
5	48MHz_2	O	Clock output-2 48MHz_2 un-modulated
6	48MHz_1	O	Clock output-3 48MHz_1 un-modulated
7	66.6MHz	O	Clock output-4 66.6MHz modulated
8	V_{SS}	P	Ground to entire chip. Connect to System Ground

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3	3.3	3.6	V
F_{XIN}	Crystal Resonator Frequency		25		MHz
T_A	Operating Temperature	-40		+85	℃
C_L	Output Driver Load Capacitance			15	pF

DC Electrical Characteristics

Parameter	Symbol	Conditions / Description	Min	Typ	Max	Unit
Overall						
Supply Current, Dynamic	I_{DD}	V_{DD} = 3.3V, F_{CLK} = 25MHz, C_L = 15pF	41	48	62	mA
Supply Current, Static	I_{DDL}	V_{DD} = 3.3V, Clock Input = 0	20	25	35	mA
All input pins						
High-Level Input Voltage	V_{IH}	V_{DD} = 3.3V	2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}	V_{DD} =3.3V	V_{SS}-0.3		0.8	V
High-Level Input Current	I_{IH}		-1		1	µA
Low-Level Input Current (pull-up)	I_{IL}		-20	-36	-80	µA
High-Level Output Source Current	I_{xOH}	V_{DD} = V (XIN) = 3.3V, V_O= 0.4V		3		mA
Low-Level Output Sink Current	I_{xOL}	V_{DD} = 3.3V, V (XIN) = V_O = 2.5V		3		mA
Clock Outputs						
High-Level Output Source Current	I_{OH}	V_O = 2.5V		-20		mA
Low-Level Output Sink Current	I_{OL}	V_O = 0.4V		23		mA
Output Impedance	Z_{OH}	V_O = 0.5 V_{DD}; output driving high		29		Ω
	Z_{OL}	V_O = 0.5 V_{DD}; output driving low		27		

AC Electrical Characteristics

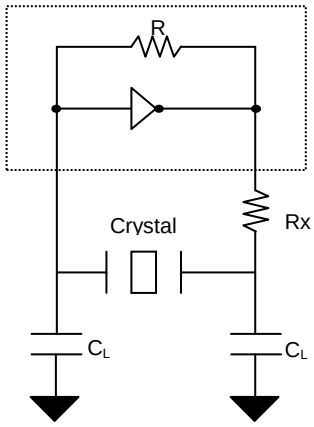
Parameter	Symbol	Conditions / Description	Min	Typ	Max	Unit
Rise Time	t_r	V_O = 0.8V to 2.0V; C_L = 15pF	300	800	900	pS
Fall Time	t_f	V_O = 2.0V to 0.8V; C_L = 15pF	360	800	900	pS
Clock Duty Cycle		Ratio of pulse width (as measured from rising edge to next falling edge at V_{DD}/2) to one clock period	45		55	%
Note: 1. C_L = 15pF, Input clock frequency = 25MHz.						

Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	25MHz
Frequency tolerance	± 50 ppm or better at 25℃
Operating temperature range	-25℃ to +85℃
Storage temperature	-40℃ to +85℃
Load capacitance(C_P)	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

Note: Note: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

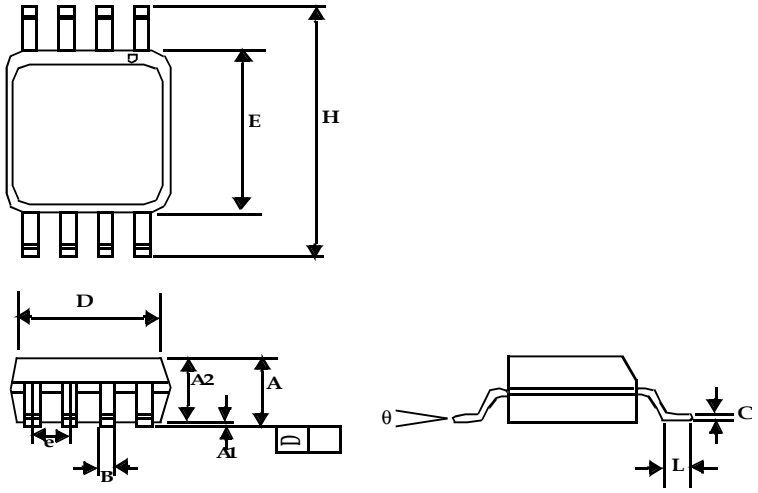
Typical Crystal Interface Circuit



$C_L = 2*(C_P – C_S)$,
Where C_P = Load capacitance of crystal
C_S = Stray capacitance due to $C_{IN,}$ PCB, Trace etc.

Package Information

8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Ordering Codes

Part number	Marking	Package Configuration	Temperature Range
ASM3P2111BG-08SR	AEI	8-pin SOIC TAPE & REEL, Green	0℃ to +70℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free

Note: This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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