Am9114/Am91L14

1024x4 Static RAM

DISTINCTIVE CHARACTERISTICS

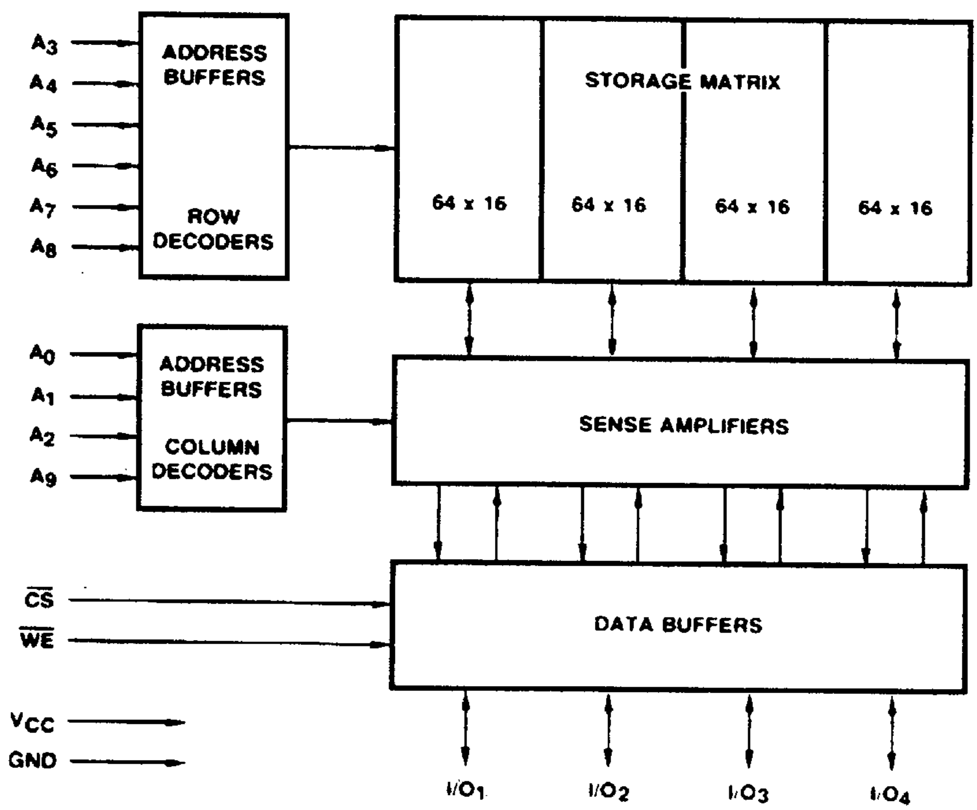
- Low operating and standby power
- Access times down to 200 ns
- Am9114 is a direct plug-in replacement for 2114
- High output drive: 3.2-mA sink current @ 0.4 V
- TTL-identical input/output levels

GENERAL DESCRIPTION

The Am91 . Am91L14 Series are high-performance, static, N-Chann..., read/write, random-access memories organized as 1024 x 4. Operation is from a single 5-V supply, and all input/output levels are identical to standard TTL specifications. Low-power version is available with power savings of over 30%.

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 3.2 mA for Am9114 provides increased short-circuit current for improved capacitive drive.

BLOCK DIAGRAM



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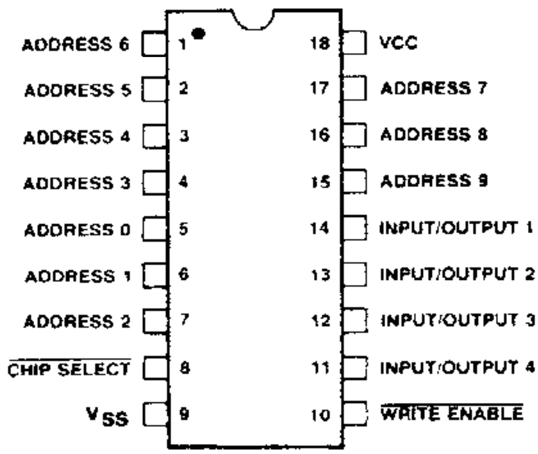
PRODUCT SELECTOR GUIDE

Part Number			Am9114/91L14		Am9114/91L14
Speed Indicator			B	C	E
Maximum Access Time (ns)			450	300	200
0 to +70°C	I_{CC} (mA)	Standard	70	70	70
		Low-Power	50	50	50
−55 to +125°C	I_{CC} (mA)	Standard	80	80	80
		Low-Power	60	60	60

CONNECTION DIAGRAM

Top View

DIPs



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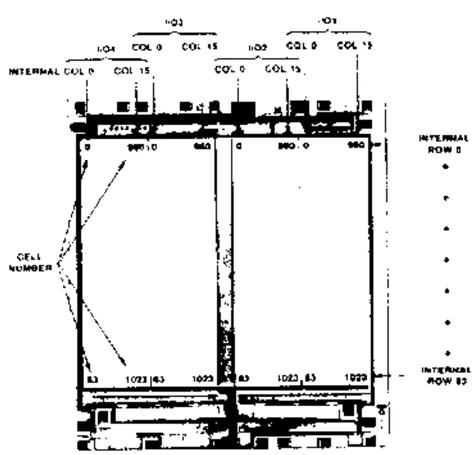
Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A_0	A_9
A_1	A_8
A_2	A_7
A_3	A_0
A_4	A_1
A_5	A_2
A_6	A_3
A_7	A_4
A_8	A_5
A_9	A_6



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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM9114 E D C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 18-Pin Plastic DIP (PD 018)
D = 18-Pin Ceramic DIP (CD 018)

b. SPEED OPTION
B = 450 ns
C = 300 ns
E = 200 ns

a. DEVICE NUMBER/DESCRIPTION
Am9114/Am91L14
1024 x 4 Static RAM
Am91L14 = Low-Power Version

Valid Combinations	
AM9114B	PC, PCB, DC, DCB
AM91L14B	
AM9114C	
AM91L14C	
AM9114E	
AM91L14E	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**

b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM9124 B /B V A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
V = 18-Pin Ceramic DIP (CD 018)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
B = 450 ns
C = 300 ns
E = 200 ns

a. DEVICE NUMBER/DESCRIPTION
Am9114/Am91L14
1024 x 4 Static RAM
Am91L14 = Low-Power Version

Valid Combinations	
AM9114B	/BVA
AM91L14B	
AM9114C	
AM91L14C	
AM9114E	
AM91L14E	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The address input lines select the memory location from which to read or write.

$\overline{CS}$ $\overline{\text{Chip Select}}$ (Input, Active LOW)
The $\overline{CS}$ line selects the memory device for active operation.

$\overline{WE}$ $\overline{\text{Write Enable}}$ (Input, Active LOW)
When both $\overline{CS}$ and $\overline{WE}$ are LOW, data on the input lines is written to the location presented on the address input lines.

$I/O_1 - I/O_4$ Data In/Out Bus (Bidirectional)
These lines provide the path for data to be written to or read from the selected memory location.

V_{CC} Power Supply

V_{SS} Ground

TABLE 1. SUPPLY CURRENT ADVANTAGE

		Worst Case Current (mA at 0°C)	
Configuration	**Part Number**	**100% Duty Cycle**	**50% Duty Cycle**
2K x 8	9114 91L14	280 200	280 200
4K x 12	9114 91L14	840 600	840 600
8K x 16	9114 91L14	2240 1600	2240 1600

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .... −65 to +150°C
Ambient Temperature with
Power Applied .... −55 to +125°C
Supply Voltage .... −0.5 V to +7.0 V
Signal Voltages with
Respect to Ground .... −0.5 V to +7.0 V
Power Dissipation .... 1.0 W
DC Output Current .... 10 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Ambient Temperature (T_A) .... 0°C to +70°C
Supply Voltage (V_{CC}) .... +4.5V to +5.5 V

Military (M) Devices*
Case Temperature (T_C) .... −55°C to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military products 100% tested at T_C = +25°C, +125°C and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
I_{OH}	Output HIGH Current	V_{CC} = +4.5V, V_{OH} = 2.4V	91(L)14		−1.0		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4V	T_A = 70°C	91(L)14	3.2		mA
			T_A = +125°C	91(L)14	2.4		
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10	μA
I_{OZ}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$ Output Disabled	T_A = 0 to +70°C		−10	10	μA
			T_A = −55 to +125°C		−50	50	
I_{OS}	Output Short Circuit Current	(Note 3)	91(L)14C			75	mA
			91(L)14M			75	
I_{CC}	Operating Supply Current	V_{CC} = Max. $\overline{CS} \leq V_{IL}$	T_A = 0°C	Standard devices		70	mA
				L devices		50	
			T_A = −55°C	Standard devices		80	
				L devices		60	
C_{IN}	Input Capacitance	(Note 7)	f = 1.0 MHz, T_A = 25°C, All pins at 0V			7	pF
$C_{I/O}$	I/O Capacitance					7	

Notes: 1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the "Instant-ON" case temperature.
3. For test purposes, not more than one output at a time should be shorted. Short-circuit test duration should not exceed 30 seconds. Actual testing is performed for only 5 ms.
4. Test conditions assume signal transition time of 10 ns or less, timing reference levels of 1.5 V, output loading of the specified I_{OL}/I_{OH} plus 100 pF or plus 5 pF for T_{CX}, T_{OTD} and T_{OTW}.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. The specified address access time will be valid only when Chip Select is low soon enough for t_{CO} to elapse.
7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
8. Transition is measured from 1.5 V on the input to (V_{OH} − 500 mV) and (V_{OL} + 500 mV) on the output.

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SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 4 – 6)

No.	Parameter Symbol	Parameter Description	B Devices Min.	B Devices Max.	C Devices Min.	C Devices Max.	E Devices Min.	E Devices Max.	Unit
READ CYCLE									
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)	450		300		200		ns
2	t_A	Address Valid to Data Out Valid Delay (Address Access Time)		450		300		200	ns
3	t_{CO}	Chip Select LOW to Data Out Valid (Note 6)		120		100		70	ns
4	t_{CX}	Chip Select LOW to Data Out On (Notes 7, 8)	10		10		10		ns
5	t_{OTD}	Chip Select HIGH to Data Out Off (Notes 7, 8)		100		80		60	ns
6	t_{OHA}	Output hold after address change	50		50		50		ns
WRITE CYCLE									
7	t_{WC}	Address Valid to Address Do Not Care Time (Write Cycle Time)	450		300		200		ns
8	t_W	Write Enable LOW to Write Enable HIGH Time (Note 5)	200		150		120		ns
9	t_{WR}	Write Enable HIGH to Address Do Not Care Time	0		0		0		ns
10	t_{OTW}	Write Enable LOW to Data Out Off Delay (Notes 7, 8)		100		80		60	ns
11	t_{DW}	Data In Valid to Write Enable HIGH Time	200		150		120		ns
12	t_{DH}	Write Enable HIGH to Data In Do Not Care Time	0		0		0		ns
13	t_{AW}	Address Valid to Write Enable LOW Time	0		0		0		ns
14	t_{CW}	Chip Select LOW to Write Enable HIGH Time (Note 5)	200		150		120		90

Notes: See notes following DC Characteristics table.

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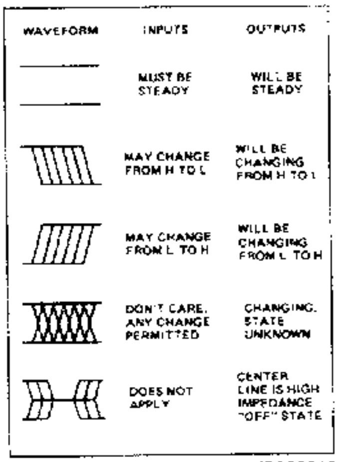
SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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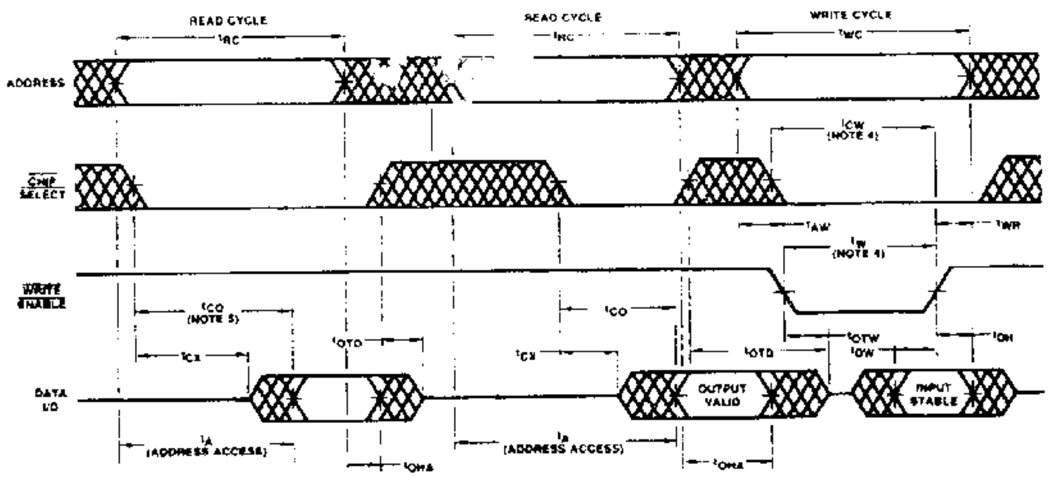

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Notes: See notes following DC Characteristics table.

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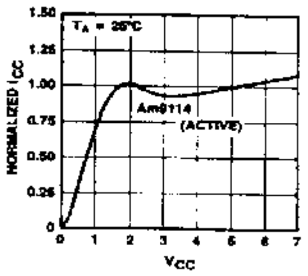
TYPICAL PERFORMANCE CURVES

Normalized Supply Current Versus Supply Voltage



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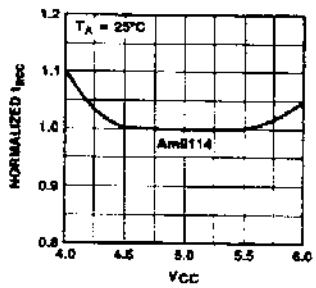
Normalized Access Time Versus Supply Voltage



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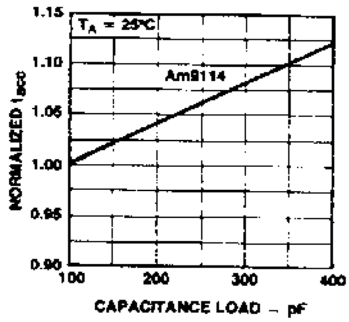
Normalized Access Time Versus Output Loading



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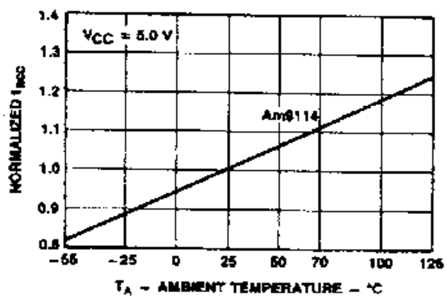
Normalized Access Time Versus Ambient Temperature



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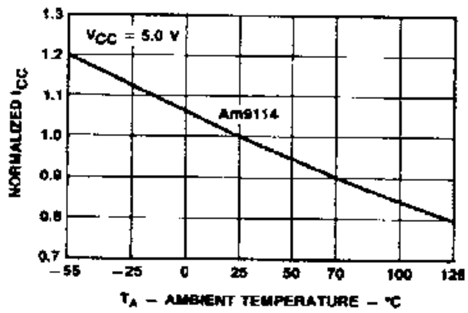
Normalized Supply Current Versus Ambient Temperature



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