



Am29F400AT/Am29F400AB

4 Megabit (524,288 x 8-Bit/262,144 x 16-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V \pm 10% for read and write operations**
 - Minimizes system level power requirements
- **Compatible with JEDEC-standards**
 - Pinout and software compatible with single-power-supply flash
 - Superior inadvertent write protection
- **Package options**
 - 44-pin SO
 - 48-pin TSOP
- **Minimum 100,000 write/erase cycles guaranteed**
- **High performance**
 - 60 ns maximum access time
- **Sector erase architecture**
 - One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and seven 64 Kbytes
 - Any combination of sectors can be erased. Also supports full chip erase.
- **Sector protection**
 - Hardware method that disables any combination of sectors from write or erase operations. Implemented using standard PROM programming equipment.
- **Embedded Erase™ Algorithms**
 - Automatically preprograms and erases the chip or any sector
- **Embedded Program™ Algorithms**
 - Automatically programs and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/BY)**
 - Hardware method for detection of program or erase cycle completion
- **Erase Suspend/Resume**
 - Supports reading data from a sector not being erased
- **Low power consumption**
 - 20 mA typical active read current for Byte Mode
 - 28 mA typical active read current for Word Mode
 - 30 mA typical program/erase current
- **Enhanced power management for standby mode**
 - 1 μ A typical standby current
- **Boot Code Sector Architecture**
 - T = Top sector
 - B = Bottom sector
- **Hardware RESET pin**
 - Resets internal state machine to the read mode

5.0 V-only Flash

GENERAL DESCRIPTION

The Am29F400A is a 4 Mbit, 5.0 Volt-only Flash memory organized as 512 Kbytes of 8 bits each or 256 Kwords of 16 bits each. The 4 Mbits of data is divided into 11 sectors of one 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbytes, for flexible erase capability. The 8 bits of data will appear on DQ0–DQ7 or 16 bits on DQ0–DQ15. The Am29F400A is offered in 44-pin SO and 48-pin TSOP packages. This device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. 12.0 Volt V_{PP} is not required for program or erase operations. The device can also be re-programmed in standard EPROM programmers.

The standard Am29F400A offers access times of 60 ns, 70 ns, 90 ns, 120 ns and 150 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (\overline{CE}), write enable (\overline{WE}) and output enable (\overline{OE}) controls.

The Am29F400A is entirely command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry.

Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 Volt Flash or EPROM devices.

The Am29F400A is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This device also features a sector erase architecture. This allows for sectors of memory to be erased and re-programmed without affecting the data contents of other sectors. A sector is typically erased and verified within 1.5 seconds. The Am29F400A is erased when shipped from the factory.

The Am29F400A device also features hardware sector protection. This feature will disable both program and erase operations in any combination of eleven sectors of memory.

AMD has implemented an Erase Suspend feature that enables the user to put erase on hold for any period of time to read data from a sector that was not being erased. Thus, true background erase can be achieved.

The device features single 5.0 Volt power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by the $\overline{RY/BY}$ pin. Data Polling of DQ7, or by the Toggle Bit (DQ6). Once the end of a program or erase cycle has been completed, the device automatically resets to the read mode.

The Am29F400A also has a hardware \overline{RESET} pin. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm will be terminated. The internal state machine will then be reset into the read mode. The \overline{RESET} pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program Algorithm or Embedded Erase Algorithm, the device will be automatically reset to the read mode and will have erroneous data stored in the address locations being operated on. These locations will need rewriting after the Reset. Resetting the device will enable the system's microprocessor to read the boot-up firmware from the Flash memory.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F400A memory electrically erases all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

Flexible Sector-Erase Architecture

- One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and seven 64 Kbyte sectors
- Individual-sector or multiple-sector erase capability
- Sector protection is user definable

		(x8)	(x16)
SA10	16 Kbyte	7FFFFh	3FFFFh
SA9	8 Kbyte	7BFFFh	3DFFFh
SA8	8 Kbyte	79FFFh	3CFFFh
SA7	32 Kbyte	77FFFh	3BFFFh
SA6	64 Kbyte	6FFFFh	37FFFh
SA5	64 Kbyte	5FFFFh	2FFFFh
SA4	64 Kbyte	4FFFFh	27FFFh
SA3	64 Kbyte	3FFFFh	1FFFFh
SA2	64 Kbyte	2FFFFh	17FFFh
SA1	64 Kbyte	1FFFFh	0FFFFh
SA0	64 Kbyte	0FFFFh	07FFFh
		00000h	00000h

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Am29F400AT Sector Architecture

		(x8)	(x16)
SA10	64 Kbyte	7FFFFh	3FFFFh
SA9	64 Kbyte	6BFFFh	37FFFh
SA8	64 Kbyte	5FFFFh	2FFFFh
SA7	64 Kbyte	4FFFFh	27FFFh
SA6	64 Kbyte	3FFFFh	1FFFFh
SA5	64 Kbyte	2FFFFh	17FFFh
SA4	64 Kbyte	1FFFFh	0FFFFh
SA3	32 Kbyte	0FFFFh	07FFFh
SA2	8 Kbyte	07FFFh	03FFFh
SA1	8 Kbyte	05FFFh	02FFFh
SA0	16 Kbyte	03FFFh	01FFFh
		00000h	00000h

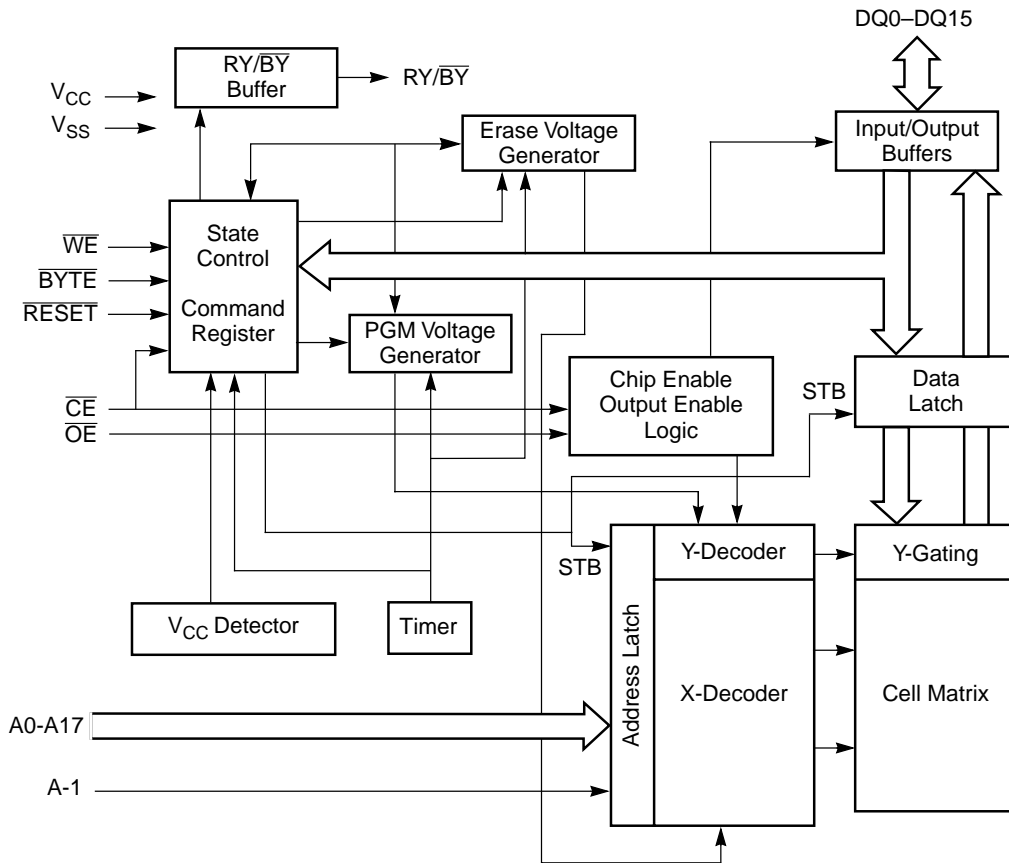
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Am29F400AB Sector Architecture

PRODUCT SELECTOR GUIDE

Family Part No:	Am29F400A				
Ordering Part No: $V_{CC} = 5.0\text{ V} \pm 5\%$	-65				
$V_{CC} = 5.0\text{ V} \pm 10\%$		-70	-90	-120	-150
Max Access Time (ns)	60	70	90	120	150
\overline{CE} (\overline{E}) Access (ns)	60	70	90	120	150
\overline{OE} (\overline{G}) Access (ns)	30	30	35	50	55

BLOCK DIAGRAM

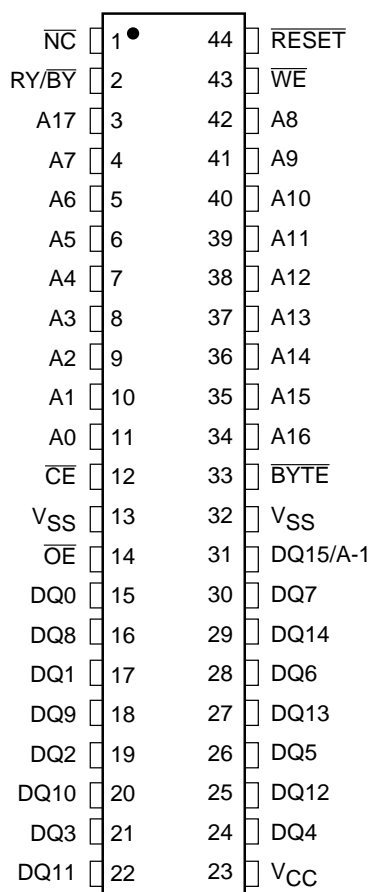


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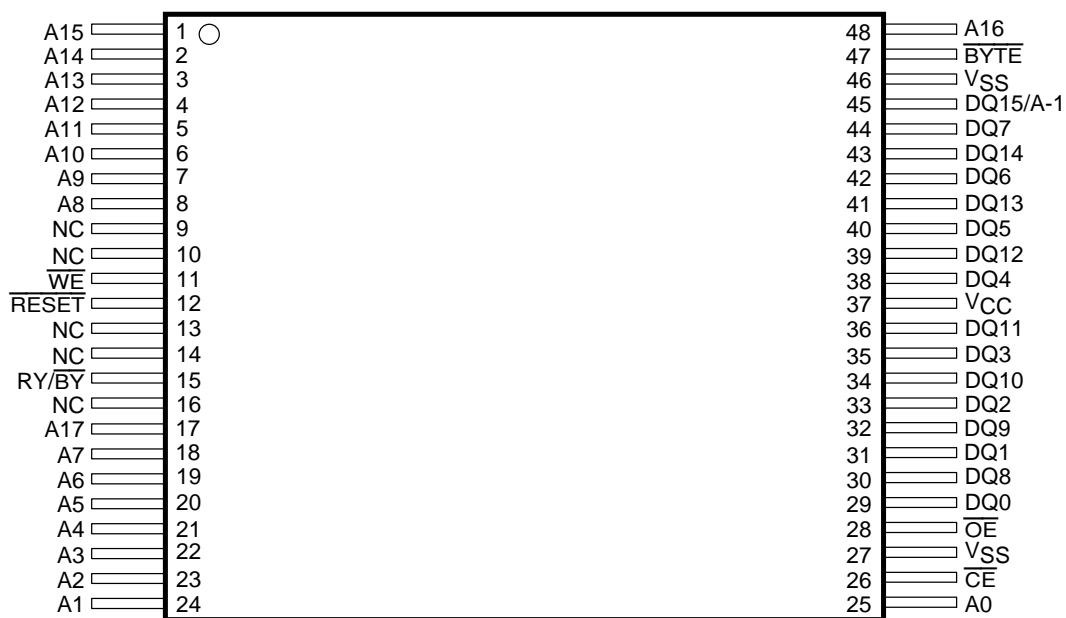
CONNECTION DIAGRAMS

SO



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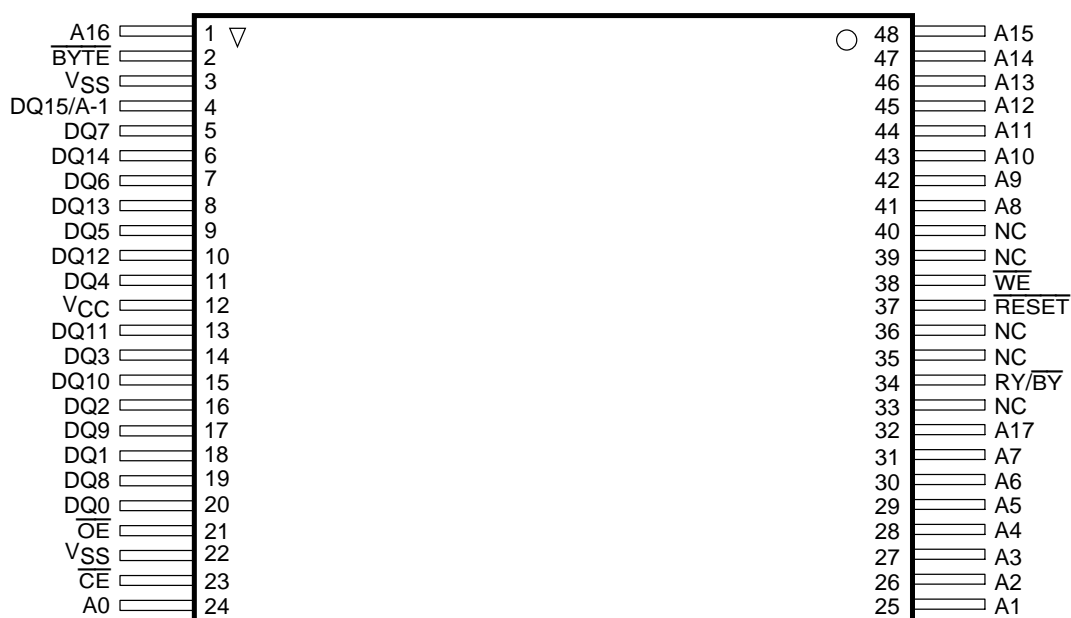
CONNECTION DIAGRAMS



Standard TSOP

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Reverse TSOP

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PIN CONFIGURATION

A1, A0–A17 = 18 Addresses

$\overline{\text{BYTE}}$ = Selects 8-bit or 16-bit mode

$\overline{\text{CE}}$ = Chip Enable

DQ0–DQ15 = 16 Data Inputs/Outputs

NC = Pin Not Connected Internally

$\overline{\text{OE}}$ = Output Enable

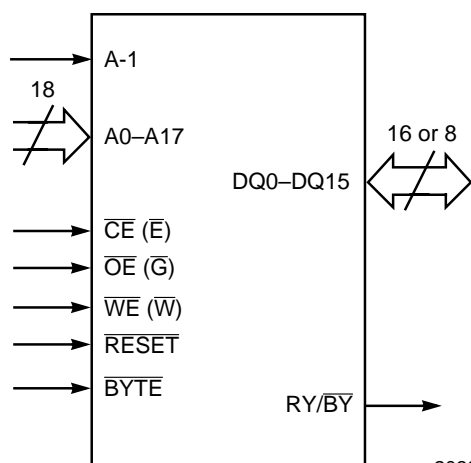
$\overline{\text{RESET}}$ = Hardware Reset Pin, Active Low

RY/ $\overline{\text{BY}}$ = Ready/ $\overline{\text{Busy}}$ Output

V_{SS} = +5.0 Volt Single-Power Supply
($\pm 10\%$ for -90, -120, -150) or ($\pm 5\%$ for -75)

V_{SS} = Device Ground

$\overline{\text{WE}}$ = Write Enable

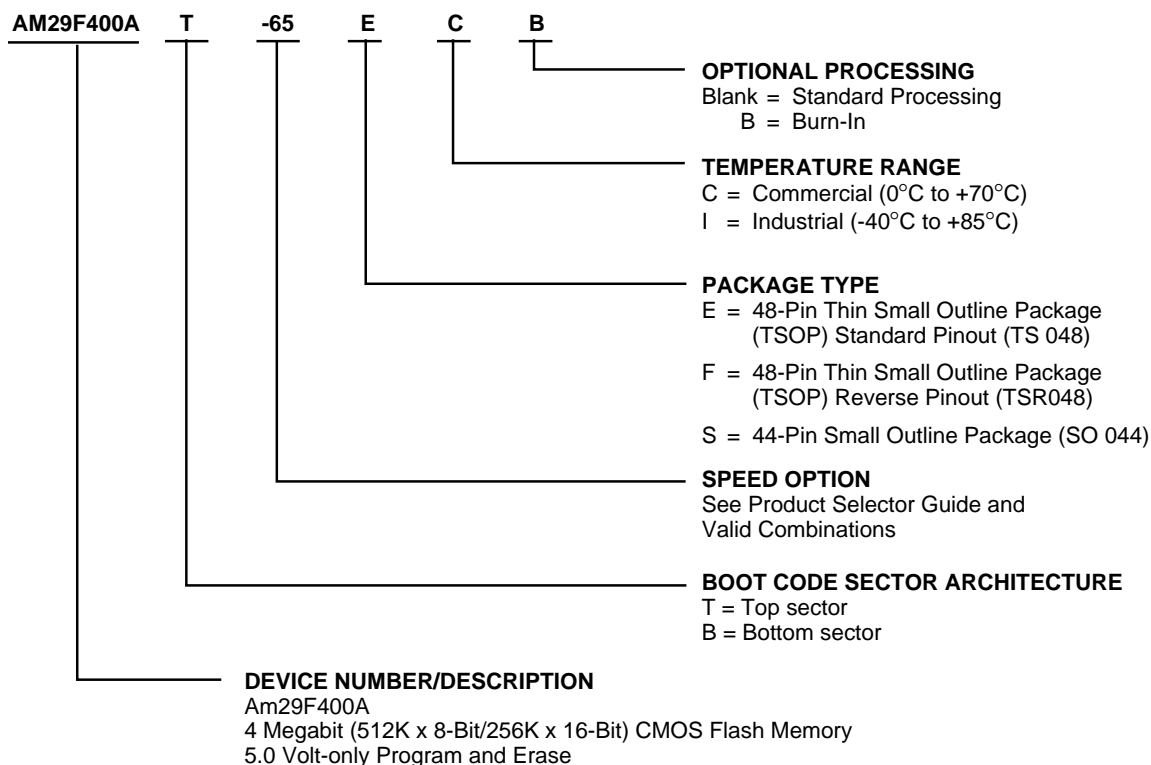
LOGIC SYMBOL


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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



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Valid Combinations	
AM29F400AT/B-65	EC, EI, FC, FI, SC, SI
AM29F400AT/B-70	EC, EI, EE, EEB, FC, FI, FE, FEB, SC, SI, SE, SEB
AM29F400AT/B-90	
AM29F400AT/B-120	
AM29F400AT/B-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1. Am29F400A User Bus Operations ($\overline{\text{BYTE}} = V_{IH}$)

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0	A1	A6	A9	DQ0–DQ15	$\overline{\text{RESET}}$
Autoselect, AMD Manuf. Code (Note 1)	L	L	H	L	L	L	V_{ID}	Code	H
Autoselect Device Code (Note 1)	L	L	H	H	L	L	V_{ID}	Code	H
Read	L	L	H	A0	A1	A6	A9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	HIGH Z	H
Output Disable	L	H	H	X	X	X	X	HIGH Z	H
Write	L	H	L	A0	A1	A6	A9	D_{IN}	H
Verify Sector Protect (Note 2)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V_{ID}
Hardware Reset	X	X	X	X	X	X	X	HIGH Z	L

Table 2. Am29F400A User Bus Operations ($\overline{\text{BYTE}} = V_{IL}$)

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0	A1	A6	A9	DQ0–DQ7	DQ8–DQ15	$\overline{\text{RESET}}$
Autoselect, AMD Manuf. Code (Note 1)	L	L	H	L	L	L	V_{ID}	Code	HIGH Z	H
Autoselect Device Code (Note 1)	L	L	H	H	L	L	V_{ID}	Code	HIGH Z	H
Read	L	L	H	A0	A1	A6	A9	D_{OUT}	HIGH Z	H
Standby	H	X	X	X	X	X	X	HIGH Z	HIGH Z	H
Output Disable	L	H	H	X	X	X	X	HIGH Z	HIGH Z	H
Write	L	H	L	A0	A1	A6	A9	D_{IN}	HIGH Z	H
Verify Sector Protect (Note 2)	L	L	H	L	H	L	V_{ID}	Code	HIGH Z	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	HIGH Z	V_{ID}
Hardware Reset	X	X	X	X	X	X	X	HIGH Z	HIGH Z	L

Legend:

L = logic 0, H = logic 1, X = Don't Care. See Characteristics for voltage levels.

Notes:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 4.
2. Refer to the section on Sector Protection.

Read Mode

The Am29F400A has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{\text{CE}}$ is the power control and should be used for device selection. $\overline{\text{OE}}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{\text{CE}}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{\text{OE}}$ to valid data at the output pins (as-

suming the addresses have been stable for at least $t_{ACC} - t_{OE}$ time).

Standby Mode

There are two ways to implement the standby mode on the Am29F400A device, both using the $\overline{\text{CE}}$ pin.

A CMOS standby mode is achieved with the $\overline{\text{CE}}$ input held at $V_{CC} \pm 0.5$ V. Under this condition the current is typically reduced to less than 5 μA . A TTL standby mode is achieved with the $\overline{\text{CE}}$ pin held at V_{IH} . Under this condition the current is typically reduced to 1 mA.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{\text{OE}}$ input.

It is possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order address bits A12–A17 is the desired sector address, will produce a logical “1” at DQ0 for a protected sector. See Table 3 for Autoselect codes.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors of the Am29F400A device in order to change data in-system. The Sector Unprotect mode is activated by setting the $\overline{\text{RESET}}$ pin to high voltage (12V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the 12 V is taken away from

the $\overline{\text{RESET}}$ pin, all the previously protected sectors will be protected again. Refer to Figures 16 and 17.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. **Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode.** Table 7 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Moreover, both Reset/Read commands are functionally equivalent, resetting the device to the read mode.

accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 100 μ s from the rising edge of the last \overline{WE} will initiate the execution of the Sector Erase command(s). If another falling edge of the \overline{WE} occurs within the 100 μ s time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this period will reset the device to the read mode, ignoring the previous command string. In that case, restart the erase on those sectors and allow them to complete.

(Refer to the Write Operation Status section for DQ3, Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 10).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100 μ s time out from the rising edge of the \overline{WE} pulse for the last sector erase command pulse and terminates when the data on DQ7, Data Polling, is "1" (see Write Operation Status section) at which time the device returns to the read mode. Data Polling must be performed at an address within any of the sectors being erased.

Figure 1 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from a sector not being erased. This command is applicable **ONLY** during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are "don't-cares" when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15 μ s to suspend the erase operation. When the device has entered the erase-suspended mode, DQ6 will stop toggling. The user must use the address of a sector being erased for reading DQ6 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Write Operation Status

Table 8. Write Operation Status

	Status	DQ7	DQ6	DQ5	DQ3
In Progress	Auto-Programming	$\overline{DQ7}$	Toggle	0	0
	Program/Erase in Auto-Erase	0	Toggle	0	1
Exceeded Time Limits	Auto-Programming	$\overline{DQ7}$	Toggle	1	0
	Program/Erase in Auto-Erase	0	Toggle	1	1

Notes:

1. D8–D15 = Don't Care for x16 mode.
2. DQ4 for AMD internal use only.

RY/BY**Ready/Busy**

The Am29F400A provides a RY/BY open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or have been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/BY pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the Am29F400A is placed in an Erase Suspend mode, the RY/BY output will be high.

During programming, the RY/BY pin is driven low after the rising edge of the fourth WE pulse. During an erase operation, the RY/BY pin is driven low after the rising edge of the sixth WE pulse. The RY/BY pin should be ignored while RESET is at V_{IL} . Refer to Figure 12 for a detailed timing diagram.

Since this is an open-drain output, several RY/BY pins can be tied together in parallel with a pull-up resistor to V_{CC} .

RESET**Hardware Reset**

The Am29F400A device may be reset by driving the RESET pin to V_{IL} . The RESET pin must be kept low (V_{IL}) for at least 500 ns. Any operation in progress will be terminated and the internal state machine will be reset to the read mode 20 μ s after the RESET pin is driven low. Furthermore, once the RESET pin goes high, the device requires an additional 50 ns before it will allow read access. When the RESET pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be indeterminate.

The RESET pin may be tied to the system reset input. Therefore, if a system reset occurs during the Embedded Program or Erase Algorithm, the device will be automatically reset to read mode and this will enable the system's microprocessor to read the boot-up firmware from the Flash memory.

Byte/Word Configuration

The BYTE pin selects the byte (8-bit) mode or word (16 bit) mode for the Am29F400A device. When this pin is driven high, the device operates in the word (16

bit) mode. The data is read and programmed at DQ0–DQ15. When this pin is driven low, the device operates in byte (8 bit) mode. Under this mode, the DQ15/A-1 pin becomes the lowest address bit and DQ8–DQ14 bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ0–DQ7 and the DQ8–DQ15 bits are ignored. Refer to Figures 14 and 15 for the timing diagram.

Data Protection

The Am29F400A is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, the Am29F400A locks out write cycles for $V_{CC} < V_{LKO}$ (see DC Characteristics section for voltages). When $V_{CC} < V_{LKO}$, the command register is disabled, all internal program/erase circuits are disabled, and the device resets to the read mode. The Am29F400A ignores all writes until $V_{CC} > V_{LKO}$. The user must ensure that the control pins are in the correct logic state when $V_{CC} > V_{LKO}$ to prevent unintentional writes.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on \overline{OE} , \overline{CE} , or \overline{WE} will not initiate a write cycle.

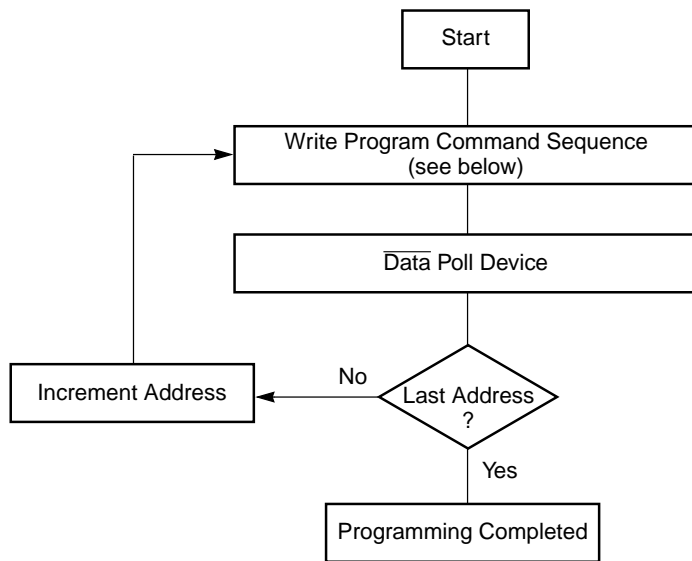
Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle \overline{CE} and \overline{WE} must be a logical zero while \overline{OE} is a logical one.

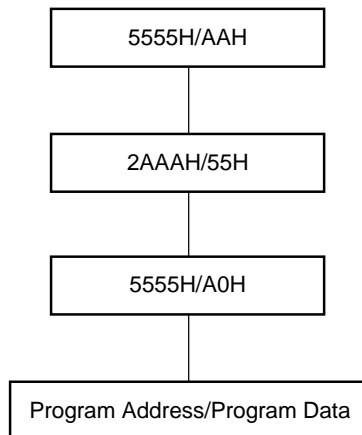
Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of \overline{WE} . The internal state machine is automatically reset to the read mode on power-up.

EMBEDDED ALGORITHMS



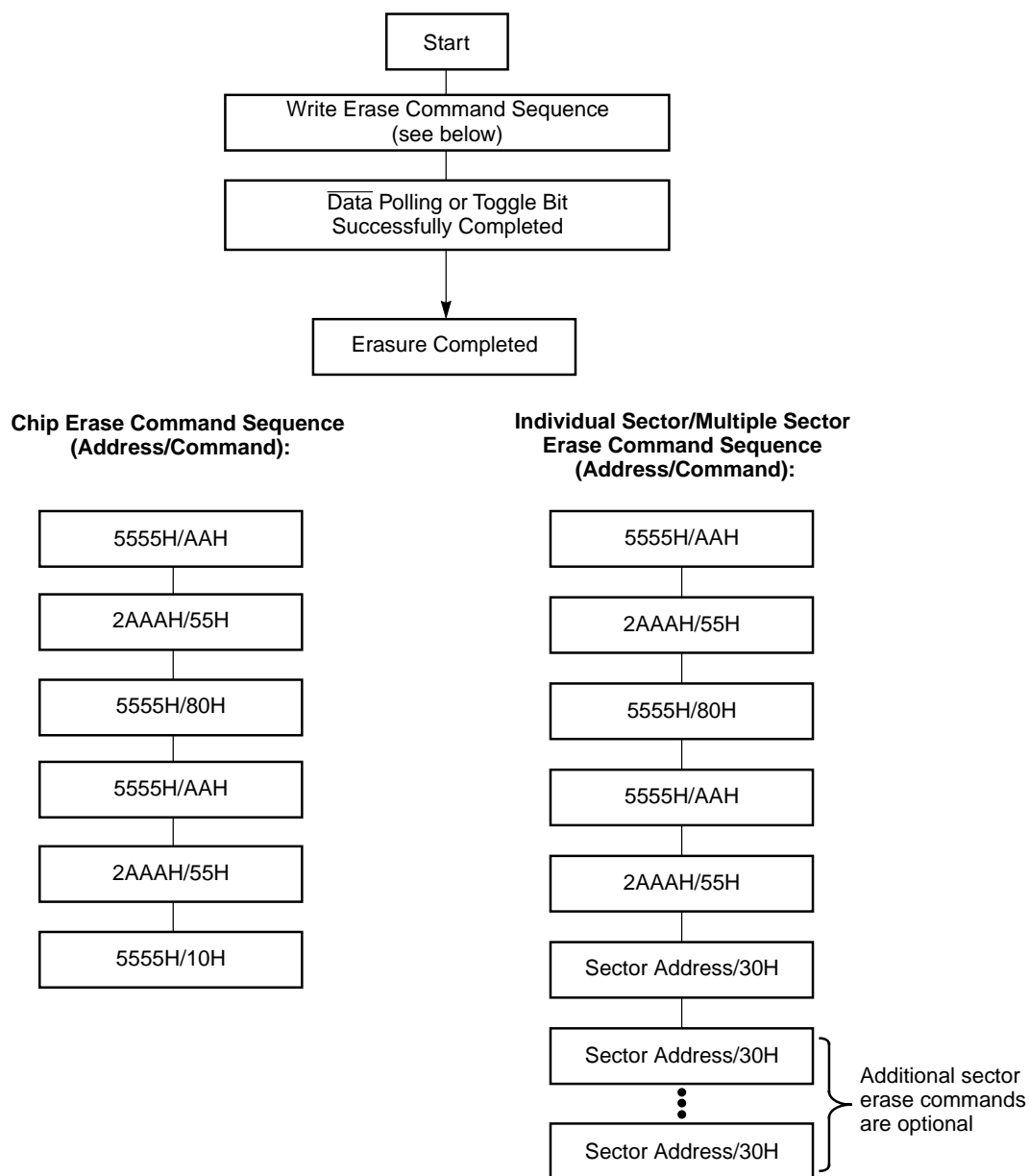
Program Command Sequence (Address/Command):



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Figure 1. Embedded Programming Algorithm

EMBEDDED ALGORITHMS

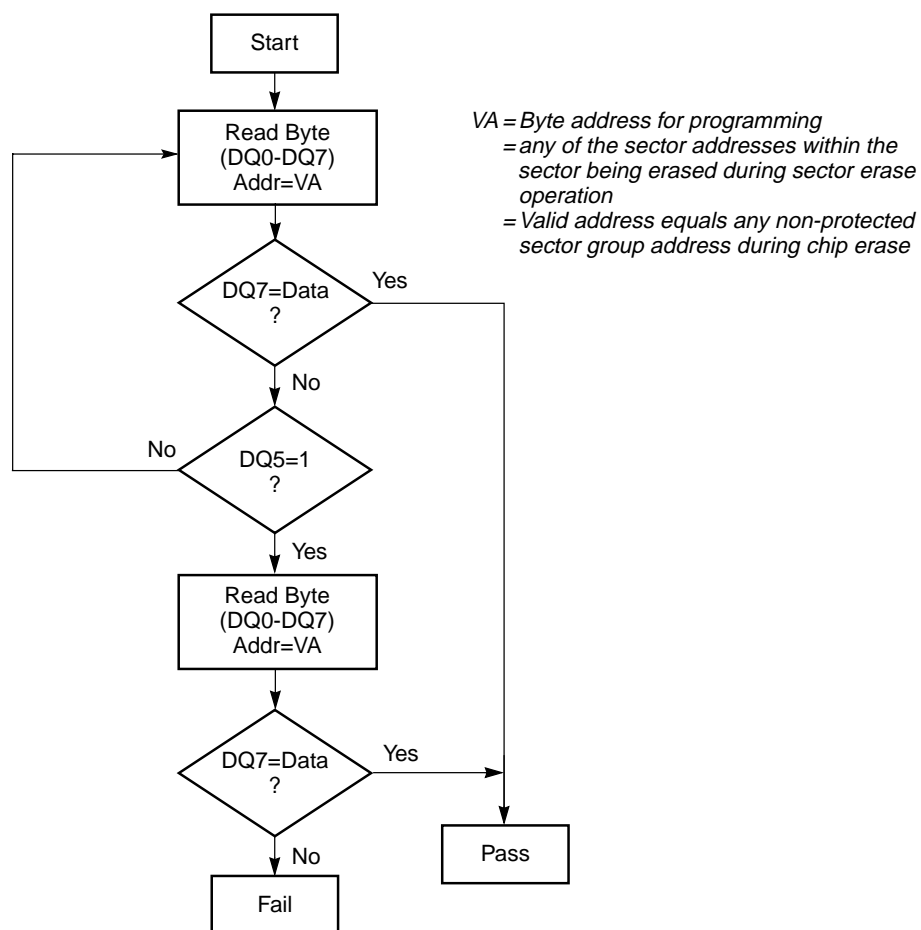


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Note:

To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Figure 2. Embedded Erase Algorithm

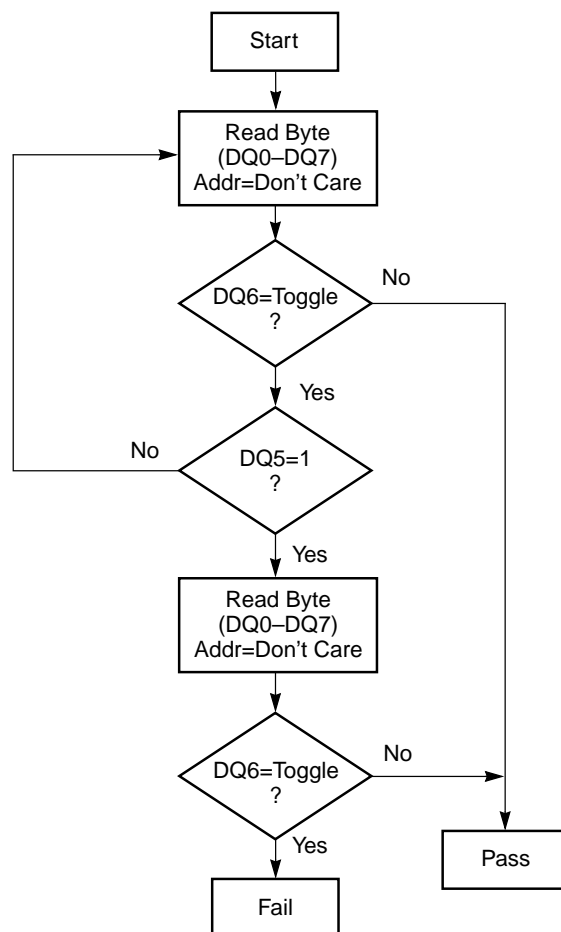


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Note:

DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

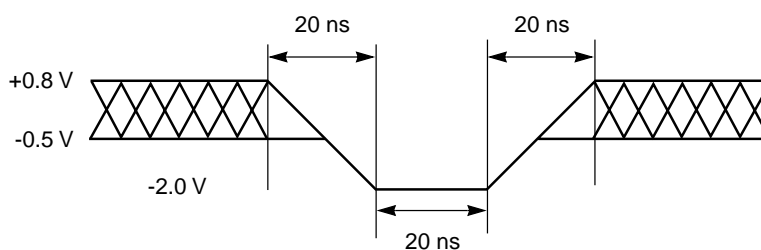
Figure 3. Data Polling Algorithm



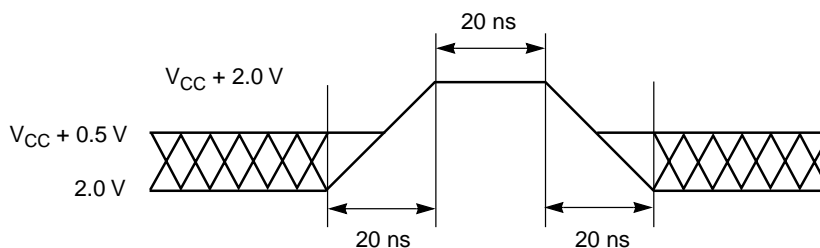
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Note:

DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 4. Toggle Bit Algorithm

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Figure 5. Maximum Negative Overshoot Waveform

20380B-13

Figure 6. Maximum Positive Overshoot Waveform

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
 Plastic Packages -65°C to +125°C
 Ambient Temperature
 with Power Applied. -55°C to +125°C
 Voltage with Respect to Ground
 All pins except A9, \overline{OE} and \overline{RESET}
 (Note 1) -2.0 V to +7.0 V
 V_{CC} (Note 1). -2.0 V to +7.0 V
 A9, \overline{OE} , and \overline{RESET} (Note 2). -2.0 V to +13.0 V
 Output Short Circuit Current (Note 3) 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC} + 0.5$ V. During voltage transitions, input or I/O pins may overshoot to $V_{CC} + 2.0$ V for periods up to 20 ns. See Figure 7 and Figure 8.
2. Minimum DC input voltage on pins A9, \overline{OE} , and \overline{RESET} is -0.5 V. During voltage transitions, A9, \overline{OE} , and \overline{RESET} may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns. See Figure 7 and Figure 8.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A). 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). -40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A). -55°C to +125°C

 V_{CC} Supply Voltages

V_{CC} for Am29F400T/B-65, +4.75 V to +5.25 V

V_{CC} for Am29F400T/B-70, -90,
 -120, -150 +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5.0 V-only Flash

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ Max		± 1.0	μA
I_{LIT}	A9, \overline{OE} , \overline{RESET} Input Load Current	$V_{CC} = V_{CC}$ Max, A9, \overline{OE} , $\overline{RESET} = 12.5$ V		50	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ Max		± 1.0	μA
I_{CC1}	V_{CC} Active Read Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ Byte		40	mA
		Word		50	
I_{CC2}	V_{CC} Active Program/Erase Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		60	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$		1.0	mA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	$V_{CC} + 0.5$	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	$V_{CC} = 5.0$ V	11.5	12.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	2.4		V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2	4.2	V

Notes:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with \overline{OE} at V_{IH} .
2. I_{CC} active while Embedded Program or Erase Algorithm is in progress.
3. Not 100% tested.

DC CHARACTERISTICS (continued)

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ Max			± 1.0	μA
I_{LIT}	A9, \overline{OE} , \overline{RESET} Input Load Current	$V_{CC} = V_{CC}$ Max, A9, \overline{OE} , $\overline{RESET} = 12.5$ V			50	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ Max			± 1.0	μA
I_{CC1}	V_{CC} Active Read Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ Byte		20	40	mA
		Word		28	50	
I_{CC2}	V_{CC} Active Program/Erase Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	50	mA
I_{CC3}	V_{CC} Standby Current (Note 4)	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$		1	5	μA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		$0.7 \times V_{CC}$		$V_{CC} + 0.3$	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	$V_{CC} = 5.0$ V	11.5		12.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output Low Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	$0.85 V_{CC}$			V
V_{OH2}		$I_{OH} = -100$ μA , $V_{CC} = V_{CC}$ Min	$V_{CC} - 0.4$			V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2		4.2	V

Notes:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with \overline{OE} at V_{IH} .
2. I_{CC} active while Embedded Program or Erase Algorithm is in progress.
3. Not 100% tested.
4. $I_{CC3} = 20$ μA max at extended temperatures ($> +85^{\circ}C$).

AC CHARACTERISTICS

Read-Only Operations Characteristics

Parameter Symbols		Description	Test Setup	Speed Option (Notes 1 and 2)					Unit
JEDEC	Standard			-65	-70	-90	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min	60	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$ Max	60	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$ Max	60	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	Max	30	30	35	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 3, 4)	Max	20	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 3, 4)	Max	20	20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, \overline{CE} or \overline{OE} , Whichever Occurs First	Min	0	0	0	0	0	ns
	t_{Ready}	\overline{RESET} Pin Low to Read Mode (Note 4)	Max	20	20	20	20	20	μs
	t_{ELFL} t_{ELFH}	\overline{CE} to \overline{BYTE} Switching Low or High	Max	5	5	5	5	5	ns

Notes:

1. Test Conditions (for -65 only)
Output Load: 1 TTL gate and 30 pF
Input Rise and Fall Times: 5 ns
Input Pulse Levels: 0.0 V to 3.0 V
Timing Measurement Reference Level: 1.5 V input and output
2. Test Conditions (for -70, -90, -120, -150)
Output Load: 1 TTL gate and 100 pF
Input Rise and Fall Times: 20 ns
3. Output Driver Disable Time
4. Not 100% tested.

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level: 0.8 V and 2.0 V input and output

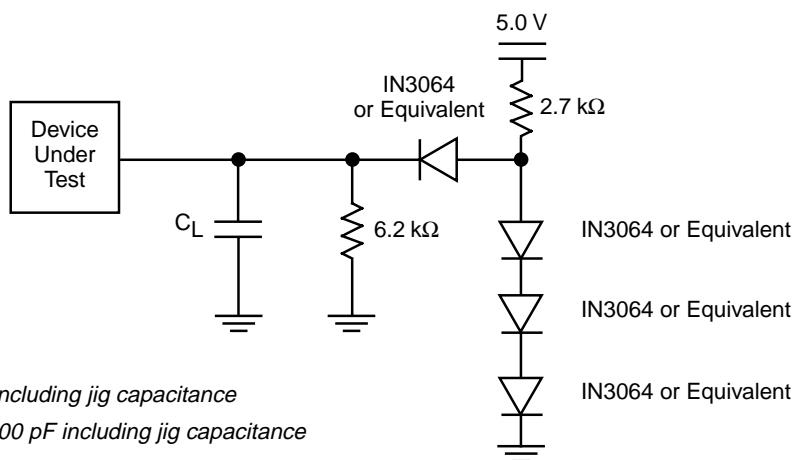
**Notes:**For -65: $C_L = 30$ pF including jig capacitanceFor all others: $C_L = 100$ pF including jig capacitance

Figure 7. Test Conditions

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AC CHARACTERISTICS

Write (Erase/Program) Operations





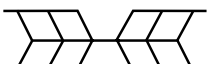
Parameter Symbols		Description		Speed Option (Notes 1 and 2)					Unit
JEDEC	Standard			-65	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	60	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	150	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	30	30	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	0	ns
	t_{OEHL}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	ns
			Toggle and Data Polling (Note 2)	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE High to WE Low)	Min	0	0	0	0	0	ns
t_{ELWL}	t_{CS}	\overline{CE} Setup Time	Min	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	\overline{CE} Hold Time	Min	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	45	50	50	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Byte	Typ	7	7	7	7	μ s
			Word	Typ	14	14	14	14	μ s
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ	1.0	1.0	1.0	1.0	1.0	sec
			Max	8	8	8	8	8	sec
	t_{VCS}	V_{CC} Setup Time (Note 2)	Min	50	50	50	50	50	μ s
	t_{VIDR}	Rise Time to V_{ID} (Notes 2, 3)	Min	500	500	500	500	500	ns
	t_{OESP}	\overline{OE} Setup Time to \overline{WE} Active (Notes 2, 3)	Min	4	4	4	4	4	μ s
	t_{RP}	\overline{RESET} Pulse Width	Min	500	500	500	500	500	ns
	t_{FLQZ}	BYTE Switching Low to Output High Z (Notes 3, 4)	Max	20	20	30	30	30	ns
	t_{BUSY}	Program/Erase Valid to $\overline{RY}/\overline{BY}$ Delay (Note 2)	Min	30	30	35	50	55	ns
	t_{RESSP}	\overline{RESET} Setup Time to \overline{WE} Active	Min	4	4	4	4	4	μ s

Notes:

1. This does not include the preprogramming time.
2. Not 100% tested.
3. These timings are for Temporary Sector Unprotect operation.
4. Output Driver Disable Time.

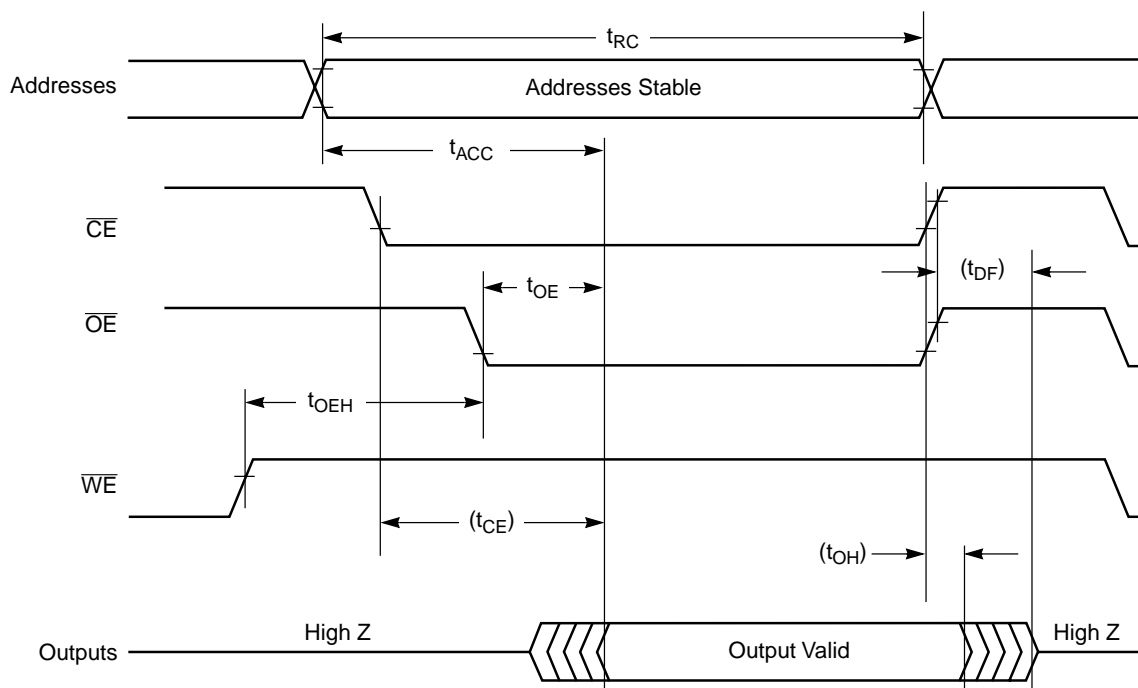
5.0 V-only Flash

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

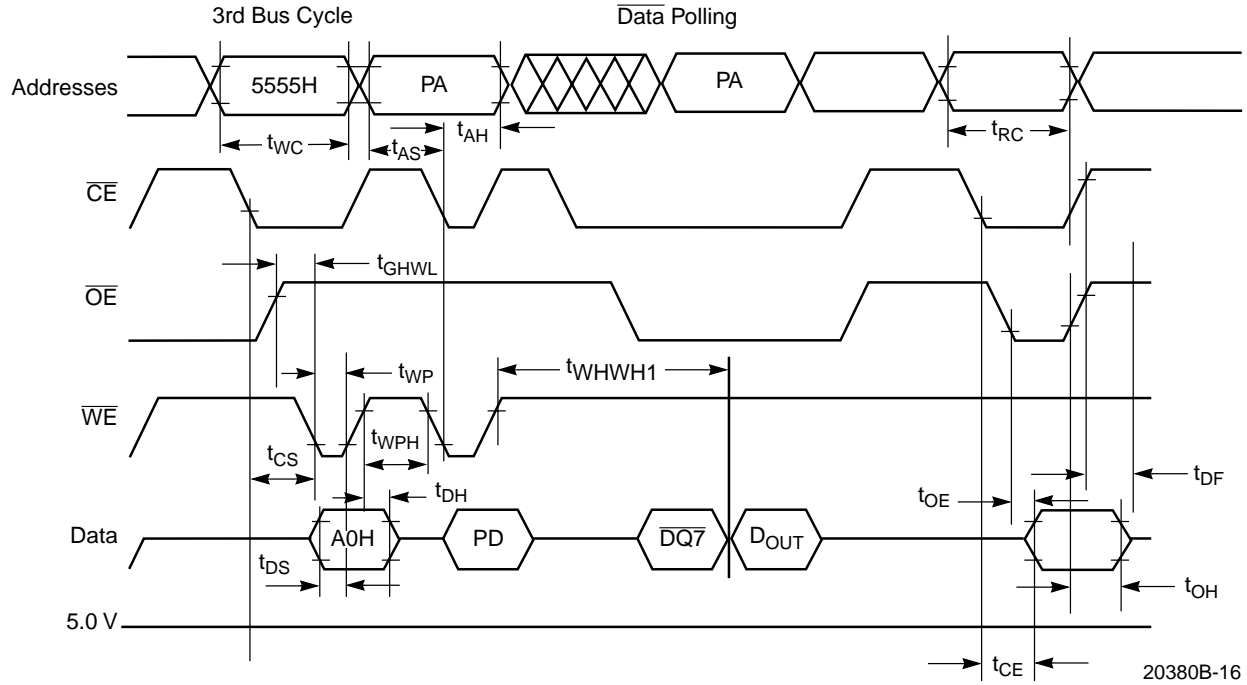
SWITCHING WAVEFORMS



20380B-15

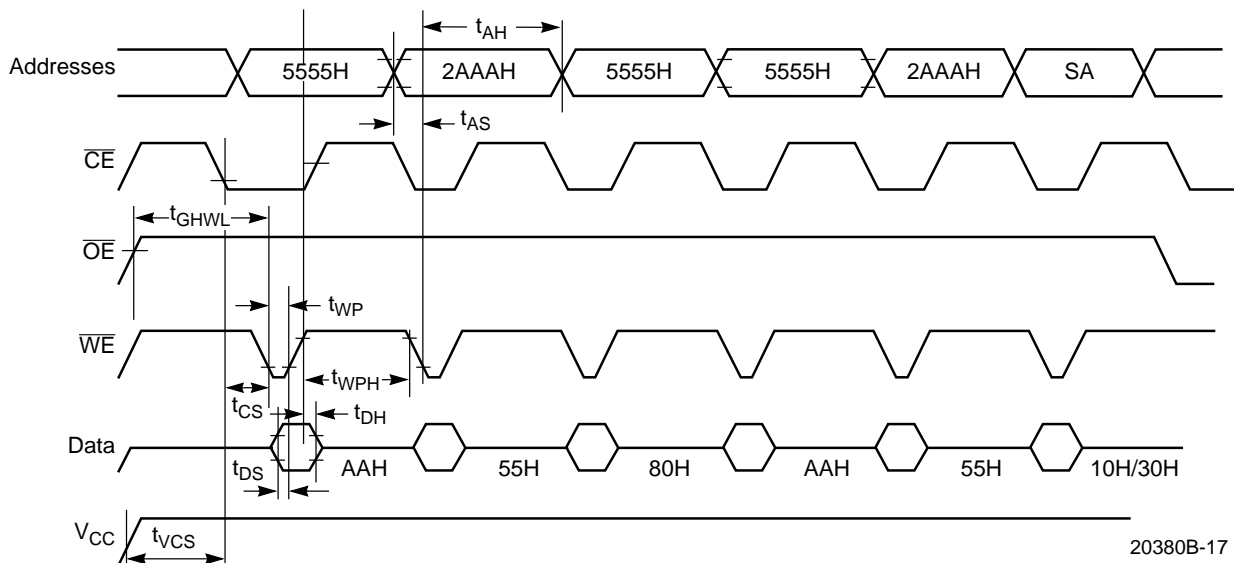
Figure 8. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

**Notes:**

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for the x16 mode.

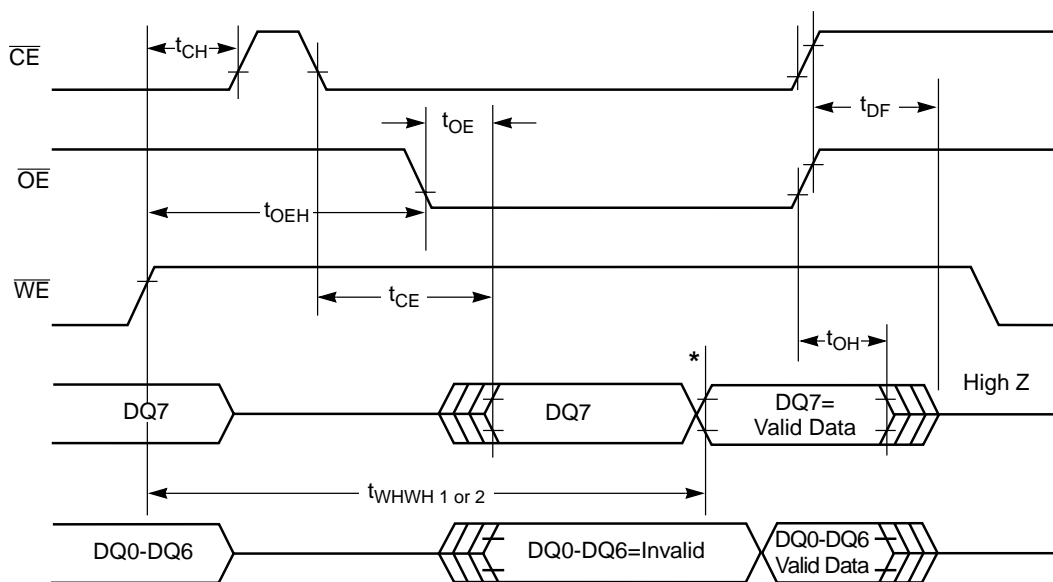
Figure 9. Program Operation Timings

**Notes:**

1. SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.
2. These waveforms are for the x16 mode.

Figure 10. AC Waveforms Chip/Sector Erase Operations

SWITCHING WAVEFORMS

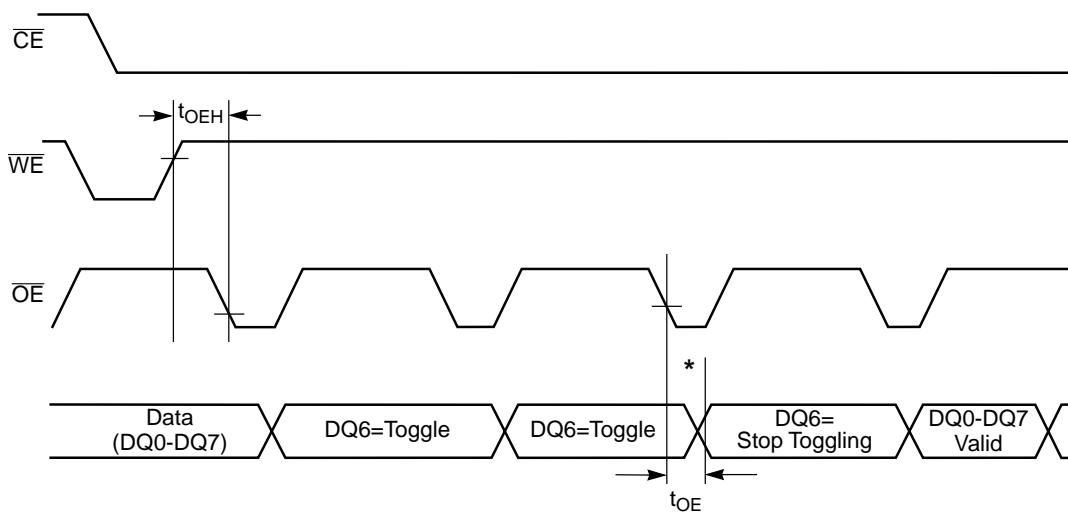


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Note:

*DQ7=Valid Data (The device has completed the Embedded operation).

Figure 11. AC Waveforms for Data Polling During Embedded Algorithm Operations



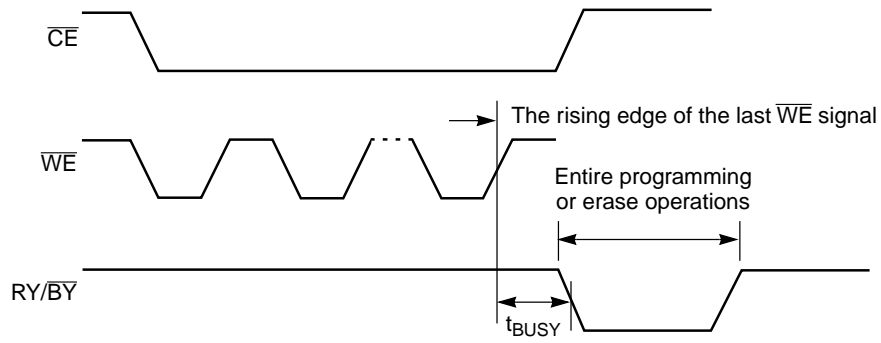
20380B-19

Note:

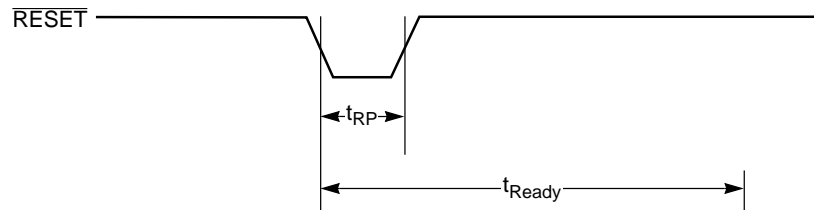
*DQ6 stops toggling (The device has completed the Embedded operation).

Figure 12. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

SWITCHING WAVEFORMS



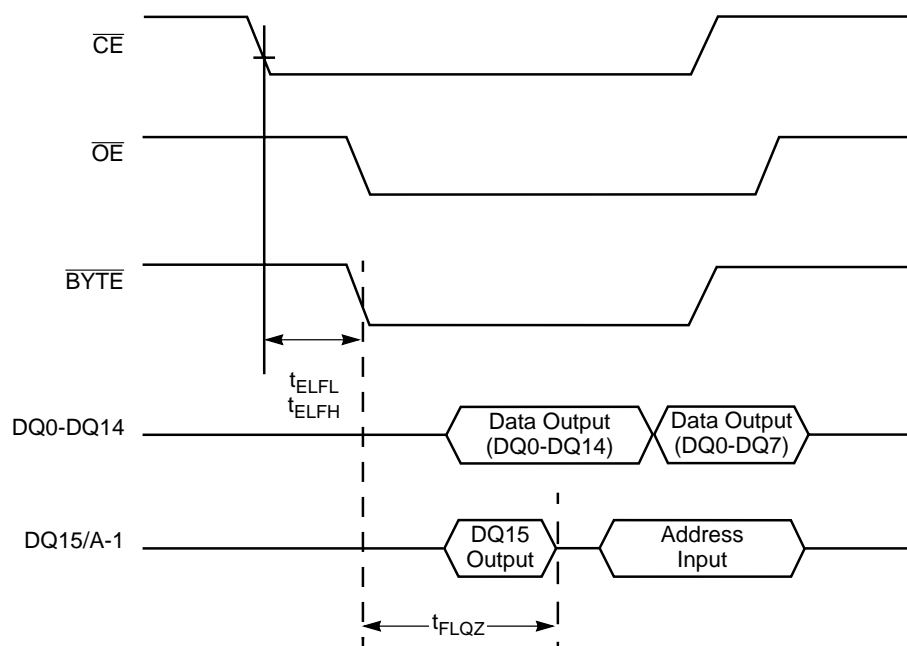
20380B-20

Figure 13. RY/\overline{BY} Timing Diagram During Program/Erase Operations

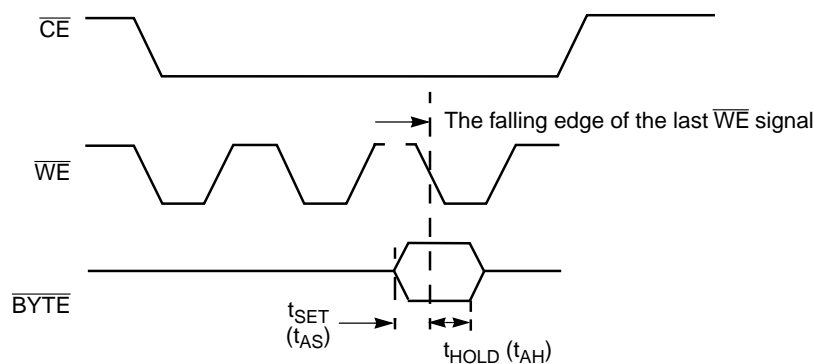
20380B-21

Figure 14. \overline{RESET} Timing Diagram

SWITCHING WAVEFORMS

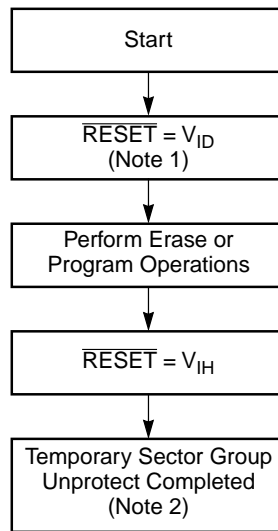


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Figure 15. \overline{BYTE} Timing Diagram for Read Operation

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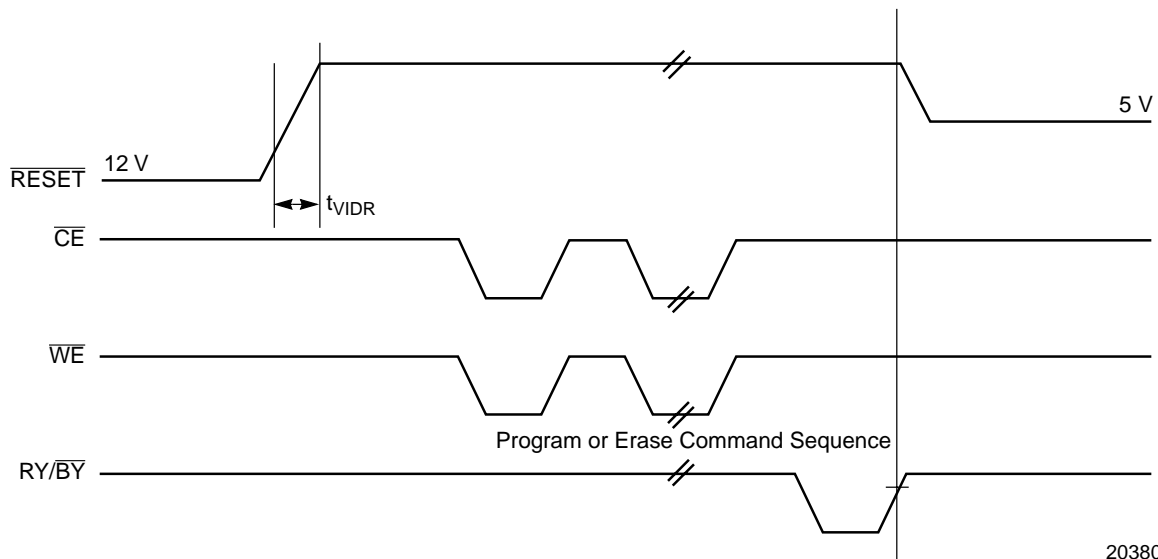
Figure 16. \overline{BYTE} Timing Diagram for Write Operations



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Notes:

1. All protected sectors unprotected.
2. All previously protected sectors are protected once again.

Figure 17. Temporary Sector Unprotect Algorithm

20380B-25

Figure 18. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS

Write/Erase/Program Operations

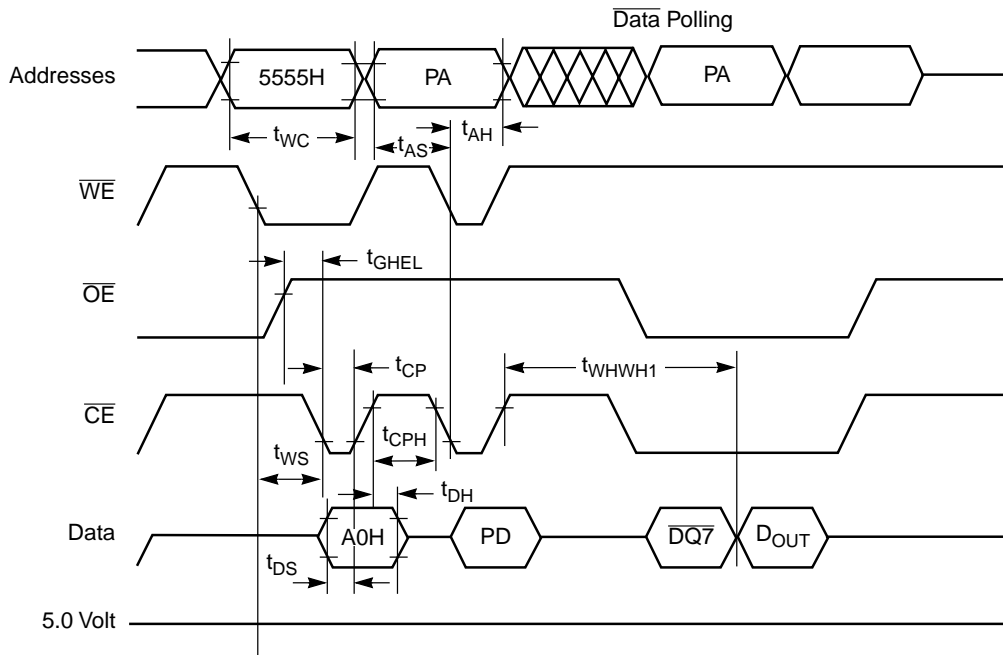
Alternate \overline{CE} Controlled Writes

Parameter Symbols				Speed Option (Notes 1 and 2)					Unit
JEDEC	Standard			-65	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)	Min	60	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	30	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	0	0	0	ns
	t_{OEHL}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	ns
			Toggle and Data Polling (Note 2)	Min	10	10	10	10	ns
t_{GHLEL}	t_{GHLEL}	Read Recover Time Before Write	Min	0	0	0	0	0	ns
t_{WLEL}	t_{WS}	\overline{WE} Setup Time	Min	0	0	0	0	0	ns
t_{EHWL}	t_{WH}	\overline{WE} Hold Time	Min	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	\overline{CE} Pulse Width	Min	35	35	45	50	50	ns
t_{EHEL}	t_{CPH}	\overline{CE} Pulse Width High	Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Byte	Typ	7	7	7	7	μ s
			Word	Typ	14	14	14	14	μ s
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ	1.0	1.0	1.0	1.0	1.0	sec
			Max	8	8	8	8	8	sec
	t_{FLQZ}	BYTE Switching Low to Output High Z (Note 2)	Max	20	20	30	30	30	ns

Notes:

1. This does not include the preprogramming time.
2. Not 100% tested.

SWITCHING WAVEFORMS



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Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for the x16 mode.

Figure 19. Alternate \overline{CE} Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits		Unit	Comments
	Typ (Note 1)	Max		
Sector Erase Time	1.0	8	sec	Excludes 00H programming prior to erasure
Chip Erase Time	11	88	sec	Excludes 00H programming prior to erasure
Byte Programming Time	7	300 (Note 3)	μ s	Excludes system-level overhead (Note 4)
Word Programming Time	14	600	μ s	Excludes system-level overhead (Note 4)
Chip Programming Time	3.6	10.8 (Notes 3, 5)	sec	Excludes system-level overhead (Note 4)

Notes:

1. 25°C, 5.0 V V_{CC} , 100,000 cycles.
2. Although Embedded Algorithms allow for longer chip program and erase time, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.
3. Under worst case condition of 90°C, 4.5 V V_{CC} , 100,000 cycles.
4. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Embedded Erase algorithm, all bytes are programmed to 00H before erasure.
5. The Embedded Algorithms allow for 2.5 ms byte program time. $DQ5 = "1"$ only after a byte takes the theoretical maximum time to program. A minimal number of bytes may require significantly more programming pulses than the typical byte. The majority of the bytes will program within one or two pulses. This is demonstrated by the Typical and Maximum Programming Times listed above.

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all I/O pins	-1.0 V	$V_{CC} + 1.0$ V
V_{CC} Current	-100 mA	+100 mA

Includes all pins except V_{CC} . Test conditions: $V_{CC} = 5.0$ V, one pin at a time.

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	8	10	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz.

SO PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	10	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25^\circ\text{C}$, $f = 1.0$ MHz.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

REVISION SUMMARY**Distinctive Characteristics:**

High Performance: The fastest speed option available is now 60 ns.

Enhanced power management for standby mode: Changed typical standby current to 1 μ A.

General Description:

First paragraph, first sentence should read, "...organized as 512 Kbytes of 8 bits each or 256 Kwords of 16 bits each." Added 60 ns speed option.

Product Selector Guide:

Added -65 column (60 ns, $\pm 5\%$ V_{CC}). Added -70 (70 ns, $\pm 10\%$ V_{CC}) and deleted -75 speed option.

Ordering Information, Standard Products:

The -65 speed option is now listed in the example.

Valid Combinations: Added -65 and -70, and deleted -75 speed options.

Tables 1 and 2, User Bus Operations:

Corrected \overline{WE} for read operations; was don't care (X), is now H.

Standby Mode:

Corrected standby mode current; was 100 μ A, is now 5 μ A.

Table 5, Sector Address Tables (Am29F400AB):

Corrected x16 starting address for SA5; was 1C000h, is now 28000h.

Erase Suspend:

Third paragraph, third sentence: Deleted the word "NOT."

Operating Ranges:

V_{CC} Supply Voltages: Added -65 and deleted -75 speed options in the list. Changed A9 maximum to +13.0 V.

DC Characteristics:

CMOS Compatible: Revised I_{CC} specifications. Added Note 4 (refers to I_{CC3}).

AC Characteristics:

Read Only Operations Characteristics: Added the -65 column and test conditions.

Replaced -75 column with -70 column.

Test Conditions, Figure 7:

Changed speed option in first C_L statement from -75 to -65.

AC Characteristics:

Write/Erase/Program Operations, Alternate CE Controlled Writes: Added the -65 column. Replaced -75 column with -70 column. Revised sector erase and programming specifications.

Erase and Programming Performance:

Revised specifications in table. Clarified table and notes.

Table 7, Command Definitions

Revised Note 5 to cover all upper address bits that are don't care.

Deleted Note 6.