PRELIMINARY

# Am29F200T/Am29F200B

## 2 Megabit (262,144 x 8-Bit/131,072 x 16-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

Advanced Micro Devices

## DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% write and erase, read**
  - — Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  - — Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard word-wide pinouts**
  - — 44-pin SO
  - — 48-pin TSOP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - — 70 ns maximum access time
- **Sector erase architecture**
  - — Three 64 Kbytes, one 32 Kbyte, one 16 Kbyte and two 8 Kbytes
  - — Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase Algorithms**
  - — Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithms**
  - — Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - — 20 mA typical active read current for Byte Mode
  - — 28 mA typical active read current for Word Mode
  - — 30 mA typical write/erase current
  - — 25 µA typical standby current
- **Low $V_{CC}$ write inhibit ≤ 3.2 V**
- **Sector protection**
  - — Hardware method disables any combination of sectors from write or erase operations
- **Erase Suspend/Resume**
  - — Suspends the erase operation to allow a read in another sector within the same device
- **Boot Code Sector Architecture**
  - — T = Top sector
  - — B = Bottom sector

## GENERAL DESCRIPTION

The Am29F200 is a 2 Mbit, 5.0 V-only Flash memory organized as 256K bytes of 8 bits each or 128K words of 16 bits each. The Am29F200 is offered in 44-pin SO and 48-pin TSOP packages. This device is designed to be programmed in-system with the standard system 5.0 V $V_{CC}$ supply. A 12.0 V $V_{PP}$ is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers. The Am29F200 is erased when shipped from the factory.

The standard Am29F200 offers access times between 70 ns and 150 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$) and output enable ($\overline{\text{OE}}$) controls.

The Am29F200 is pin and command set compatible with JEDEC standard 2 Mbit E²PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

## PRODUCT SELECTOR GUIDE

| Family Part No: | Am29F200 | | | |
|---|---|---|---|---|
| Ordering Part No: $V_{CC}$ = 5.0 V ± 5% | -75 | | | |
| $V_{CC}$ = 5.0 V ± 10% | | -90 | -120 | -150 |
| Max Access Time (ns) | 70 | 90 | 120 | 150 |
| $\overline{\text{CE}}$ ($\overline{\text{E}}$) Access (ns) | 70 | 90 | 120 | 150 |
| $\overline{\text{OE}}$ ($\overline{\text{G}}$) Access (ns) | 30 | 35 | 50 | 55 |

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The Am29F200 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire chip or any individual sector is typically erased and verified in 1.5 seconds (if already completely preprogrammed).

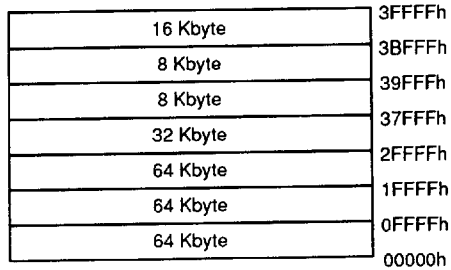
This device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low $V_{CC}$ detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by Data Polling of DQ7, by the Toggle Bit feature on DQ6, or the RY/BY pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

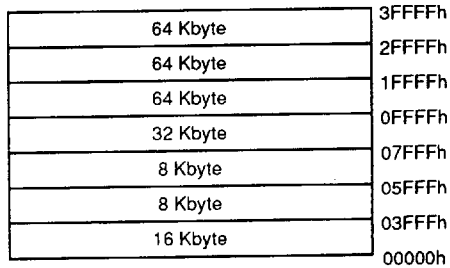
AMD's Flash technology combines years of EPROM and $E^2$PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F200 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

## Flexible Sector-Erase Architecture

- Three 64 Kbytes, one 32 Kbyte, one 16 Kbyte, and two 8 Kbytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user-definable




**Am29F200T Sector Architecture** 18608A-1




**Am29F200B Sector Architecture** 18608A-2



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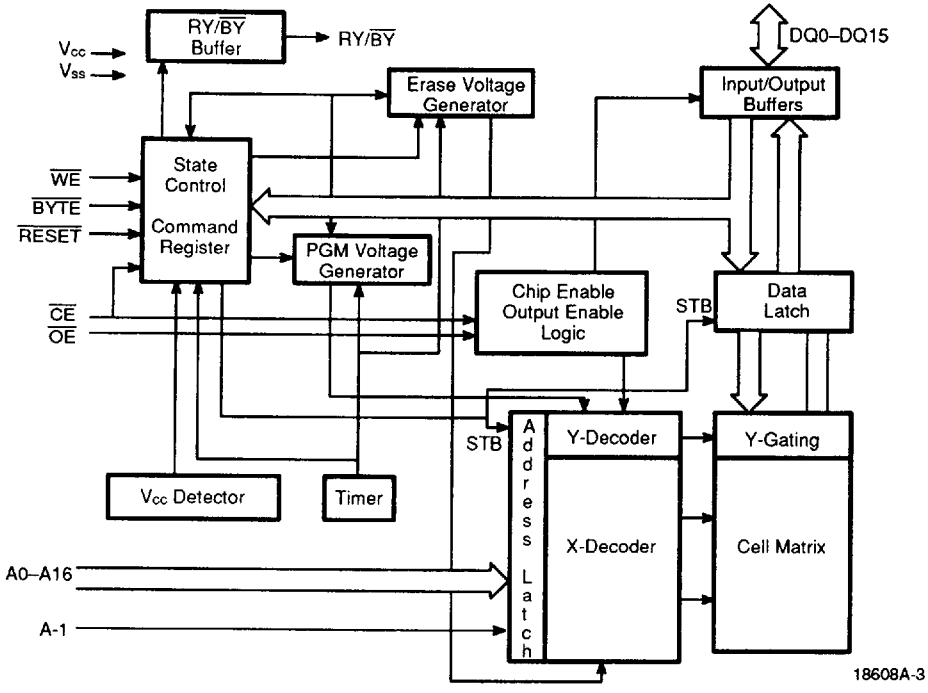
## BLOCK DIAGRAM



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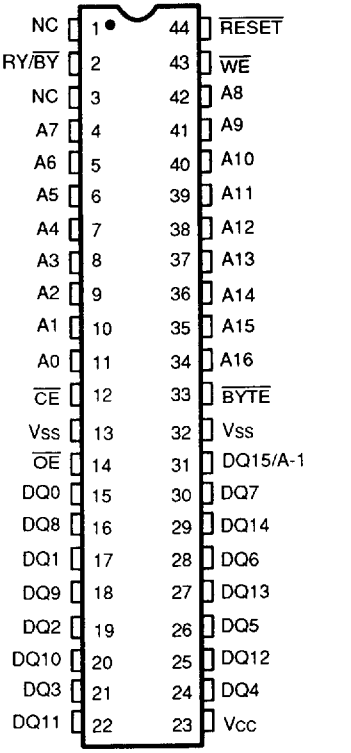
## CONNECTION DIAGRAMS

SO

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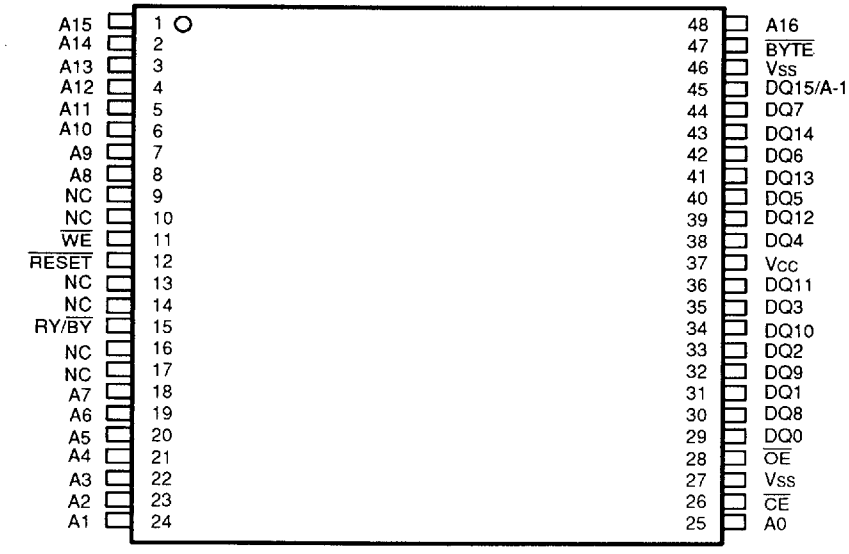
## CONNECTION DIAGRAMS

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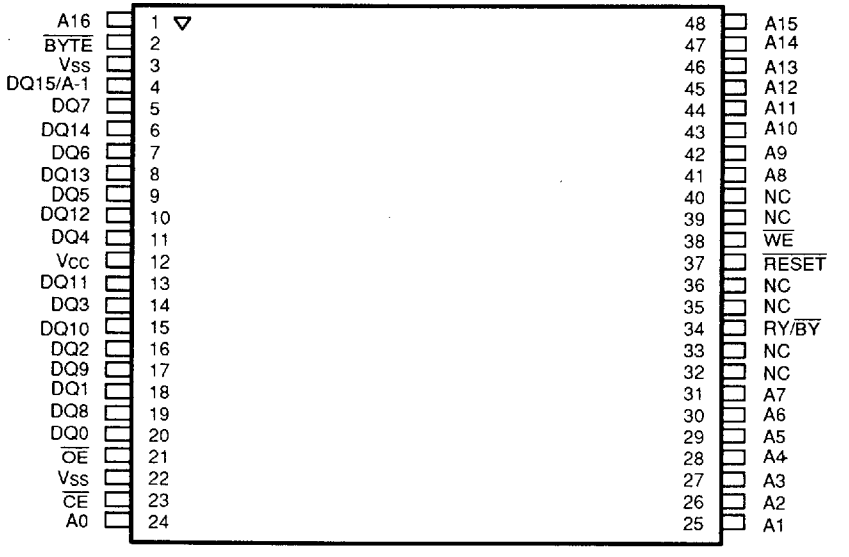
**Standard TSOP**

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**Reverse TSOP**



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## LOGIC SYMBOL

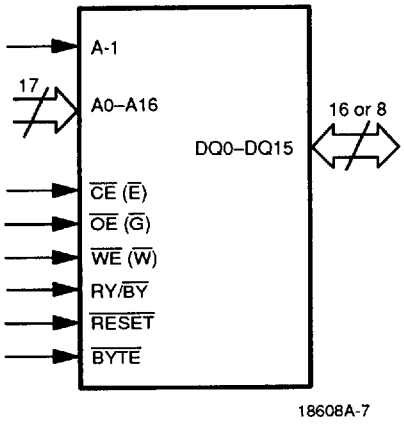


**Table 1. Am29F200 Pin Configuration**

| Pin | Function |
|---|---|
| A-1, A0–A16 | Address Inputs |
| DQ0–DQ15 | Data Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| RY/$\overline{BY}$ | Ready-Busy Input |
| $\overline{RESET}$ | Hardware Reset Pin/Sector Protect Unlock |
| $\overline{BYTE}$ | Selects 8-bit or 16-bit mode |
| NC | No Internal Connection |
| $V_{SS}$ | Device Ground |
| $V_{CC}$ | Device Power Supply (5.0 V ± 10% or ± 5%) |



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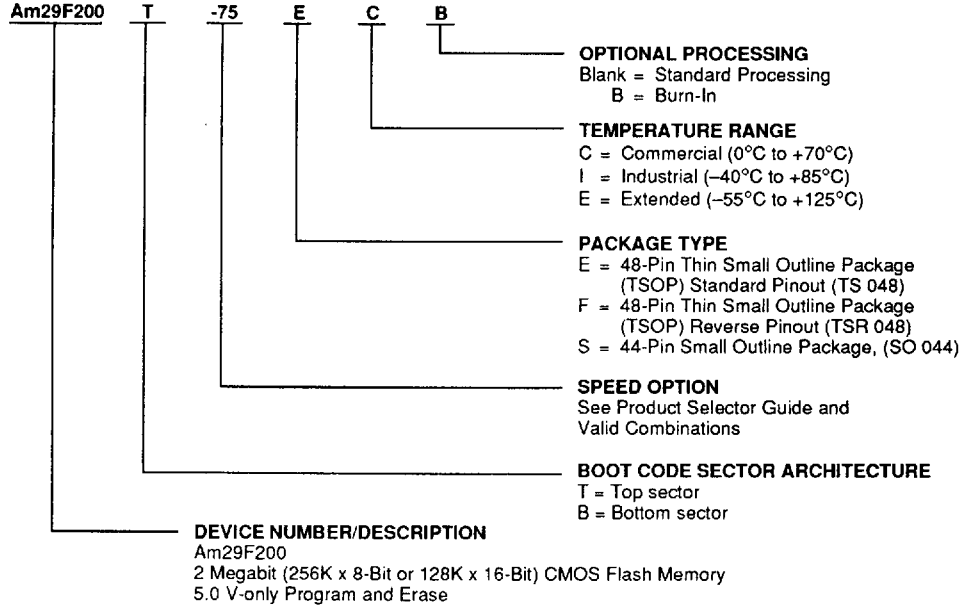
## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | |
|---|---|
| Am29F200T/B-75 | EC, FC, SC |
| Am29F200T/B-90 | EC, EI, FC, FI, EE, EEB, FE, FEB, SC, SI, SE, SEB |
| Am29F200T/B-120 | |
| Am29F200T/B-150 | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.



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**Table 2. Am29F200 User Bus Operations ($\overline{BYTE}$ = $V_{IH}$)**

| Operation | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | A0 | A1 | A6 | A9 | DQ0–DQ15 | $\overline{RESET}$ |
|---|---|---|---|---|---|---|---|---|---|
| Auto-Select Manufacturer Code (1) | L | L | H | L | L | L | $V_{ID}$ | Code | H |
| Auto-Select Device Code (1) | L | L | H | H | L | L | $V_{ID}$ | Code | H |
| Read (3) | L | L | H | A0 | A1 | A6 | A9 | $D_{OUT}$ | H |
| Standby | H | X | X | X | X | X | X | HIGH Z | H |
| Output Disable | L | H | H | X | X | X | X | HIGH Z | X |
| Write | L | H | L | A0 | A1 | A6 | A9 | $D_{IN}$ | H |
| Enable Sector Protect | L | $V_{ID}$ | L | X | X | X | $V_{ID}$ | X | H |
| Verify Sector Protect (2) | L | L | H | L | H | L | $V_{ID}$ | Code | H |
| Temporary Sector Unprotect | X | X | X | X | X | X | X | X | $V_{ID}$ |
| Reset (Hardware) | X | X | X | X | X | X | X | HIGH Z | L |

**Table 3. Am29F200 User Bus Operations ($\overline{BYTE}$ = $V_{IL}$)**

| Operation | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | A0 | A1 | A6 | A9 | DQ0–DQ7 | $\overline{RESET}$ |
|---|---|---|---|---|---|---|---|---|---|
| Auto-Select Manufacturer Code (1) | L | L | H | L | L | L | $V_{ID}$ | Code | H |
| Auto-Select Device Code (1) | L | L | H | H | L | L | $V_{ID}$ | Code | H |
| Read (3) | L | L | H | A0 | A1 | A6 | A9 | $D_{OUT}$ | H |
| Standby | H | X | X | X | X | X | X | HIGH Z | H |
| Output Disable | L | H | H | X | X | X | X | HIGH Z | X |
| Write | L | H | L | A0 | A1 | A6 | A9 | $D_{IN}$ | H |
| Enable Sector Protect | L | $V_{ID}$ | L | X | X | X | $V_{ID}$ | X | H |
| Verify Sector Protect (2) | L | L | H | L | H | L | $V_{ID}$ | Code | H |
| Temporary Sector Unprotect | X | X | X | X | X | X | X | X | $V_{ID}$ |
| Reset (Hardware) | X | X | X | X | X | X | X | HIGH Z | L |

***Legend:***

*L = $V_{IL}$, H = $V_{IH}$, X = Don't Care. See DC Characteristics for voltage levels.*

***Notes:***

1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 7.*
2. *Refer to the section on Sector Protection.*
3. *$\overline{WE}$ can be $V_{IL}$ if $\overline{OE}$ is $V_{IL}$, $\overline{OE}$ at $V_{IH}$ initiates the write operations.*

## Read Mode

The Am29F200 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time ($t_{ACC}$) is equal to the delay from stable addresses to valid output data. The chip enable access time ($t_{CE}$) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC}$–$t_{OE}$ time).



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## Standby Mode

The Am29F200 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc ± 0.5 V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at $V_{IH}$) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

## Output Disable

With the $\overline{OE}$ input at a logic high level ($V_{IH}$), output from the device is disabled. This will cause the output pins to be in a high impedance state.

## Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force $V_{ID}$ (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from $V_{IL}$ to $V_{IH}$. All addresses are don't cares except A0, A1, and A6.

The manufacturer and device codes may also be read via the command register, for instances when the Am29F200 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 7 (refer to Autoselect Command section).

Byte 0 (A0 = $V_{IL}$) represents the manufacturer's code (AMD=01H) and byte 1 (A0 = $V_{IH}$) the device identifier code (Am29F200T = 51H and Am29F200B = 52H for x8 mode; Am29F200T = 2251H and Am29F200B = 2252H for x16 mode). These two bytes/words are given in the table below. All identifiers for manufacturer and device will exhibit odd parity with the DQ7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be $V_{IL}$ (see Tables 4.1 and 4.2).

**Table 4.1 Am29F200 Sector Protection Verify Autoselect Codes**

| Type | | | A12–A16 | A6 | A1 | A0 | Code (HEX) |
|---|---|---|---|---|---|---|---|
| Manufacturer's Code | | | X | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | 01H |
| Am29F200 Device Code | Am29F200T | Byte | X | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 51H |
| | | Word | | | | | 2251H |
| | Am29F200B | Byte | X | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 52H |
| | | Word | | | | | 2252H |
| Sector Protection | | | Sector Addresses | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | 01H* |

**Outputs 01H at protected sector addresses*

**Table 4.2 Expanded Autoselect Code Table**

| Type | | Code | DQ 15 | DQ 14 | DQ 13 | DQ 12 | DQ 11 | DQ 10 | DQ 9 | DQ 8 | DQ 7 | DQ 6 | DQ 5 | DQ 4 | DQ 3 | DQ 2 | DQ 1 | DQ 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer's Code | | 01H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Am29F200 Device Code | Am29F200T(B) | 51H | A–1 | HI–Z | HI–Z | HI–Z | HI–Z | HI–Z | HI–Z | HI–Z | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| | (W) | 2251H | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| | Am29F200B(B) | 52H | A–1 | HI–Z | HI–Z | HI–Z | HI–Z | HI–Z | HI–Z | HI–Z | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| | (W) | 2252H | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| Sector Protection | | 01H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

*(B) – Byte mode*

*(W) – Word mode*



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Table 5. Sector Address Tables (Am29F200T)

| | A16 | A15 | A14 | A13 | A12 | Address Range |
|---|---|---|---|---|---|---|
| SA0 | 0 | 0 | X | X | X | 00000h–0FFFFh |
| SA1 | 0 | 1 | X | X | X | 10000h–1FFFFh |
| SA2 | 1 | 0 | X | X | X | 20000h–2FFFFh |
| SA3 | 1 | 1 | 0 | X | X | 30000h–37FFFh |
| SA4 | 1 | 1 | 1 | 0 | 0 | 38000h–39FFFh |
| SA5 | 1 | 1 | 1 | 0 | 1 | 3A000h–3BFFFh |
| SA6 | 1 | 1 | 1 | 1 | X | 3C000h–3FFFFh |

Table 6. Sector Address Tables (Am29F200B)

| | A16 | A15 | A14 | A13 | A12 | Address Range |
|---|---|---|---|---|---|---|
| SA0 | 0 | 0 | 0 | 0 | X | 00000h–03FFFh |
| SA1 | 0 | 0 | 0 | 1 | 0 | 04000h–05FFFh |
| SA2 | 0 | 0 | 0 | 1 | 1 | 06000h–07FFFh |
| SA3 | 0 | 0 | 1 | X | X | 08000h–0FFFFh |
| SA4 | 0 | 1 | X | X | X | 10000h–1FFFFh |
| SA5 | 1 | 0 | X | X | X | 20000h–2FFFFh |
| SA6 | 1 | 1 | X | X | X | 30000h–3FFFFh |

## Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written to by bringing $\overline{WE}$ to $V_{IL}$, while $\overline{CE}$ is at $V_{IL}$ and $\overline{OE}$ is at $V_{IH}$. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

## Sector Protection

The Am29F200 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 6). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (AMD's ExpressFlash™ Service).

To activate this mode, the programming equipment must force $V_{ID}$ on address pin A9 and control pin $\overline{OE}$, (suggest $V_{ID}$ = 11.5 V) and $\overline{CE}$ = $V_{IL}$. The sector addresses (A16, A15, A14, A13, and A12) should be set to the sector to be protected. Tables 5 and 6 define the sector address for each of the seven (7) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. Refer to figures 17 and 18 for sector protect algorithm and waveforms.

To verify programming of the protection circuitry, the programming equipment must force $V_{ID}$ on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at $V_{IL}$ and $\overline{WE}$ at $V_{IH}$. Scanning the sector addresses (A16, A15, A14, A13, and A12) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" code at device output DQ0 for a protected sector. Otherwise the device will produce 00H for an unprotected sector. In this mode, the lower order addresses, except for A0, A1, and A6 are don't care. Address locations with A1 = $V_{IL}$ are reserved for Autoselect manufacturer and device codes.



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It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A16, A15, A14, A13, and A12) are the sector address will produce a logical "1" at DQ0 for a protected sector. See Tables 4.1 and 4.2 for Autoselect codes.

## Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors of the Am29F200 device in order to change data. The Sector Unprotect mode is activated by setting the $\overline{\text{RESET}}$ pin to high voltage (12V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the 12V is taken away from the $\overline{\text{RESET}}$ pin, all the previously protected sectors will be protected again.

## Sector Unprotect

The Am29F200 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force $V_{ID}$ on control pin $\overline{\text{OE}}$ and address pin A9. The $\overline{\text{CE}}$ and A0 pins must be set at $V_{IL}$. Pins A6 and A1 must be set to $V_{IH}$. Refer to Figure 19 for the sector unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{\text{WE}}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at $V_{IL}$. Performing a read operation at address location XXX2H, where the higher order addresses (A16, A15, A14, A13, and A12) define a particular sector address, will produce 00H at data outputs (DQ0–DQ7) for an unprotected sector.

## Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. **Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode**. Table 7 defines the valid register command sequences. Note that the Erase Suspend (B0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable). Please note that commands are always written at DQ0–DQ7 and DQ8–DQ15 bits are ignored.

**Table 7. Am29F200 Command Definitions**

| Command Sequence Read/Reset | | Bus Write Cycles Req'd | First Bus Write Cycle | | Second Bus Write Cycle | | Third Bus Write Cycle | | Fourth Bus Read/Write Cycle | | Fifth Bus Write Cycle | | Sixth Bus Write Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read/Reset | | 1 | XXXH | F0H | | | | | | | | | | |
| Read/Reset | Word | 4 | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | RA | RD | | | | |
| | Byte | | AAAAH | | 5555H | | AAAAH | | | | | | | |
| Autoselect | Word | 4 | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | | | | | | |
| | Byte | | AAAAH | | 5555H | | AAAAH | | | | | | | |
| Program | Word | 4 | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | PA | Data | | | | |
| | Byte | | AAAAH | | 5555H | | AAAAH | | | | | | | |
| Chip Erase | Word | 6 | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| | Byte | | AAAAH | | 5555H | | AAAAH | | AAAAH | | 5555H | | AAAAH | |
| Sector Erase | Word | 6 | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | SA | 30H |
| | Byte | | AAAAH | | 5555H | | AAAAH | | AAAAH | | 5555H | | | |
| Sector Erase Suspend | | | Erase can be suspended during sector erase with Addr (don't care), Data (B0H) | | | | | | | | | | | |
| Sector Erase Resume | | | Erase can be resumed after suspend with Addr (don't care), Data (30H) | | | | | | | | | | | |

***Notes:***

1. *Address bit A15 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA) Write Sequences may be initiated with A15 in either state.*
2. *Address bits A16 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).*
3. *Bus operations are defined in Table 2.*
4. *RA = Address of the memory location to be read.*
   *PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{\text{WE}}$ pulse.*
   *SA = Address of the sector to be erased. The combination of A16, A15, A14, A13, and A12 will uniquely select any sector.*
5. *RD = Data read from location RA during read operation.*
   *PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{\text{WE}}$.*
6. *The system should generate the following address patterns:*
   *Word Mode: 5555H or 2AAAH to addresses A0 – A14*
   *Byte Mode: AAAAH or 5555H to addresses A-1 – A14.*



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## Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

## Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code (Am29F200T = 51H and Am29F200B = 52H for x8 mode; Am29F200T = 2251H and Am29F200B = 2252H for x16 mode) (see Tables 4.1 and 4.2).

All manufacturer and device codes will exhibit odd parity with DQ7 defined as the parity bit.

Scanning the sector addresses (A16, A15, A14, A13, and A12) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

## Byte/Word Programming

The device is programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

## Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

## Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (30H) is latched on the rising edge of $\overline{WE}$. A time-out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs, otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be



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re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun will corrupt the data in that sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 6).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 80 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to the read mode. $\overline{Data}$ Polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

## Erase Suspend

Erase Suspend command allows the user to interrupt the chip and then perform data reads (not program) from a non-busy sector during a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the Chip Erase or Programming operation. The Erase Suspend command (B0H) which is allowed only during the Sector Erase Operation includes the sector erase time-out period after the Sector Erase commands (30H). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be ignored as such, but instead will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are don't-cares when writing the erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 µs to 15 µs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit (DQ6) to determine if the chip has entered the pseudo-read mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter intermittent problems. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command, the user must wait until the toggle bit stops toggling before data reads from the device can be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal (pulse) counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the DQ5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

## Write Operation Status

**Table 8. Hardware Sequence Flags**

| | Status | DQ7 | DQ6 | DQ5 | DQ3 | DQ2–DQ0 |
|---|---|---|---|---|---|---|
| In Progress | Auto-Programming | $\overline{DQ7}$ | Toggle | 0 | 0 | ($\overline{D}$) (Note 1) |
| | Program/Erase in Auto Erase | 0 | Toggle | 0 | 1 | |
| Exceeded Time Limits | Auto-Programming | $\overline{DQ7}$ | Toggle | 1 | 1 | ($\overline{D}$) (Note 1) |
| | Program/Erase in Auto-Erase | 0 | Toggle | 1 | 1 | |

***Notes:***

1. *DQ0, DQ1, and DQ2 are reserve pins for future use.*
2. *DQ8–DQ15 = Don't Care for x16 mode.*
3. *DQ4 for AMD internal use only.*



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### DQ7
### Data Polling

The Am29F200 device features Data Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for Data Polling (DQ7) is shown in Figure 3.

For chip erase, the Data Polling is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For sector erase, the Data Polling is valid after the last rising edge of the sector erase WE pulse. Data Polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the Am29F200 data pins (DQ7) may change asynchronously while the output enable (OE) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 8).

See Figure 11 for the Data Polling timing specifications and diagrams.

### DQ6
### Toggle Bit

The Am29F200 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (OE toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth WE pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase WE pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either CE or OE toggling will cause the DQ6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ6 to toggle.

See Figure 12 for the Toggle Bit timing specifications and diagrams.

### DQ5
### Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The CE circuit will partially power down the device under these conditions (to approximately 2 mA). The OE and WE pins will control the output disable functions as described in Table 2.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used.

### DQ3
### Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. Data Polling



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and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 8: Hardware Sequence Flags.

**RY/$\overline{\text{BY}}$**
**Ready/Busy**

The Am29F200 provides a RY/$\overline{\text{BY}}$ output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/$\overline{\text{BY}}$ pin is low, the device will not accept any additional program or erase commands. If the Am29F200 is placed in an Erase Suspend mode, the RY/$\overline{\text{BY}}$ output will be high. Also, since this is an open drain output, many RY/$\overline{\text{BY}}$ pins can be tied together in parallel with a pull up resistor to $V_{CC}$.

During programming, the RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the fourth $\overline{\text{WE}}$ pulse. During an erase operation, the RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the sixth $\overline{\text{WE}}$ pulse. The RY/$\overline{\text{BY}}$ pin should be ignored while RESET is at $V_{IL}$. Refer to Figure 13 for a detailed timing diagram.

**$\overline{\text{RESET}}$**
**Hardware Reset**

The Am29F200 device may be reset by driving the $\overline{\text{RESET}}$ pin to $V_{IL}$. The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low ($V_{IL}$) for at least 500 ns in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset 20 µs after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the device requires an additional 50 ns before it will allow read access. When the $\overline{\text{RESET}}$ pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{\text{BY}}$ output signal should be ignored during the $\overline{\text{RESET}}$ pulse. Refer to Figure 14 for the timing diagram.

## Byte/Word Configuration

The $\overline{\text{BYTE}}$ pin selects the byte (8-bit) mode or word (16 bit) mode for the Am29F200 device. When this pin is driven high, the device operates in the word (16 bit) mode. The data is read and programmed at DQ0–DQ15. When this pin is driven low, the device operates in byte (8 bit) mode. Under this mode, the DQ15/A-1 pin becomes the lowest address bit and DQ8–DQ14 bits are tristated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ0–DQ7 and the DQ8–DQ15 bits are ignored. Refer to Figures 15 and 16 for the timing diagram.

## Data Protection

The Am29F200 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form $V_{CC}$ power-up and power-down transitions or system noise.

## Low $V_{CC}$ Write Inhibit

To avoid initiation of a write cycle during $V_{CC}$ power-up and power-down, a write cycle is locked out for $V_{CC}$ less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the $V_{CC}$ level is greater than $V_{LKO}$. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when $V_{CC}$ is above 3.2 V.

## Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will not initiate a write cycle.

## Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IH}$. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

## Power-Up Write Inhibit

Power-up of the device with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to the read mode on power-up.



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## EMBEDDED ALGORITHMS

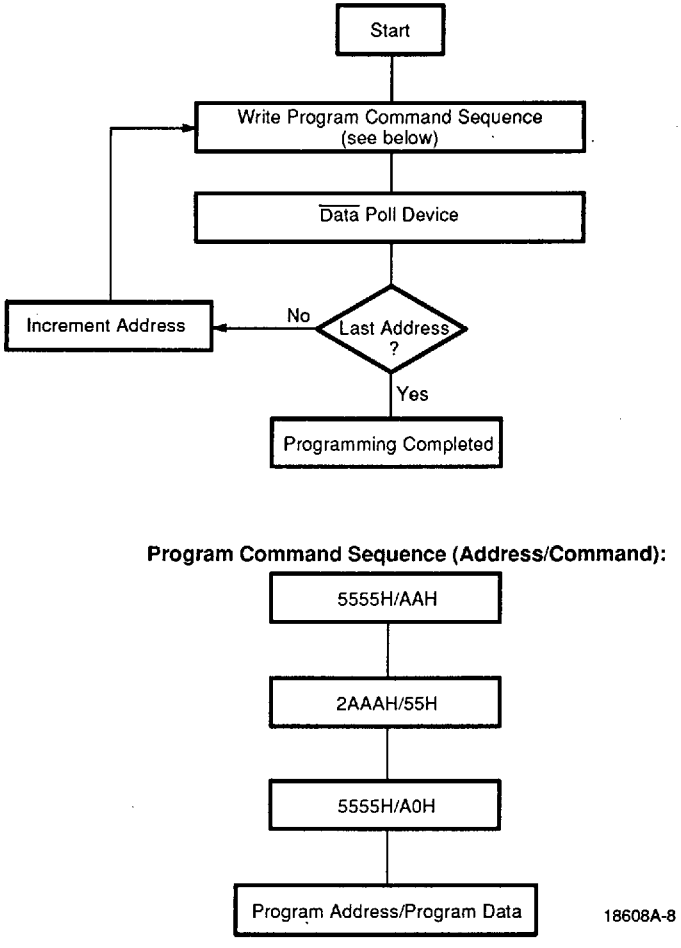


**Figure 1. Embedded Programming Algorithm**

**Table 9. Embedded Programming Algorithm**

| Bus Operations | Command Sequence | Comments |
|---|---|---|
| Standby (Note 1) | | |
| Write | Program | Valid Address/Data Sequence |
| Read | | Data Polling to Verify Programming |
| Standby (Note 1) | | Compare Data Output to Data Expected |

***Note:***

*1. Device is either powered-down, erase inhibit or program inhibit.*



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## EMBEDDED ALGORITHMS

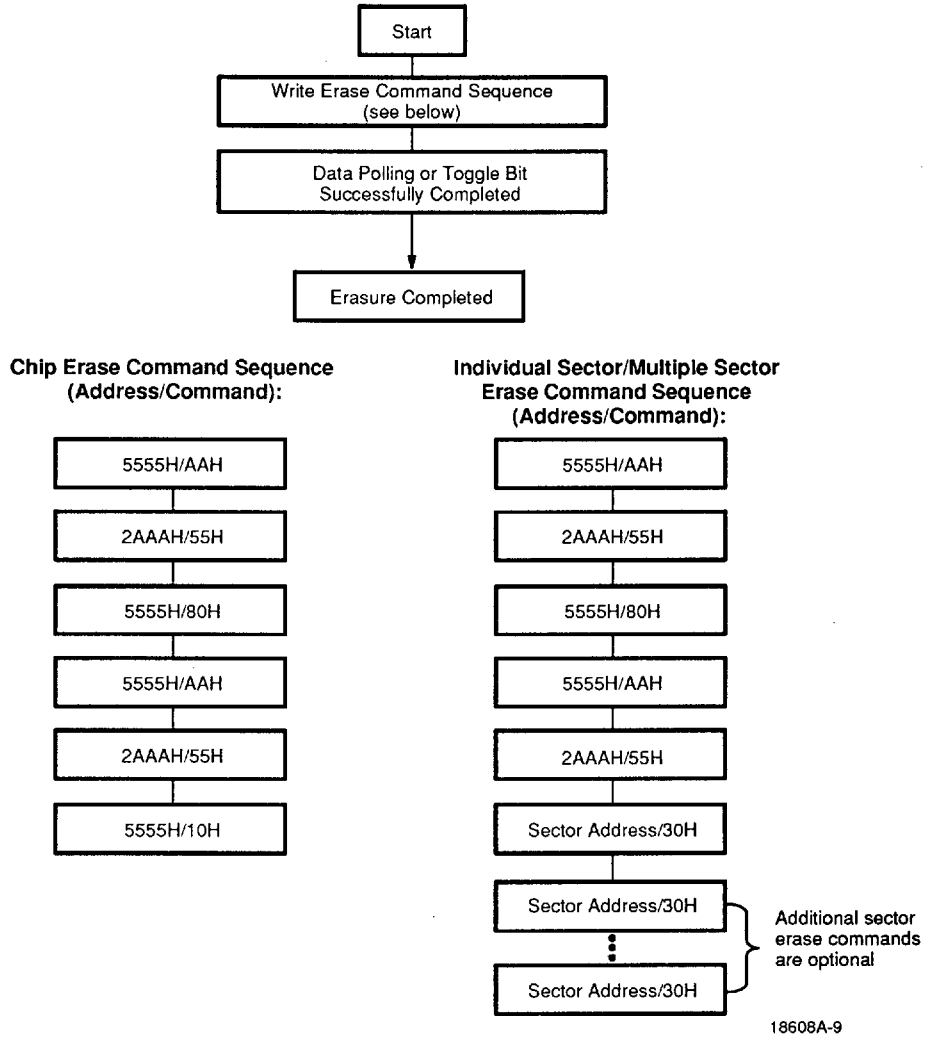


Figure 2. Embedded Erase Algorithm

Table 10. Embedded Erase Algorithm

| Bus Operations | Command Sequence | Comments |
|---|---|---|
| Standby (Note 1) | | |
| Write | Erase | |
| Read | | $\overline{\text{Data}}$ Polling to Verify Erasure |
| Standby (Note 1) | | Compare Output to FFH |

***Note:***

*1. Device is either powered-down, erase inhibit or program inhibit.*



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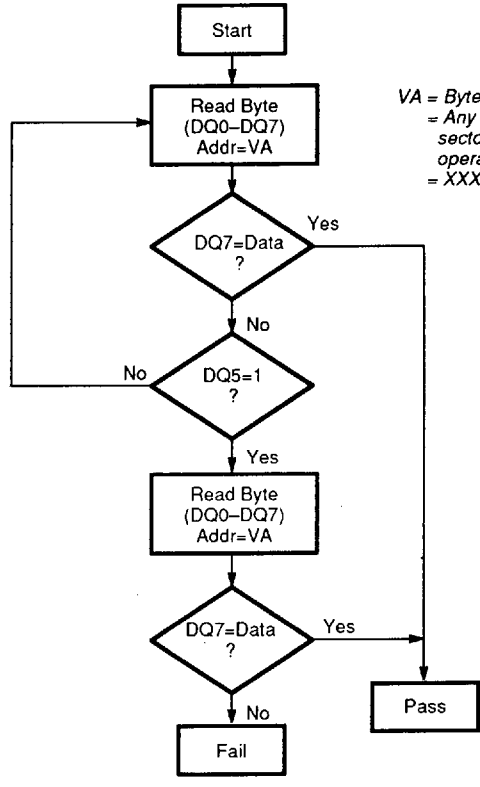


***Note:***

1. *DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

**Figure 3. $\overline{\text{Data}}$ Polling Algorithm**



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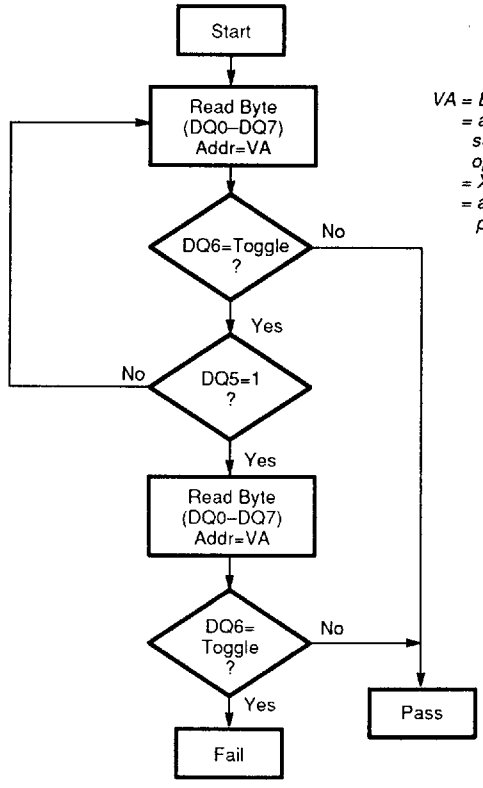


*VA = Byte address for programming*
*= any of the sector addresses within the sector being erased during sector erase operation*
*= XXXXH during chip erase*
*= any address not within the sector in the process of an Erase Suspend operation*

***Note:***

1. *DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".*

**Figure 4. Toggle Bit Algorithm**

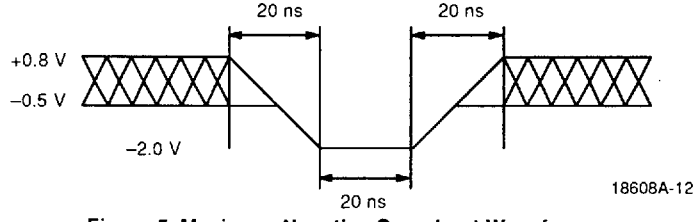


**Figure 5. Maximum Negative Overshoot Waveform**

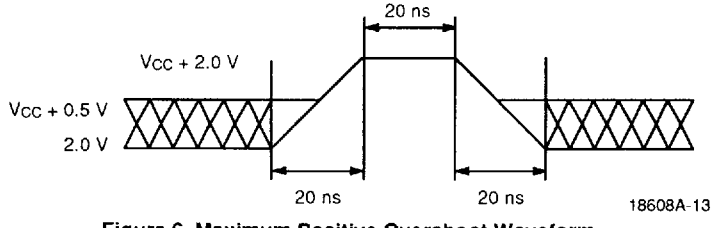


**Figure 6. Maximum Positive Overshoot Waveform**



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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... −65°C to +150°C
Plastic Packages ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to Ground
All pins except A9 (Note 1) ..... −2.0 V to +7.0 V

$V_{CC}$ (Note 1) ..... −2.0 V to +7.0 V

A9 (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

***Notes:***

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot $V_{SS}$ to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is $V_{CC}$ + 0.5 V. During voltage transitions, outputs may overshoot to $V_{CC}$ + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 pin is −0.5 V. During voltage transitions, A9 may overshoot $V_{SS}$ to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

## OPERATING RANGES

**Commercial (C) Devices**
Case Temperature (Tc) ..... 0°C to +70°C

**Industrial (I) Devices**
Case Temperature (Tc) ..... −40°C to +85°C

**Extended (E) Devices**
Case Temperature (Tc) ..... −55°C to +125°C

**Military (M) Devices**
Case Temperature (Tc) ..... −55°C to +125°C

**$V_{CC}$ Supply Voltages**
$V_{CC}$ for Am29F200T/B-75 ..... +4.75 V to +5.25 V

$V_{CC}$ for Am29F200T/B-90, 120 ... +4.50 V to +5.50 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*



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## DC CHARACTERISTICS
### TTL/NMOS Compatible

| Parameter Symbol | Parameter Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = Vss to Vcc, Vcc = Vcc Max | | | ±1.0 | µA |
| $I_{LIT}$ | A9 Input Load Current | Vcc = Vcc Max, A9 = 12.5 V | | | 50 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = Vss to Vcc, Vcc = Vcc Max | | | ±1.0 | µA |
| $I_{CC1}$ | Vcc Active Current (Note 1) | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | Byte | | 40 | mA |
| | | | Word | | 50 | |
| $I_{CC2}$ | Vcc Active Current (Notes 2, 3) | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | | | 60 | mA |
| $I_{CC3}$ | Vcc Standby Current | Vcc = Vcc Max, $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$ | | | 1.0 | mA |
| $V_{IL}$ | Input Low Level | | | –0.5 | 0.8 | V |
| $V_{IH}$ | Input High Level | | | 2.0 | Vcc + 0.5 | V |
| $V_{ID}$ | Voltage for Autoselect and Sector Protect | Vcc = 5.0 V | | 11.5 | 12.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 5.8 mA, Vcc = Vcc Min | | | 0.45 | V |
| $V_{OH}$ | Output High Level | $I_{OH}$ = –2.5 mA Vcc = Vcc Min | | 2.4 | | V |
| $V_{LKO}$ | Low Vcc Lock-Out Voltage | | | 3.2 | 4.2 | V |

***Notes:***

1. *The Icc current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at $V_{IH}$.*
2. *Icc active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*



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## DC CHARACTERISTICS (continued)
### CMOS Compatible

| Parameter Symbol | Parameter Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = Vss to Vcc, Vcc = Vcc Max | | | ±1.0 | µA |
| $I_{LIT}$ | A9 Input Load Current | Vcc = Vcc Max, A9 = 12.5 V | | | 50 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = Vss to Vcc, Vcc = Vcc Max | | | ±1.0 | µA |
| $I_{CC1}$ | Vcc Active Current (Note 1) | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | Byte | | 40 | mA |
| | | | Word | | 50 | |
| $I_{CC2}$ | Vcc Active Current (Notes 2, 3) | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | | | 60 | mA |
| $I_{CC3}$ | Vcc Standby Current | Vcc = Vcc Max, $\overline{CE}$ = Vcc ± 0.5 V, $\overline{OE}$ = $V_{IH}$ | | | 100 | µA |
| $V_{IL}$ | Input Low Level | | | –0.5 | 0.8 | V |
| $V_{IH}$ | Input High Level | | | 0.7x Vcc | Vcc +0.3 | V |
| $V_{ID}$ | Voltage for Autoselect and Sector Protect | Vcc = 5.0 V | | 11.5 | 12.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 5.8 mA, Vcc = Vcc Min | | | 0.45 | V |
| $V_{OH1}$ | Output High Voltage | $I_{OH}$ = –2.5 mA, Vcc = Vcc Min | | 0.85 Vcc | | V |
| $V_{OH2}$ | | $I_{OH}$ = –100 µA, Vcc = Vcc Min | | Vcc –0.4 | | V |
| $V_{LKO}$ | Low Vcc Lock-out Voltage | | | 3.2 | 4.2 | V |

***Notes:***

1. *The $I_{CC}$ current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at $V_{IH}$.*
2. *$I_{CC}$ active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*



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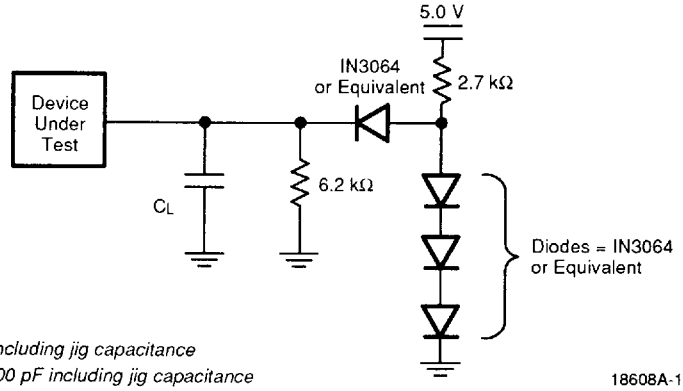
## AC CHARACTERISTICS

### Read Only Operations Characteristics

| Parameter Symbols | | Description | Test Setup | | -75 (Note 1) | -90 (Note 2) | -120 (Note 2) | -150 (Note 2) | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Standard | | | | | | | | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time (Note 4) | | Min | 70 | 90 | 120 | 150 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | $\overline{CE}$ = $V_{IL}$<br>$\overline{OE}$ = $V_{IL}$ | Max | 70 | 90 | 120 | 150 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | $\overline{OE}$ = $V_{IL}$ | Max | 70 | 90 | 120 | 150 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | Max | 30 | 35 | 50 | 55 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z (Note 3, 4) | | Max | 20 | 20 | 30 | 35 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z (Note 3, 4) | | Max | 20 | 20 | 30 | 35 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First | | Min | 0 | 0 | 0 | 0 | ns |
| | $t_{Ready}$ | $\overline{RESET}$ pin low to read mode | | Max | 20 | 20 | 20 | 20 | µs |
| | $t_{ELFL}$<br>$t_{ELFH}$ | $\overline{CE}$ to $\overline{BYTE}$ switching low or high | | Max | 5 | 5 | 5 | 5 | ns |

***Notes:***

1. *Test Conditions:*
   *Output Load: 1 TTL gate and 30 pF*
   *Input rise and fall times: 5 ns*
   *Input pulse levels: 0.0 V to 3.0 V*
   *Timing measurement reference level*
   *Input: 1.5 V*
   *Output: 1.5 V*
2. *Test Conditions:*
   *Output Load: 1 TTL gate and 100 pF*
   *Input rise and fall times: 20 ns*
   *Input pulse levels: 0.45 V to 2.4 V*
   *Timing measurement reference level*
   *Input: 0.8 and 2.0 V*
   *Output: 0.8 and 2.0 V*
3. *Output driver disable time.*
4. *Not 100% tested.*




***Notes:***

*For -70: $C_L$ = 30 pF including jig capacitance*
*For all others: $C_L$ = 100 pF including jig capacitance*

**Figure 7. Test Conditions**



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## AC CHARACTERISTICS

### Write/Erase/Program Operations

| Parameter Symbols | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| JEDEC | Standard | Description | | -70 | -90 | -120 | -150 | Unit |
| tAVAV | tWC | Write Cycle Time (3) | Min | 70 | 90 | 120 | 150 | ns |
| tAVWL | tAS | Address Setup Time | Min | 0 | 0 | 0 | 0 | ns |
| tWLAX | tAH | Address Hold Time | Min | 45 | 45 | 50 | 50 | ns |
| tDVWH | tDS | Data Setup Time | Min | 30 | 45 | 50 | 50 | ns |
| tWHDX | tDH | Data Hold Time | Min | 0 | 0 | 0 | 0 | ns |
| | tOES | Output Enable Setup Time (3) | Min | 0 | 0 | 0 | 0 | ns |
| | tOEH | Output Enable Hold Time — Read (3) | Min | 0 | 0 | 0 | 0 | ns |
| | | Output Enable Hold Time — Toggle and $\overline{\text{Data}}$ Polling (3) | Min | 10 | 10 | 10 | 10 | ns |
| tGHWL | tGHWL | Read Recover Time Before Write | Min | 0 | 0 | 0 | 0 | ns |
| tELWL | tCS | $\overline{CE}$ Setup Time | Min | 0 | 0 | 0 | 0 | ns |
| tWHEH | tCH | $\overline{CE}$ Hold Time | Min | 0 | 0 | 0 | 0 | ns |
| tWLWH | tWP | Write Pulse Width | Min | 35 | 45 | 50 | 50 | ns |
| tWHWL | tWPH | Write Pulse Width High | Min | 20 | 20 | 20 | 20 | ns |
| tWHWH1 | tWHWH1 | Byte Programming Operation | Typ | 16 | 16 | 16 | 16 | µs |
| tWHWH2 | tWHWH2 | Erase Operation (1) | Typ | 1.5 | 1.5 | 1.5 | 1.5 | sec |
| | | | Max | 30 | 30 | 30 | 30 | sec |
| | tVCS | Vcc Set Up Time (3) | Min | 50 | 50 | 50 | 50 | µs |
| | tVLHT | Voltage Transition Time (2, 3, 5) | Min | 4 | 4 | 4 | 4 | µs |
| | tWPP | Write Pulse Width (2) | Min | 100 | 100 | 100 | 100 | µs |
| | tWPP2 | Write Pulse Width (5) | Min | 10 | 10 | 10 | 10 | ms |
| | tOESP | $\overline{OE}$ Setup Time to $\overline{WE}$ Active (2, 3, 5) | Min | 4 | 4 | 4 | 4 | µs |
| | tCSP | $\overline{CE}$ Setup Time to $\overline{WE}$ Active (3) | Min | 4 | 4 | 4 | 4 | µs |
| | tRP | $\overline{RESET}$ Pulse Width | Min | 500 | 500 | 500 | 500 | ns |
| | tFLQZ | $\overline{BYTE}$ Switching Low to Output High Z (3, 4) | Max | 20 | 30 | 30 | 30 | ns |
| | tBUSY | Program/Erase Valid to RD/$\overline{BY}$ delay (3) | Min | 30 | 35 | 50 | 55 | ns |

***Notes:***

1. *This does not include the preprogramming time.*
2. *These timings are for Sector Protect operation.*
3. *Not 100% tested.*
4. *Output Driver Disable Time*



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## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must Be Steady | Will Be Steady |
| | May Change from H to L | Will Be Changing from H to L |
| | May Change from L to H | Will Be Changing from L to H |
| | Don't Care, Any Change Permitted | Changing, State Unknown |
| | Does Not Apply | Center Line is High-Impedance "Off" State |

KS000010

## SWITCHING WAVEFORMS

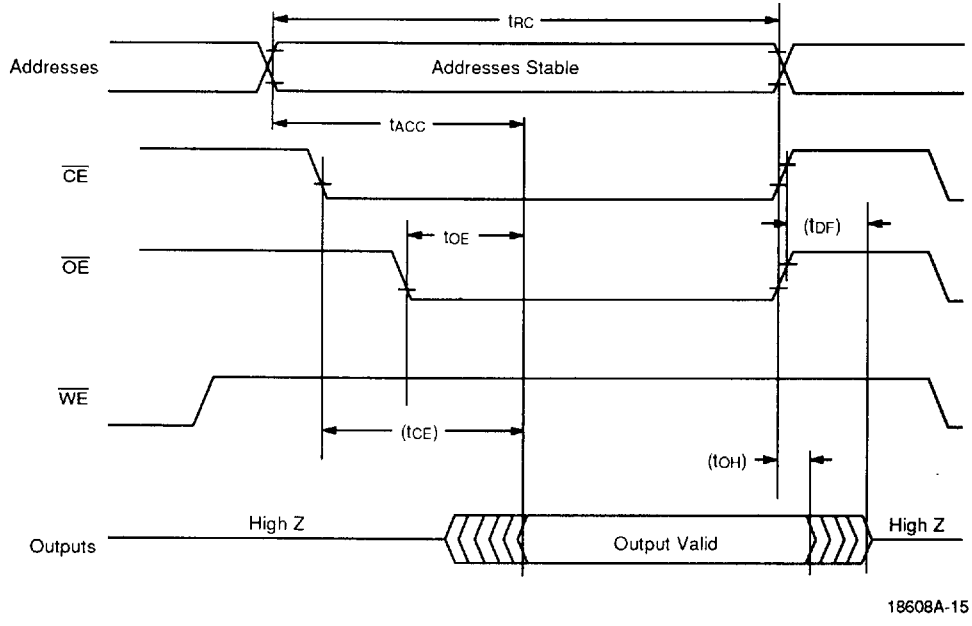


Figure 8. AC Waveforms for Read Operations



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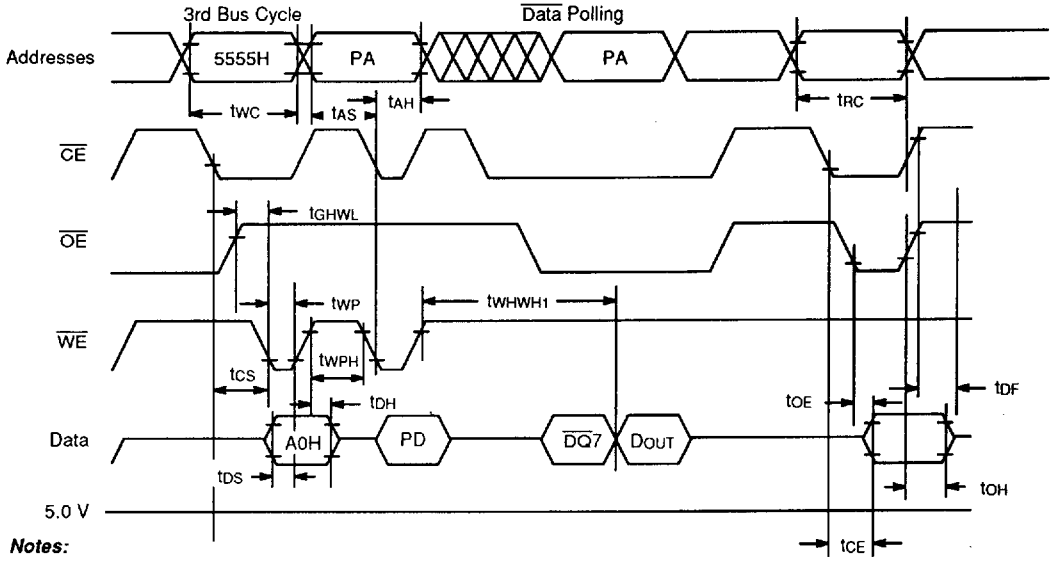
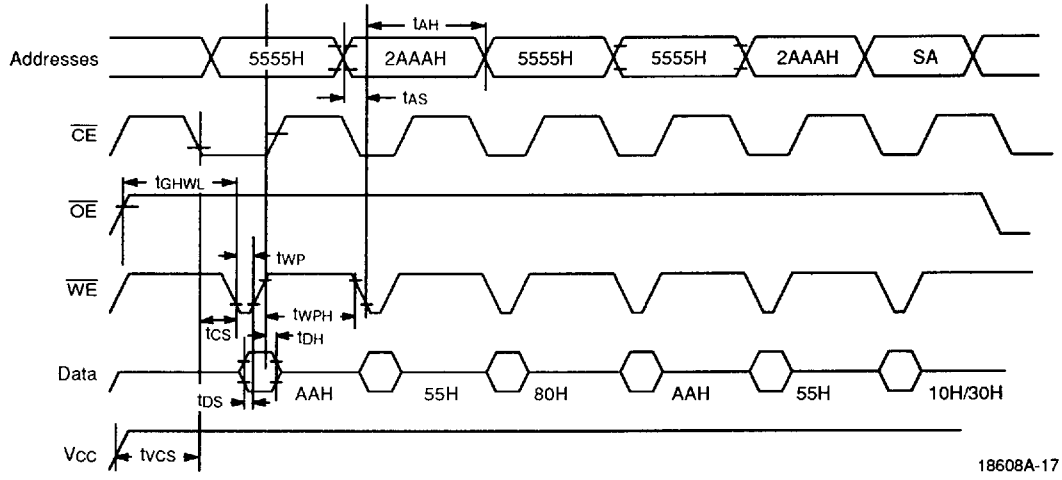
## SWITCHING WAVEFORMS




***Notes:***

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *$D_{OUT}$ is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*
6. *These waveforms are for the x16 mode.*

**Figure 9. Program Operation Timings**




***Notes:***

1. *SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.*
2. *These waveforms are for the x16 mode.*

**Figure 10. AC Waveforms Chip/Sector Erase Operations**



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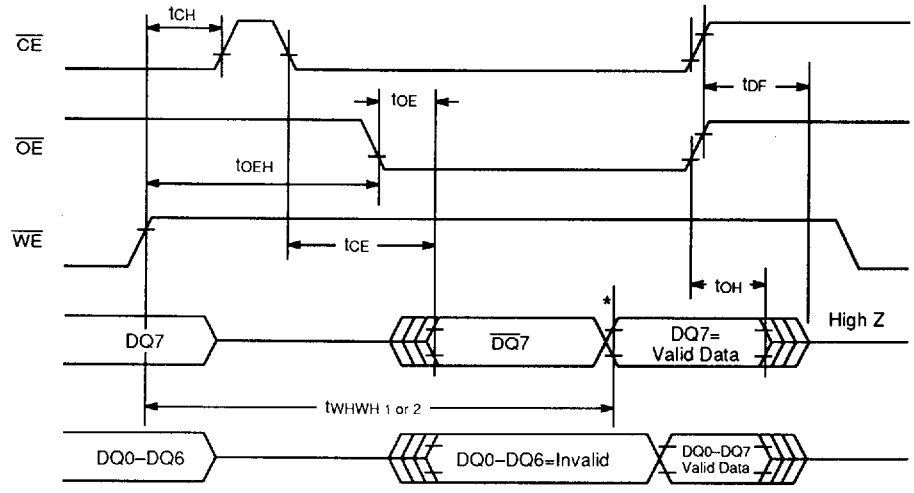
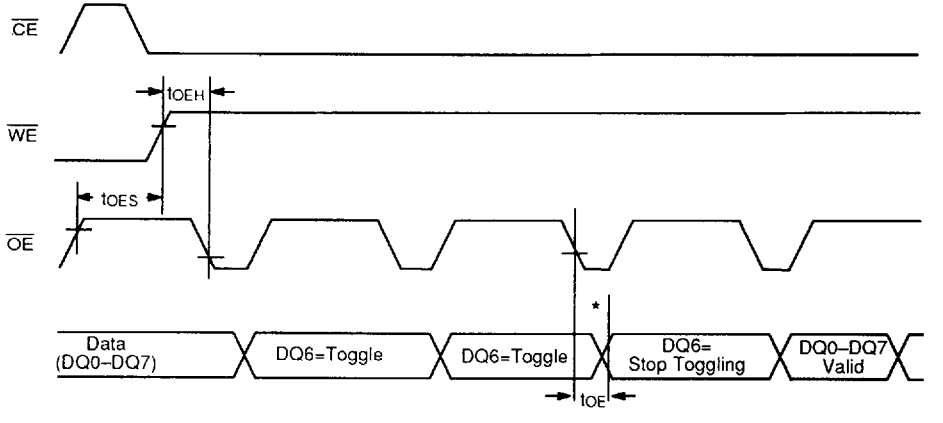
## SWITCHING WAVEFORMS




*DQ7=Valid Data (The device has completed the Embedded operation). 18608A-18

**Figure 11. AC Waveforms for Data Polling During Embedded Algorithm Operations**

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***Note:***

*DQ6 stops toggling (The device has completed the Embedded operation).

**Figure 12. AC Waveforms for Toggle Bit During Embedded Algorithm Operations**



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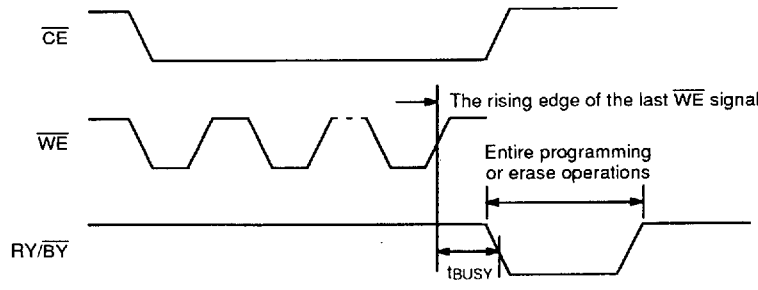


**Figure 13. RY/BY Timing Diagram During Program/Erase Operations**

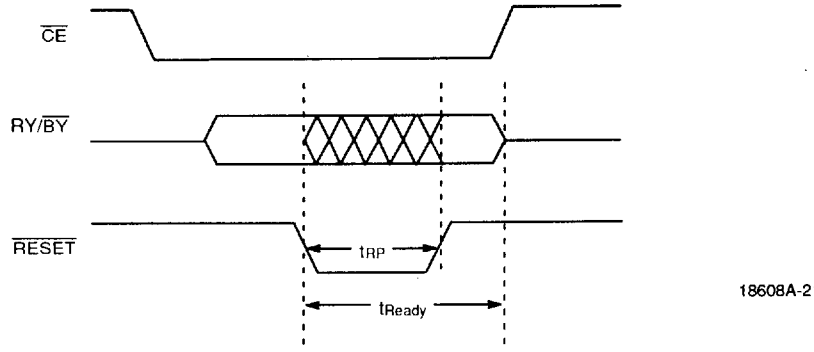


**Figure 14. RESET/RY/BY Timing Diagram**



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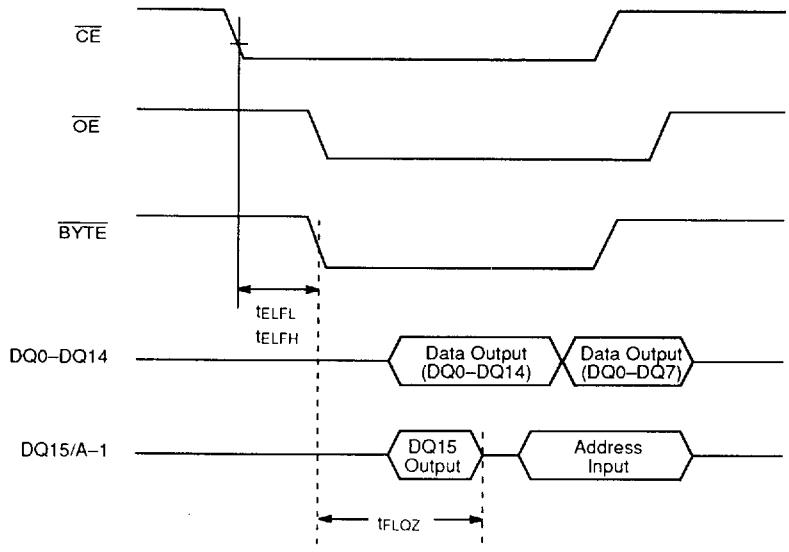


Figure 15. BYTE Timing Diagram for Read Operation

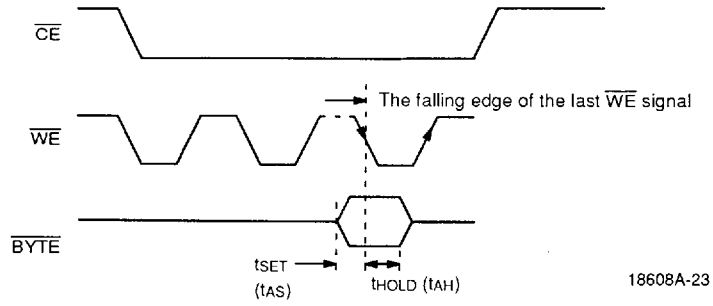


Figure 16. BYTE Timing Diagram for Write Operations



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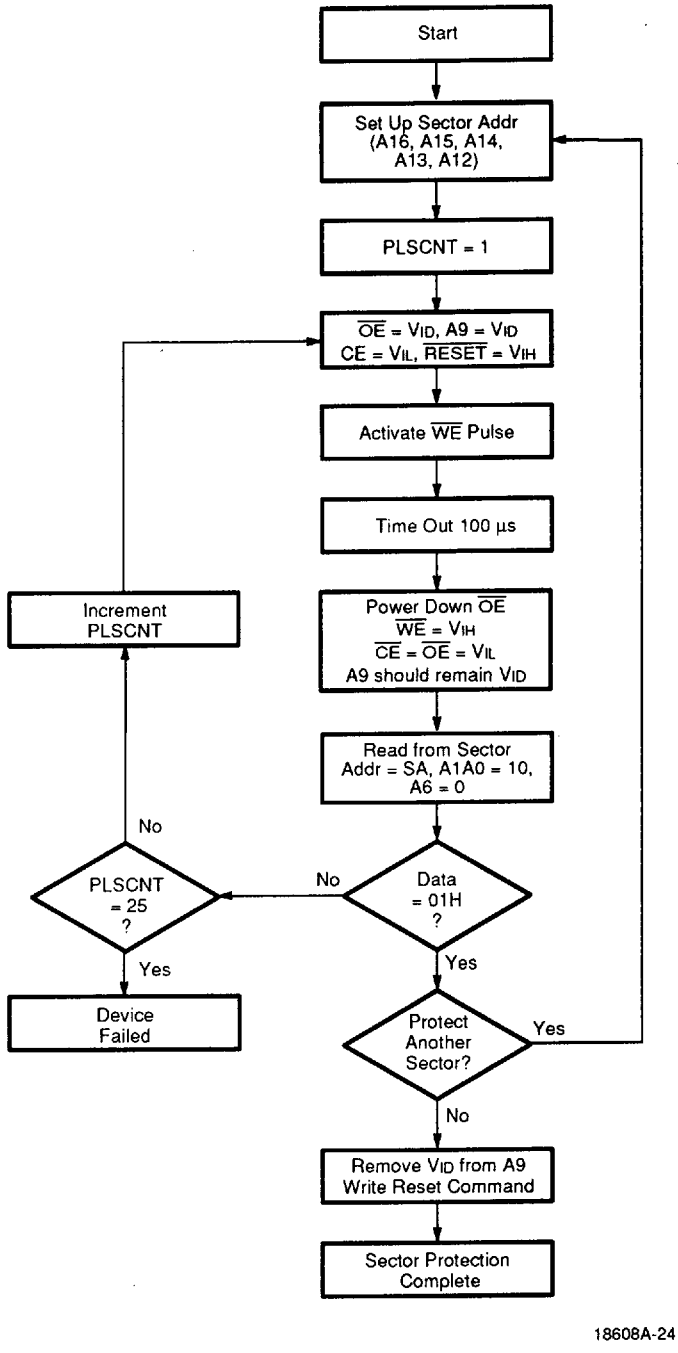


**Figure 17. Sector Protection Algorithm**



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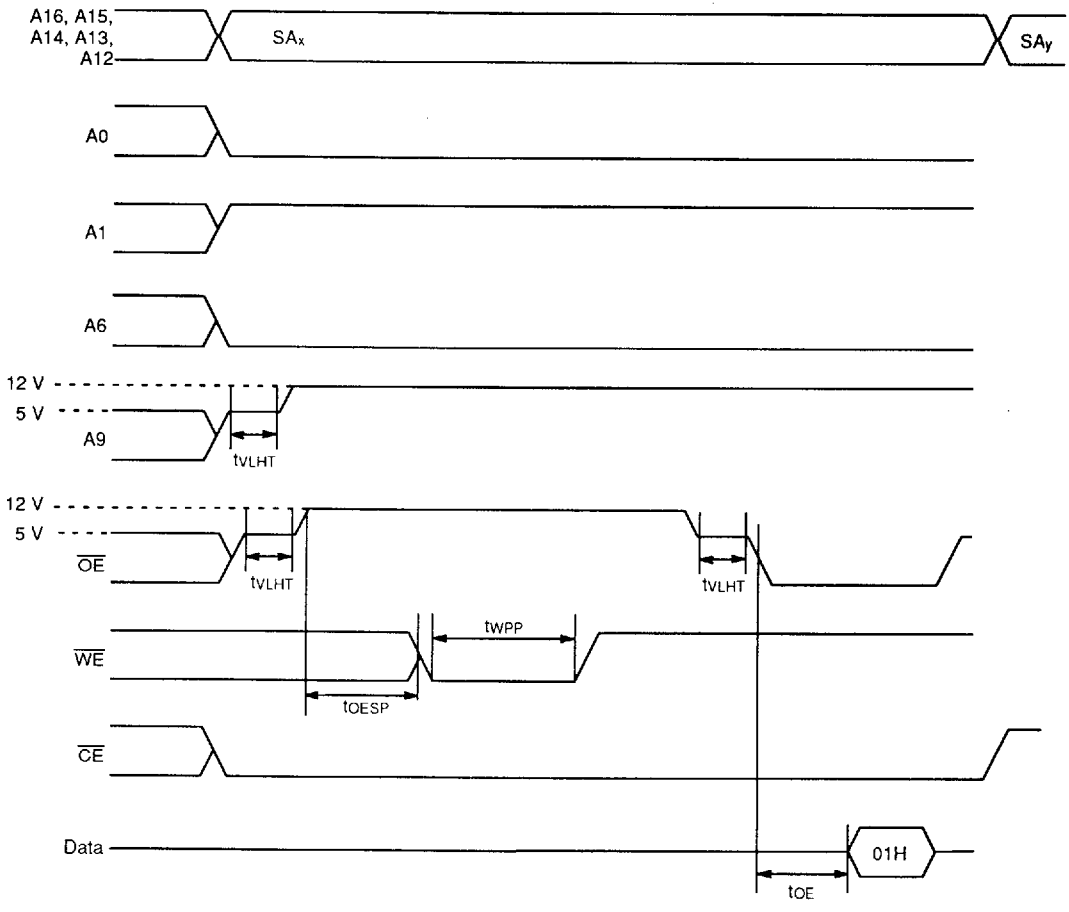
## SWITCHING WAVEFORMS




*SAx = Sector Address for initial sector*

*SAy = Sector Address for next sector*

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**Figure 18. AC Waveforms for Sector Protection**



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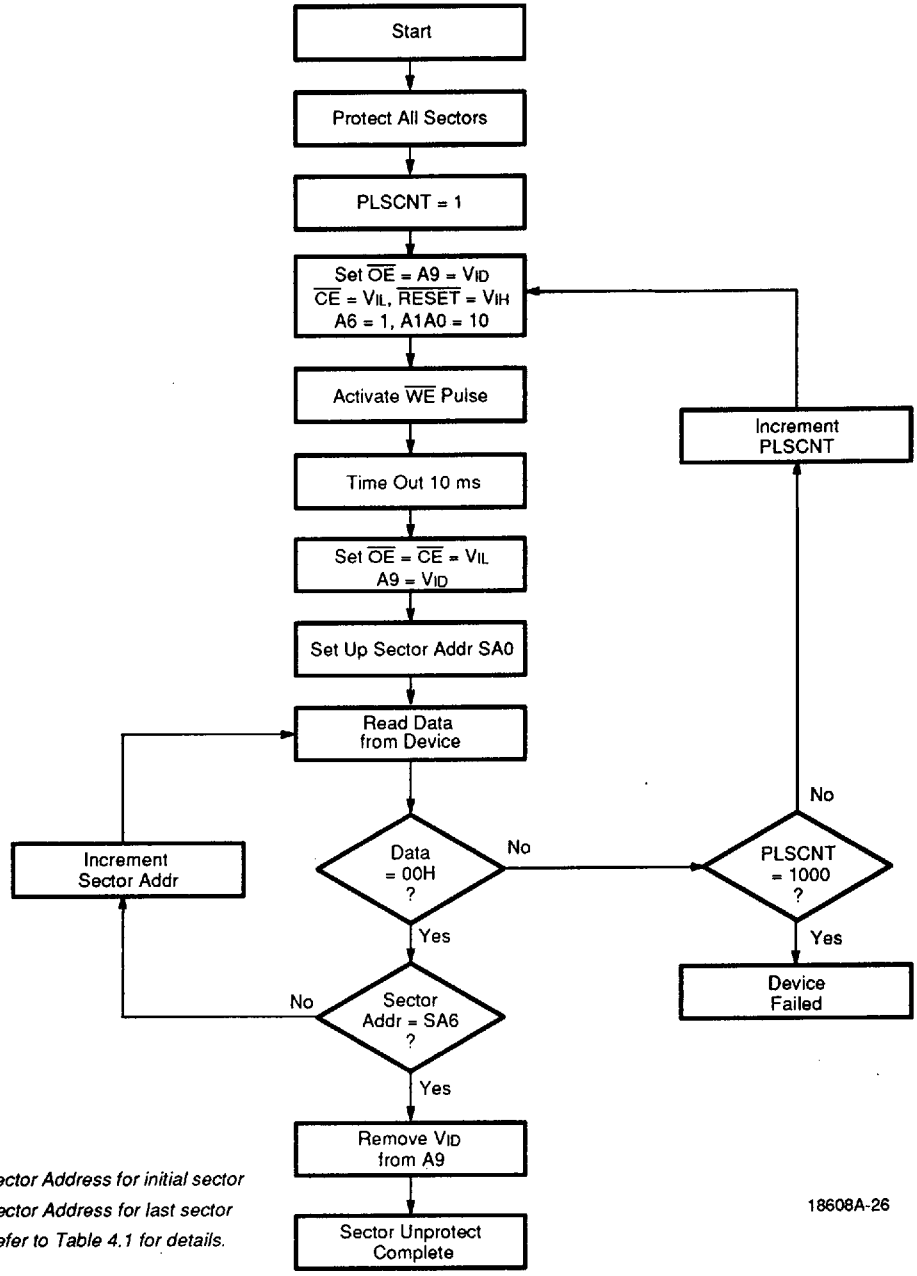


***Notes:***
*SA0 = Sector Address for initial sector*
*SA6 = Sector Address for last sector*
*Please refer to Table 4.1 for details.*

**Figure 19. Sector Unprotect Algorithm**



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## SWITCHING WAVEFORMS

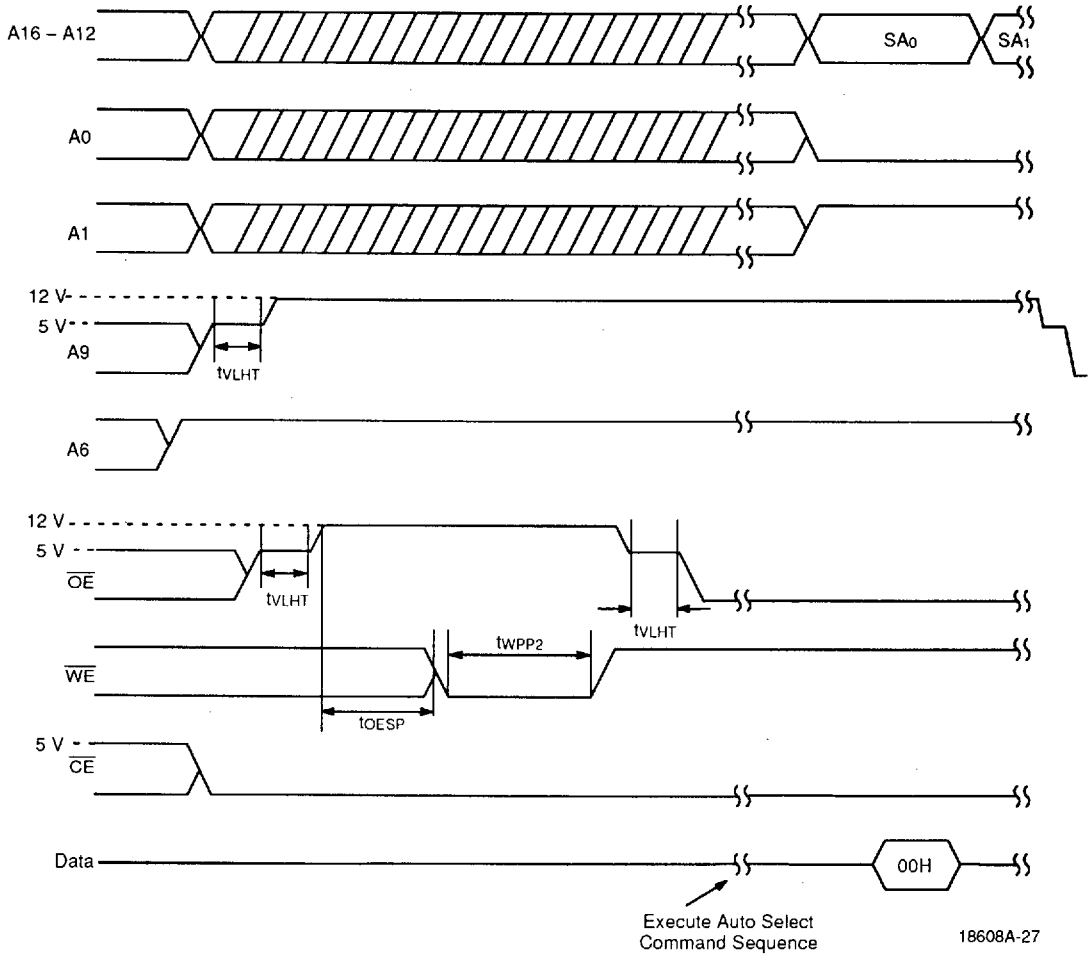


Figure 20. AC Waveforms for Sector Unprotect



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## AC CHARACTERISTICS

### Write/Erase/Program Operations

**Alternate $\overline{CE}$ Controlled Writes**

| Parameter Symbols | | | | | -70 | -90 | -120 | -150 | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Standard | Description | | | | | | | |
| tAVAV | tWC | Write Cycle Time (4) | | Min | 70 | 90 | 120 | 150 | ns |
| tAVEL | tAS | Address Setup Time | | Min | 0 | 0 | 0 | 0 | ns |
| tELAX | tAH | Address Hold Time | | Min | 45 | 45 | 50 | 50 | ns |
| tDVEH | tDS | Data Setup Time | | Min | 30 | 45 | 50 | 50 | ns |
| tEHDX | tDH | Data Hold Time | | Min | 0 | 0 | 0 | 0 | ns |
| | tOES | Output Enable Setup Time | | Min | 0 | 0 | 0 | 0 | ns |
| | tOEH | Output Enable Hold Time (4) | Read (4) | Min | 0 | 0 | 0 | 0 | ns |
| | | | Toggle and $\overline{Data}$ Polling | Min | 10 | 10 | 10 | 10 | ns |
| tGHEL | tGHEL | Read Recover Time Before Write | | Min | 0 | 0 | 0 | 0 | ns |
| tWLEL | tWS | $\overline{WE}$ Setup Time | | Min | 0 | 0 | 0 | 0 | ns |
| tEHWH | tWH | $\overline{WE}$ Hold Time | | Min | 0 | 0 | 0 | 0 | ns |
| tELEH | tCP | $\overline{CE}$ Pulse Width | | Min | 35 | 45 | 50 | 50 | ns |
| tEHEL | tCPH | $\overline{CE}$ Pulse Width High | | Min | 20 | 20 | 20 | 20 | ns |
| tWHWH1 | tWHWH1 | Byte Programming Operation | | Typ | 16 | 16 | 16 | 16 | µs |
| tWHWH2 | tWHWH2 | Erase Operation (1) | | Typ | 1.5 | 1.5 | 1.5 | 1.5 | sec |
| | | | | Max | 30 | 30 | 30 | 30 | sec |
| | tVCS | Vcc Set Up Time (4) | | Typ | 50 | 50 | 50 | 50 | µs |
| | tRP | $\overline{RESET}$ Pulse Width | | Min | 500 | 500 | 500 | 500 | ns |
| | tFLQZ | $\overline{BYTE}$ Switching Low to Output High Z (3, 4) | | Max | 20 | 30 | 30 | 30 | ns |
| | tBUSY | Program/Erase Valid to RD/$\overline{BY}$ Delay (4) | | Min | 30 | 35 | 50 | 55 | ns |

***Notes:***

1. *This does not include the preprogramming time.*
2. *These timings are for Sector Protect/Unprotect operations.*
3. *This timing is only for Sector Unprotect.*
4. *Not 100% tested.*



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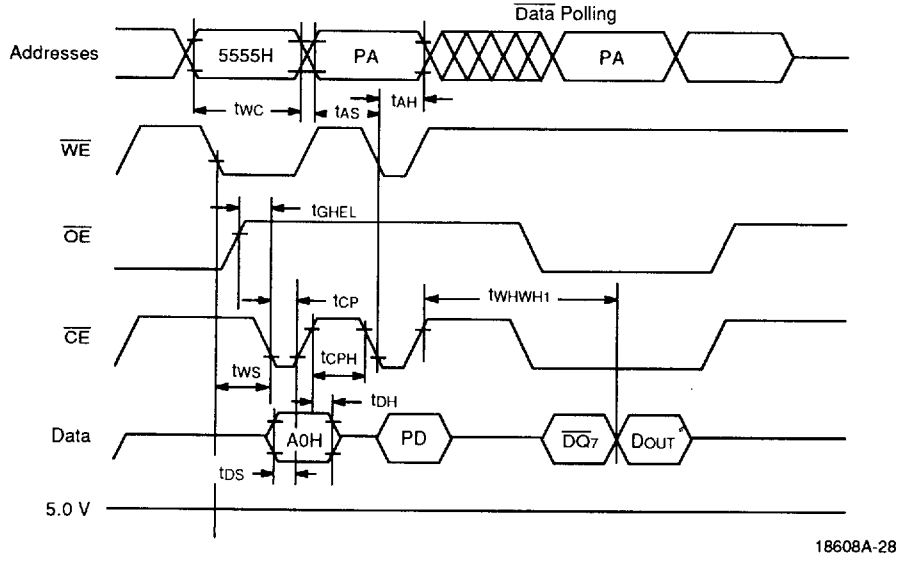


***Notes:***

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*
6. *These waveforms are for the x16 mode.*

**Figure 21. Alternate $\overline{CE}$ Controlled Program Operation Timings**



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## ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Limits | | | Unit | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Chip and Sector Erase Time | | 1.5 (Note 1) | 30 | sec | Excludes 00H programming prior to erasure |
| Byte Programming Time | | 16 | 1000 (Note 2) | µs | Excludes system-level overhead |
| Chip Programming Time | | 8.5 (Note 1) | 50 | sec | Excludes system-level overhead |
| Erase/Program Cycles | 100,000 | 1,000,000 | | Cycles | |

***Notes:***

1. *25°C, 5 V $V_{CC}$, 100,000 cycles*
2. *The Embedded Algorithms allow for 48 ms byte program time.*

## LATCHUP CHARACTERISTICS

| | Min | Max |
|---|---|---|
| Input Voltage with respect to $V_{SS}$ on all I/O pins | −1.0 V | $V_{CC}$ + 1.0 V |
| $V_{CC}$ Current | −100 mA | +100 mA |

*Includes all pins except $V_{CC}$. Test conditions: $V_{CC}$ = 5.0 V, one pin at a time.*

## TSOP PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 8 | 10 | pF |

***Notes:***

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A$ = 25°C, f = 1.0 MHz*

## SO PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{PP}$ = 0 | 8 | 10 | pF |

***Notes:***

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A$ = 25°C, f = 1.0 MHz*

## DATA RETENTION

| Parameter | Test Conditions | Min | Unit |
|---|---|---|---|
| Minimum Pattern Data Retention Time | 150°C | 10 | Years |
| | 125°C | 20 | Years |



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