Am29C827A/Am29C828A

High-Performance CMOS Bus Buffers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-speed CMOS buffers and inverters**
  - D-Y delay = 4 ns typical
- **Low standby power**
- **JEDEC FCT-compatible specs**
- **Very high output drive**
  - I_{OL} = 48 mA Commercial, 32 mA Military
- **Extra-wide (10-bit) data paths**
- **200-mV typical hysteresis on data input ports**
- **Minimal speed degradation with multiple outputs switching**
- **Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots, and ground bounce**
- **Power-up/down disable circuit provides for glitch-free power supply sequencing**
- **Ideal for driving 1Mbit x 1 and 1Mbit x 4 DRAM address inputs**
- **Can be powered off while in 3-state, ideal for card edge interface applications**
- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C827A and Am29C828A CMOS Bus Buffers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. Both devices feature 10-bit wide data paths and NORed output enables for maximum control flexibility. The Am29C827A has non-inverting outputs, while the Am29C828A has inverting outputs. Each device has data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C827A and Am29C828A are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 4 ns, as well as an output current drive of 48 mA.

The 29C827A and Am29C828A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits or edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

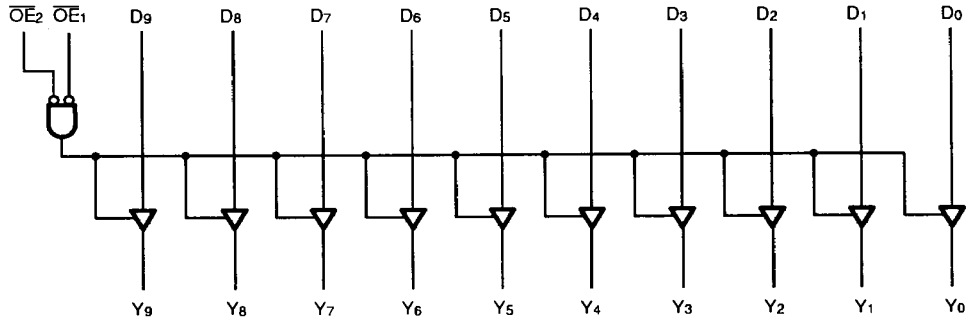
The Am29C827A and Am29C828A are available in the standard package options: DIPs, PLCCs, and SOICs.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

Publication# 11228 Rev. C Amendment/0
Issue Date: December 1990

BLOCK DIAGRAMS

Am29C827A (Noninverting)



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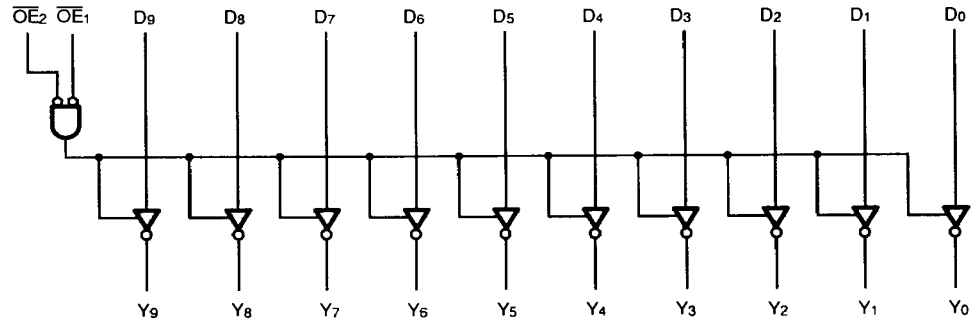
Am29C828A (Inverting)



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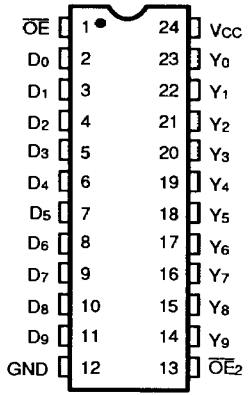
CONNECTION DIAGRAMS
(Top View)

DIPs*



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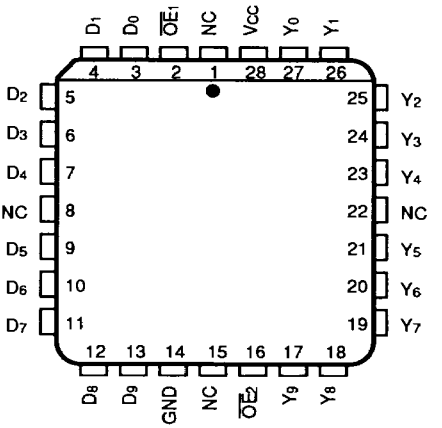
PLCC



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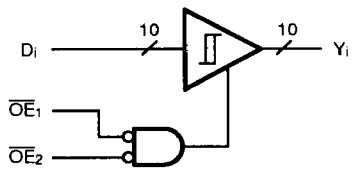
*Also available in Small Outline package; pinout identical to DIPs.

LOGIC SYMBOLS

Am29C827A



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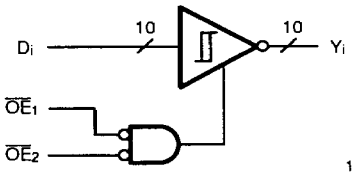
Am29C828A



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FUNCTION TABLES

Am29C827A

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	H	H	Transparent
L	L	L	L	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

Am29C828A

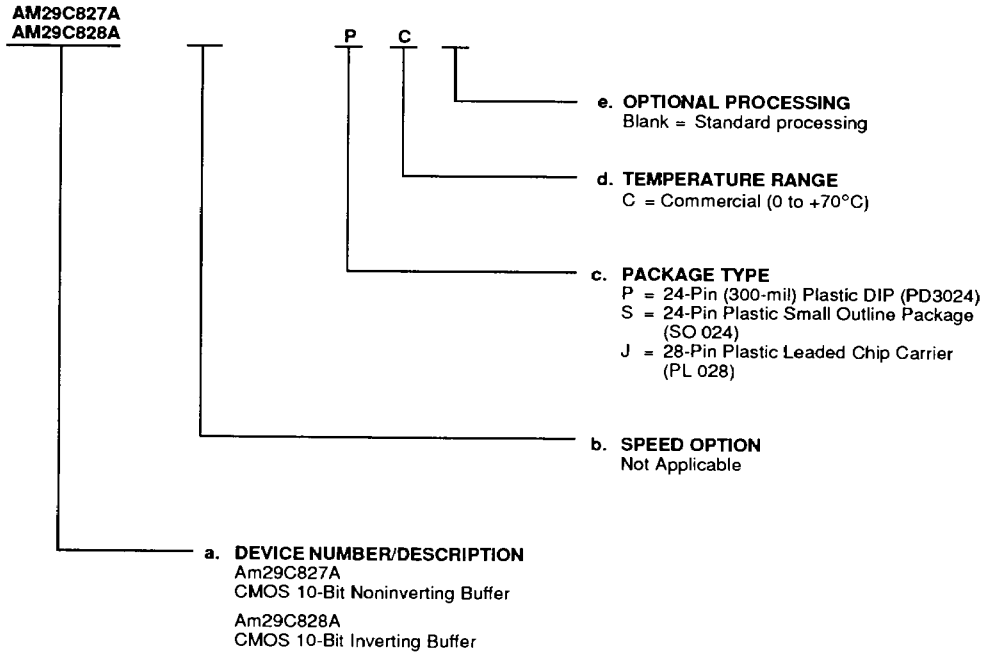
Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	H	L	Transparent
L	L	L	H	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

H = HIGH
L = LOW
X = Don't Care
Z = Hi-Z

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C827A	PC, SC, JC
AM29C828A	

Valid Combinations

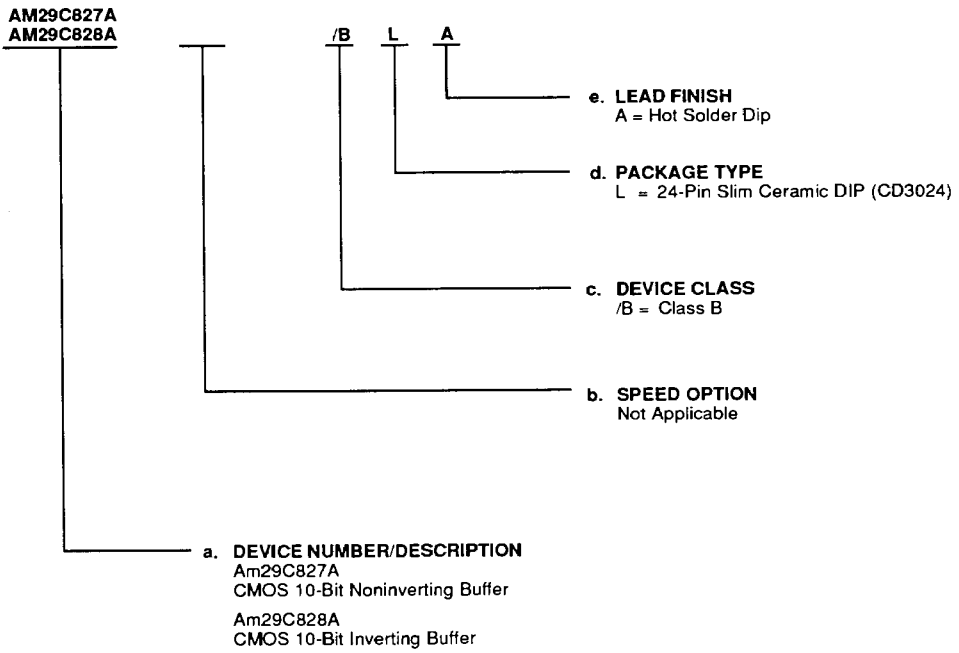
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations	
AM29C827A	/BLA
AM29C828A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$\overline{OE}_i$
Output Enables (Input, Active LOW)

When the $\overline{OE}_1$ and $\overline{OE}_2$ are both LOW, the outputs are enabled. When either one or both are HIGH, the outputs are in the Hi-Z state.

D_i
Data Inputs (Input)

D_i are the 10-bit data inputs.

Y_i
Data Outputs (Output)

Y_i are the 10-bit data outputs.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Supply Voltage to Ground Potential Continuous	–0.5 V to +7.0 V
DC Output Voltage	–0.5 V to +6.0 V
DC Input Voltage	–0.5 V to +6.0 V
DC Output Diode Current:	
Into Output	+50 mA
Out of Output	–50 mA
DC Input Diode Current:	
Into Input	+20 mA
Out of Input	–20 mA
DC Output Current per Pin:	
Into Output	+100 mA
Out of Output	–100 mA
Total DC Ground Current ($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)	
Total DC V_{CC} Current ($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)	

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Military (M) Devices

Temperature (T_A)	–55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V	MIL I_{OL} = 32 mA			0.5	V
		V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} = 48 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V				5	µA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V				+10	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = or GND				−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 2)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/ Bit
				$\overline{OE}_1$, $\overline{OE}_2$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 3)		Outputs Open		275	µA/ MHz/ Bit
				Outputs Loaded		400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output (Y_i)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	1.0	7.5	1.0	8.5	ns
t_{PHL}	Am29C827A (Noninverting) (Note 1)		1.0	7.5	1.0	8.5	ns
t_{PLH}	Data (D_i) to Output (Y_i)		1.0	7.5	0.5	8.5	ns
t_{PHL}	Am29C828A (Inverting) (Note 1)		1.0	7.5	0.5	8.5	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i		1.0	9	1.0	11	ns
t_{ZL}			3.0	12	3.0	14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i		2.0	8	2.0	9	ns
t_{LZ}			2.0	8	2.0	9	ns

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified

Symbol	Parameter Description (Note 2)	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output (Y_i)	C_L = 300 pF R_1 = 500 Ω R_2 = 500 Ω	1.0	15.5	1.0	17.0	ns
t_{PHL}	Am29C827A (Noninverting) (Note 1)		1.0	15.5	1.0	17.0	ns
t_{PLH}	Data (D_i) to Output (Y_i)		1.0	13.5	0.5	15.0	ns
t_{PHL}	Am29C828A (Inverting) (Note 1)		1.0	14	0.5	15.0	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i		1.0	13.5	1.0	15.0	ns
t_{ZL}			3.0	17	3.0	18.0	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i	C_L = 5 pF R_1 = 500 Ω R_2 = 500 Ω	2.0	7	2.0	8	ns
t_{LZ}			2.0	7	2.0	8	ns

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).
2. These parameters are guaranteed by characterization but not production tested.