Am29C660/A/B/C/D/E

CMOS Cascadable 32-Bit Error Detection and Correction Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Improves memory reliability**
  - Corrects all single-bit errors. Detects all double- and some triple-bit errors
- **Very high-speed error detection and correction**
  - Down to 9 ns data-in to error detection
- **Low-power CMOS process**
- **Cascadable for data words up to 64 bits**
- **Simplified byte operations**
  - Separate byte enables on the Data Output Latch for fast byte writes
- **Built-in diagnostics**
  - Proper EDC operation can be verified by the CPU via software control
- **Detects gross error conditions of all 1's or all 0's**

GENERAL DESCRIPTION

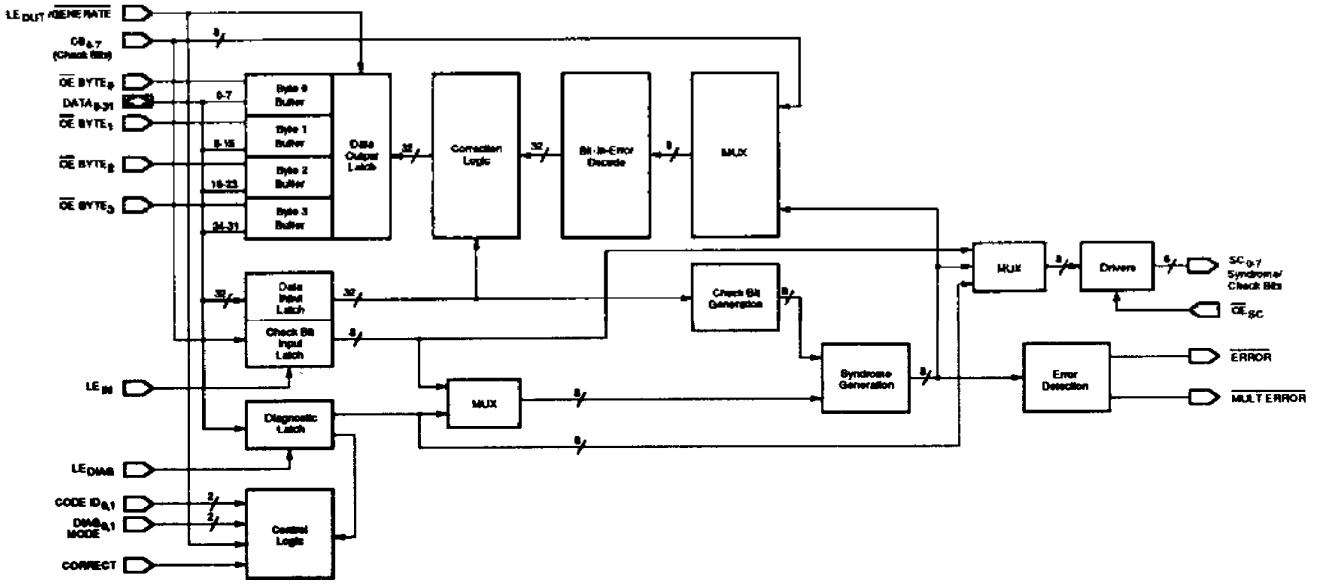
The Am29C660 CMOS Cascadable 32-Bit Error Detection and Correction Circuit (EDC) contains the logic necessary to generate check bits on a 32-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the Am29C660 detects and corrects all single-bit errors and detects all double- and some triple-bit errors. For 32-bit words, 7 check bits are used.

The Am29C660 is expandable to operate on 64-bit data words (8 check bits). In both configurations, the device makes error syndromes available on separate outputs for error logging.

The Am29C660 also features two diagnostic modes in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions.

When used with the Am29C668 Dynamic Memory Controller, the Am29C660 can perform AMD's invented memory "scrubbing" operation to provide highest data integrity.

BLOCK DIAGRAM



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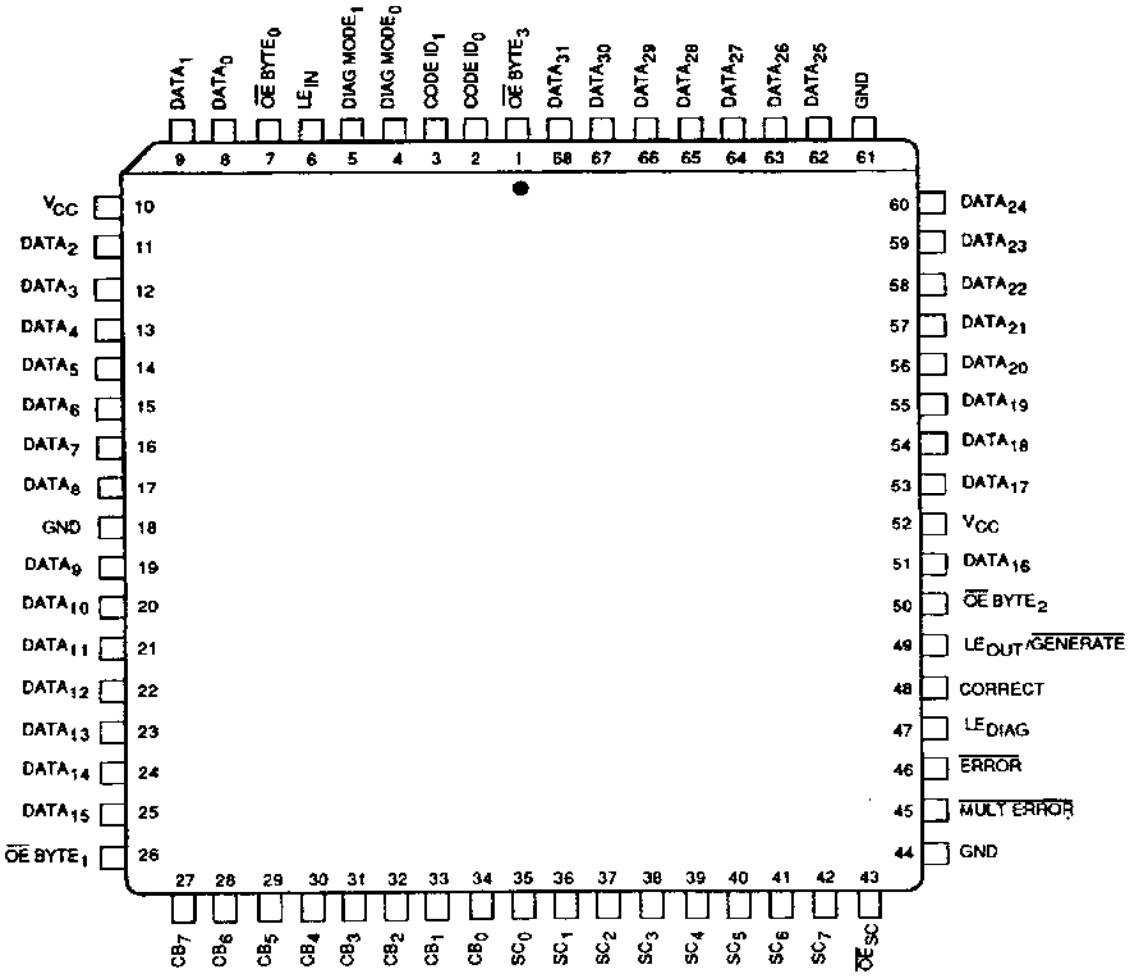
RELATED AMD PRODUCTS

Part No.	Description
Am29C668	4M Configurable Dynamic Memory Controller/Driver
Am29C983A	9-Bit x 4-Port Multiple Bus Exchange, High Speed
Am29C985	9-Bit x 4-Port Multiple Bus Exchange w/Parity
Am29C60A	16-Bit Cascadable EDC, High Speed
Am29C676	11-Bit Driver for 4M x 1 and 4M x 4 DRAMs
Am2965/6	8-Bit DRAM Driver (Inverting, Non-inverting)

CONNECTION DIAGRAMS
Top View

PLCC



Note: Pin 1 is marked for orientation (PLCC only).

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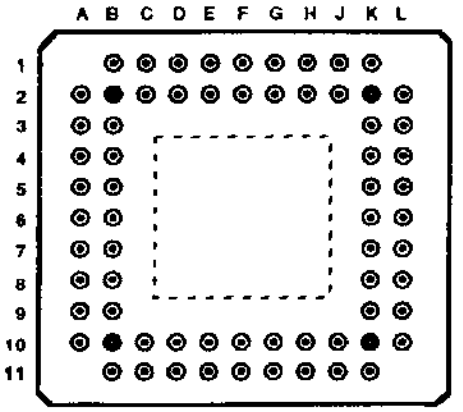
CONNECTION DIAGRAMS (Continued)

Bottom View

PGA

(Pins facing up)



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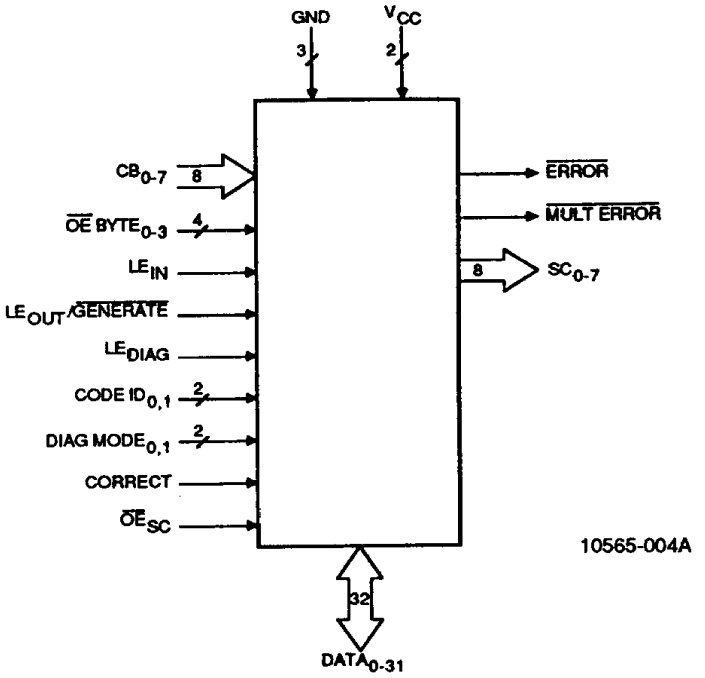
PGA PIN DESIGNATIONS
(Sorted by Pin No.)

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A-2	$DATA_1$	B-9	$DATA_{26}$	F-10	V_{CC}	K-4	CB_3
A-3	$DATA_0$	B-10	GND	F-11	$DATA_{17}$	K-5	CB_1
A-4	LE_{IN}	B-11	$DATA_{24}$	G-1	$DATA_{11}$	K-6	SC_0
A-5	DIAG $MODE_0$	C-1	$DATA_4$	G-2	$DATA_{10}$	K-7	SC_2
A-6	CODE ID_0	C-2	$DATA_3$	G-10	$\overline{OE}$ $BYTE_2$	K-8	SC_4
A-7	$DATA_{31}$	C-10	$DATA_{22}$	G-11	$DATA_{16}$	K-9	SC_6
A-8	$DATA_{29}$	C-11	$DATA_{23}$	H-1	$DATA_{13}$	K-10	GND
A-9	$DATA_{27}$	D-1	$DATA_6$	H-2	$DATA_{12}$	K-11	$\overline{MULT\ ERROR}$
A-10	$DATA_{25}$	D-2	$DATA_5$	H-10	CORRECT	L-2	CB_6
B-1	$DATA_2$	D-10	$DATA_{20}$	H-11	LE_{OUT}/ $\overline{GENERATE}$	L-3	CB_4
B-2	V_{CC}	D-11	$DATA_{21}$	J-1	$DATA_{15}$	L-4	CB_2
B-3	$\overline{OE}$ $BYTE_0$	E-1	$DATA_8$	J-2	$DATA_{14}$	L-5	CB_0
B-4	DIAG $MODE_1$	E-2	$DATA_7$	J-10	$\overline{ERROR}$	L-6	SC_1
B-5	CODE ID_1	E-10	$DATA_{18}$	J-11	LE_{DIAG}	L-7	SC_3
B-6	$\overline{OE}$ $BYTE_3$	E-11	$DATA_{19}$	K-1	$\overline{OE}$ $BYTE_1$	L-8	SC_5
B-7	$DATA_{30}$	F-1	$DATA_9$	K-2	CB_7	L-9	SC_7
B-8	$DATA_{28}$	F-2	GND	K-3	CB_5	L-10	$\overline{OE}_{SC}$

(Sorted by Pin Name)

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
L-5	CB_0	D-1	$DATA_6$	C-11	$DATA_{23}$	H-11	LE_{OUT}/ $\overline{GENERATE}$
K-5	CB_1	E-2	$DATA_7$	B-11	$DATA_{24}$	K-11	$\overline{MULT\ ERROR}$
L-4	CB_2	E-1	$DATA_8$	A-10	$DATA_{25}$	B-3	$\overline{OE}$ $BYTE_0$
K-4	CB_3	F-1	$DATA_9$	B-9	$DATA_{26}$	K-1	$\overline{OE}$ $BYTE_1$
L-3	CB_4	G-2	$DATA_{10}$	A-9	$DATA_{27}$	G-10	$\overline{OE}$ $BYTE_2$
K-3	CB_5	G-1	$DATA_{11}$	B-8	$DATA_{28}$	B-6	$\overline{OE}$ $BYTE_3$
L-2	CB_6	H-2	$DATA_{12}$	A-8	$DATA_{29}$	L-10	$\overline{OE}_{SC}$
K-2	CB_7	H-1	$DATA_{13}$	B-7	$DATA_{30}$	K-6	SC_0
A-6	CODE ID_0	J-2	$DATA_{14}$	A-7	$DATA_{31}$	L-6	SC_1
B-5	CODE ID_1	J-1	$DATA_{15}$	A-5	DIAG $MODE_0$	K-7	SC_2
H-10	CORRECT	G-11	$DATA_{16}$	B-4	DIAG $MODE_1$	L-7	SC_3
A-3	$DATA_0$	F-11	$DATA_{17}$	J-10	$\overline{ERROR}$	K-8	SC_4
A-2	$DATA_1$	E-10	$DATA_{18}$	B-10	GND	L-8	SC_5
B-1	$DATA_2$	E-11	$DATA_{19}$	F-2	GND	K-9	SC_6
C-2	$DATA_3$	D-10	$DATA_{20}$	K-10	GND	L-9	SC_7
C-1	$DATA_4$	D-11	$DATA_{21}$	J-11	LE_{DIAG}	B-2	V_{CC}
D-2	$DATA_5$	C-10	$DATA_{22}$	A-4	LE_{IN}	F-10	V_{CC}

LOGIC SYMBOL



Die Size: 0.174" x 0.176"
Gate Count: 1670

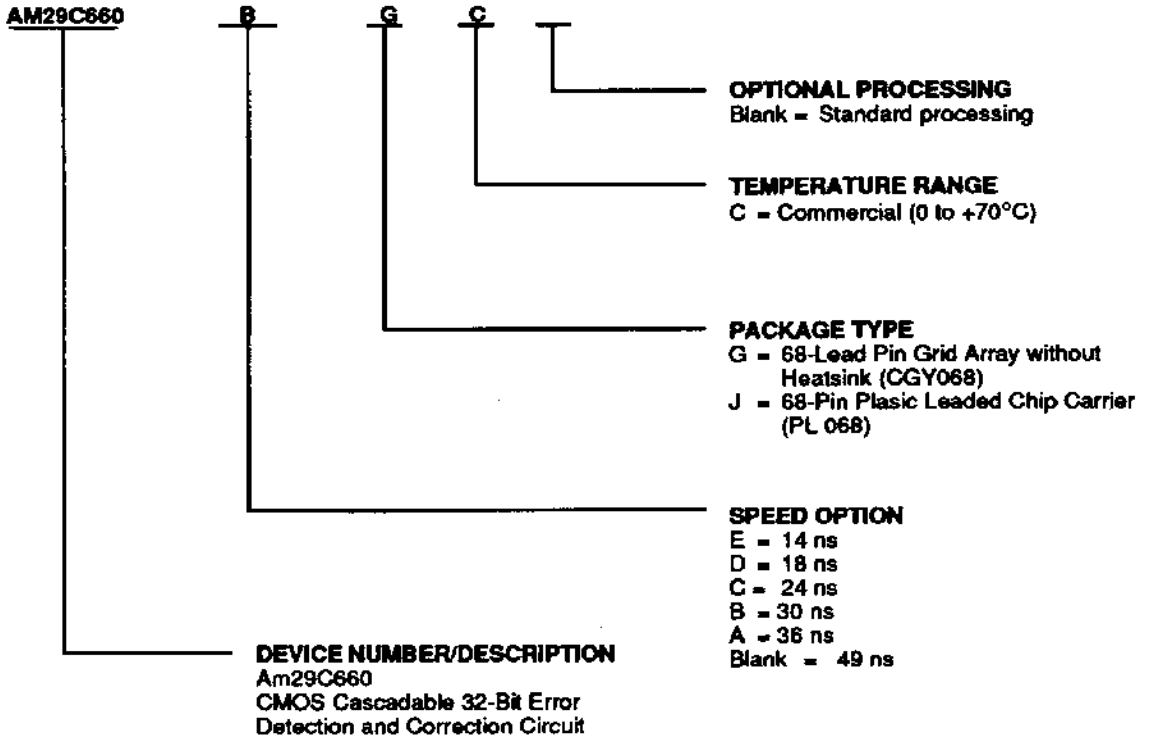
Package Information

Parameter	PGA	PLCC	Unit
θ_{JA}	34	35	°C/W
θ_{JC}	–	N/A	°C/W

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following elements:

Device Number
Speed Option (if applicable)
Package Type
Temperature Range
Optional Processing



Valid Combinations	
AM29C660	GC, JC
AM29C660A	
AM29C660B	
AM29C660C	
AM29C660D	
AM29C660E	

Valid Combinations

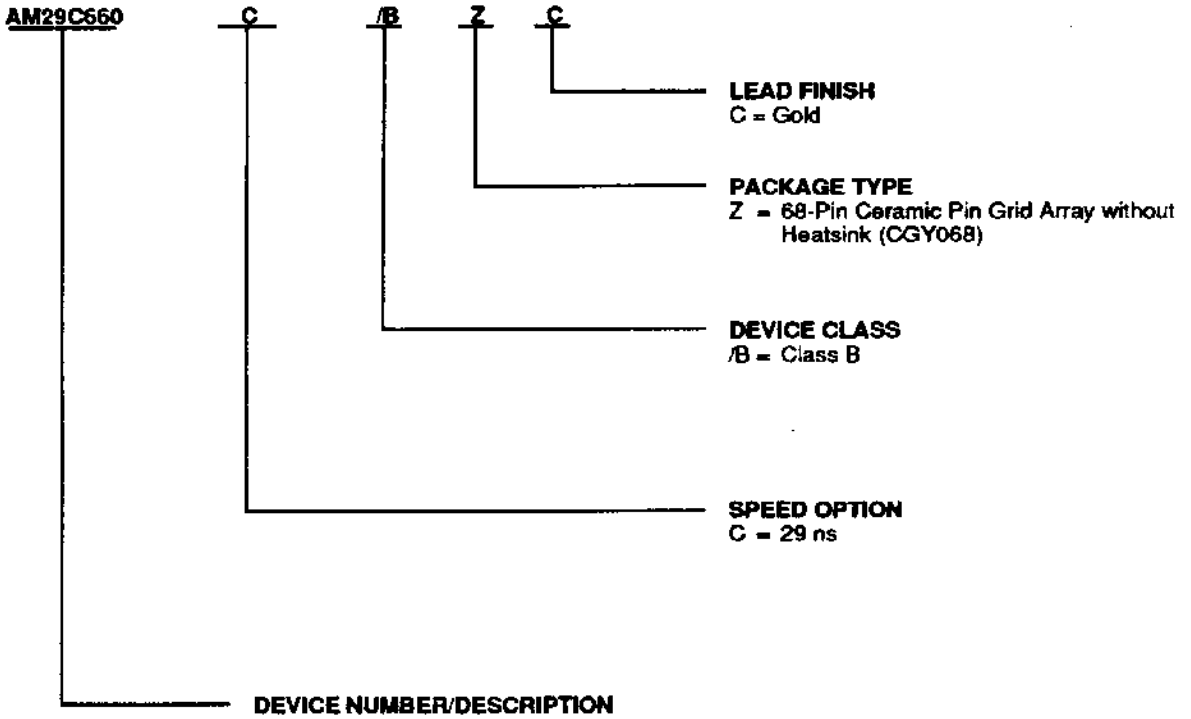
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of the following elements:

Device Number
Speed Option (if applicable)
Device Class
Package Type
Lead Finish



Valid Combinations	
AM29C660C	/BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

CB_{0-7}
Check Bits (Inputs)

These eight check bit lines are used to input bits for error detection. They are also used to input syndrome bits for error correction in the 64-bit configuration.

CODE $ID_{0,1}$
Code Identification (Inputs)

These two code identification inputs identify the size of the total data word to be processed. The two allowable data word sizes are 32 and 64 bits and their respective modified Hamming Codes are designated 32/39 and 64/72. The CODE ID inputs are also used to instruct the EDC that the CODE $ID_{0,1}$, DIAG $MODE_{0,1}$, and CORRECT signals are to be taken from the Diagnostic Latch, rather than from the input control lines (Reference Table 1).

CORRECT
Correct (Input; Active HIGH)

This signal allows the correction network to correct any single-bit error in the Data Input Latch before putting it into the Data Output Latch by complementing the bit-in-error. When the signal is LOW, the EDC routes data directly from the Data Input Latch to the Data Output Latch without correction.

$DATA_{0-31}$
Data (Inputs/Outputs; Three-State)

These bidirectional data lines provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit and $DATA_{31}$ is the most significant bit.

DIAG $MODE_{0,1}$
Diagnostic Mode Select (Inputs; Active HIGH)

These two lines control the initialization and diagnostic operation of the EDC circuit (Reference Table 2).

$\overline{\text{ERROR}}$
Error Detection Flag (Output; Active LOW)

When the EDC is in the Detect or Detect/Correct Mode, this output goes LOW if one or more syndrome bits are nonzero, indicating one or more data and/or check bits are in error. If all syndrome bits are zero, there are no errors detected and the output will be HIGH. In the Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH.

GND (3)
0-V Power Supply

These pins are the 0-V power supply to the EDC circuit. All grounds must be connected during device operation.

LE_{DIAG}
Diagnostic Latch Enable (Input)

This is the latch enable for the Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 32-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE $ID_{0,1}$, DIAG $MODE_{0,1}$, and CORRECT.

LE_{IN}
Latch Enable Data Input Latch (Input)

This input controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits, respectively. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous states.

$LE_{OUT}/\overline{\text{GENERATE}}$
Latch Enable – Data Output Latch (Input)/$\overline{\text{Generate}}$ Check Bits (Input; Active LOW)

This is a multifunction pin. When it is LOW, it operates in the Check Bit Generate Mode. In this mode, the device generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the syndrome/check bit outputs. The Data Output Latch is latched to its previous state when this pin is LOW.

When HIGH, the device is in the Detect or Detect/Correct Mode. In the Detect Mode, the device detects single and multiple errors, and generates syndrome bits specific to the data in the Data Input Latch and Check Bit Input Latch. In the Detect/Correct Mode, single-bit errors are automatically corrected, with the corrected data placed at the inputs of the Data Output Latch. The syndrome result is placed on the syndrome/check bit outputs and indicates, in a coded form, the number of errors and the specific bit in error. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network.

In the Detect/Correct Mode, single-bit errors are corrected by the network before being loaded into the Data Output Latch. In the Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The Data Output Latch is disabled with its contents unchanged if the EDC is in the Generate Mode.

$\overline{\text{MULT ERROR}}$
Multiple Error Detection Flag (Output; Active LOW)

When LOW in the Detect or Detect/Correct Mode, this output indicates that two or more bit errors have been detected. If HIGH, either one or no errors have been detected. In the Generate Mode, $\overline{\text{MULT ERROR}}$ is forced HIGH.

$\overline{\text{OE}}$ $BYTE_{0-3}$
Output Enable Bytes 0–3 (Inputs; Active LOW)

These lines control the three-state output buffers for each of the four bytes of the Data Output Latch. When LOW, they enable the output buffer of the Data Output

Latch. When HIGH, they force the Data Output Latch buffer into the high impedance state. Any number of bytes of the Data Output Latch is easily activated by separately selecting any of the four enable lines.

$\overline{OE}_{SC}$
Output Enable, Syndrome/Check Bits (Input; Active LOW)

When in the LOW state, the three-state output lines SC_{0-7} are enabled. When this input is HIGH, the syndrome/check bit outputs are in the high-impedance state.

$SC_{0,7}$
Syndrome/Check Bits (Outputs; Three-State)

These eight three-state outputs contain the check/partial check bits when the EDC is in the Generate Mode. They also contain the syndrome/partial-syndrome bits when the device is in the Detect or Detect/Correct Modes.

V_{CC} (2)
+ 5-V Positive Power Supply Voltage

These pins are the positive + 5-V power supply to the EDC Circuit. All V_{CC} pins must be connected during device operation.

FUNCTIONAL DESCRIPTION

EDC Architecture

The Am29C660 EDC Circuit is a powerful 32-bit cascadable slice used for check bit generation, error detection, error correction, and diagnostics.

As shown in the block diagram, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch and Output Buffers
- Diagnostics Latch
- Control Logic

Data Input Latch

The Latch Enable Input, LE_{IN}, controls the loading of 32 bits of data into the Data Input Latch. Depending upon the control mode, the input data is either used for check bit generation or error detection/correction.

Check Bit Input Latch

Eight check bits are loaded under the control of LE_{IN} Check bits are used in the Error Detection and Error Detection/ Correction Modes.

Check Bit Generation Logic

This block generates the appropriate check bits for the 32 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming Code.

Syndrome Generation Logic

In both the Error Detection and Error Detection/Correction Modes, this logic block compares the check bits read from the memory against a newly generated set of check bits produced for the data read in from the memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data and/or check bits is in error.

The syndrome bits are produced by an Exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors), the syndrome bits will be all zeros. If there is a single-bit error, the syndrome bits can be decoded to determine the bit-in-error.

This logic block decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the $\overline{ERROR}$ and $\overline{MULTERROR}$ outputs remain HIGH. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If two or more errors are detected, both $\overline{ERROR}$ and $\overline{MULTERROR}$ go LOW.

Error Correction Logic

For single-bit errors, the Error Correction Logic corrects (by complementing) the single data bit in error. This corrected data is loaded into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single-bit error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to the Generate Mode.

Data Output Latch and Output Buffers

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, $LE_{OUT}/\overline{GENERATE}$. The Data Output Latch may also be directly loaded from the Data Input Latch while in the Pass-Thru Mode.

Four data bytes in the Data Output Latch may be end independently (by $\overline{OE}$ $BYTE_{0-3}$) for reading onto the bidirectional data bus. This feature facilitates byte operations.

Diagnostics Latch

This is a 32-bit latch loadable from the bidirectional data lines under the control of the Diagnostic Latch Enable, LE_{DIAG} The Diagnostic Latch contains check bit information in one byte and control information in the other bytes. The Diagnostic Latch is used for driving the device when in the Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

Control Logic

The Control Logic specifies the mode in which the EDC is operating. Normally, the control logic is driven by the external control inputs. However, in the Internal Control Mode, the control signals are taken from the Diagnostic Latch. Since LE_{OUT} and $\overline{GENERATE}$ are controlled by the same pin, the latching action (LE_{OUT} from HIGH to LOW) of the Data Output Latch causes the EDC to go into the Generate Mode.

Detailed Operational Description

The Am29C660 contains the logic necessary to generate check bits on a 32-bit data field according to a modified Hamming Code. Operating on data read from memory, the EDC will correct any single-bit error, and will detect all double and some triple-bit errors. The Am29C660 may be configured to operate on 32-bit data words (with 7 check bits) and 64-bit data words (with 8 check bits). In either configuration, the device makes the error syndrome bits available on separate outputs for error logging.

Code and Byte Specification

The EDC Circuit may be configured in several different ways, and operates differently in each configuration. It is necessary to indicate to the device what size data word is involved and which bytes of the data word it is processing. This is done with the input lines CODE $ID_{0,1}$ as shown in Table 1. The two modified Hamming codes referred to in Table 1 are:

1. 32/39 Code: 32 data bits, 7 check bits (39 bits in total)

2. 64/72 Code: 64 data bits, 8 check bits (72 bits in total)

Control Mode Selection

There are nine operating modes of the Am29C660. Eight of these modes are selected as shown in Tables 2 and 3. Table 2 is the Diagnostic Mode Control Decode Table, and Table 3 is the Mode Control Decode Table. The Diagnostic Mode pins, DIAG $MODE_{0,1}$, define the five basic areas of operation. $\overline{GENERATE}$ and CORRECT further divide the operations into eight functions. The ninth mode is the Internal Control Mode which is selected by the CODE ID inputs as shown in Table 1.

Table 1. CODE ID Decode

CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	Code 32/39, 32-Bit Data Word
0	1	Internal Control Mode
1	0	Code 64/72, Lower 32-Bit Slice (0-31)
1	1	Code 64/72, Upper 32-Bit Slice (32-63)

Table 2. Diagnostic Mode Control Decode

DIAG $MODE_1$	DIAG $MODE_0$	CORRECT	Diagnostic Mode Selected
0	0	X	Normal EDC Function Mode or Non-Diagnostic Mode
0	1	X	Diagnostic Generate Mode
1	0	X	Diagnostic Detect Mode and Diagnostic Detect/Correct Mode
1	1	1	Initialize Mode
1	1	0	Pass-Thru Mode

Table 3. Mode Control Decode

Operating Mode	DIAG MODE 1	DIAG MODE 0	LEOUT/GENERATE	CORRECT	Contents of Data Output Latch	SC_{0-7} and OEsc = LOW	ERROR and MULT ERROR
Generate	0	0	0	X	*	Check bits generated from Data Input Latch	High
	1	0					
Detect	0	0	1	0	Data Input Latch	Generated from Data Input/Check Bit Latches	Valid
	0	1					
Detect/ Correct	0	0	1	1	Data Input Latch with single bit error detected	Generated from Data Input/Check Bit Latches	Valid
	0	1					
Pass-Thru	1	1	1 or ↓	0	Data Input Latch	Check Bit Latch	HIGH
Diagnostic Generate	0	1	0	X	–	Check bits from Diagnostic Latch	–
Diagnostic Detect	1	0	1	0	Data Input Latch	Data Input check bits from Diagnostic Latch	Valid
Diagnostic Detect/ Correct	1	0	1	1	Data Input Latch with single-bit error detected	Data Input check bits from Diagnostic Latch	Valid
Initialize	1	1	1 or ↓	1	Data Input Latch set to all "0"s	Check bits generated from Data Input Latch	–
Internal Control	CODE $ID_{0,1} = 10$ Control Signals CODE $ID_{0,1}$ DIAG $MODE_{0,1}$ and CORRECT are taken from the Diagnostic Latch						

* In the Generate Mode, data is read into the EDC circuit and the check bits are generated. The same data is written to the memory along with the check bits. Since the Data Output Latch is not used in the Generate Mode, LEOUT, being LOW (since it is tied to Generate) does not affect the writing of check bits.

The Generate Mode is used to display the check bits on the SC_{0-7} outputs. The Error Detect Mode provides an indication of an error or multiple errors on the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs. Single-bit errors are not corrected in this mode. The syndrome bits are provided on the SC_{0-7} outputs. In the Diagnostic Detect Mode, the syndrome bits are generated by comparing the internally generated check bits from the Data Input Latch with check bits stored in the Diagnostic Latch (as opposed to those in the Check Bit Latch).

The Detect/Correct Mode is similar to the Detect Mode except that single-bit errors will be corrected (by complementing) and made available as input to the Data Output Latch. In the Diagnostic Detect/Correct Mode, single-bit errors will be corrected as determined by the syndrome bits, which are in turn generated from the check bits corresponding to the data in the Data Input Latch and the check bits in the Diagnostic Latch.

In the Initialize Mode check bits are generated for all zero data bits. The Data Input Latch is held to a logic zero and is made available as input to the Data Output Latch.

In the Internal Control Mode, the control signals CODE $ID_{0,1}$, DIAG $MODE_{0,1}$, and CORRECT are taken from the Diagnostic Latch and their respective control inputs are disregarded.

Check and Syndrome Bits

The Am29C660 provides either check or syndrome bits on the three-state outputs SC_{0-7}. Check bits are generated from the Data Input Bits. Syndrome bits are an Exclusive-OR of the check bits generated from the data read from the memory and the check bits read from the memory with the stored data.

Syndrome bits can be decoded to determine the single bit-in-error or to indicate a double- or triple-bit error.

The check bits generated by the Am29C660 are designated as follows:

- 32-bit configuration: CX, C0, C1, C2, C4, C8, C16
- 64-bit configuration: CX, C0, C1, C2, C4, C8, C16, C32
- Pin Name: SC_0, SC_1, SC_2, SC_3, SC_4, SC_5, SC_6, SC_7.

The syndrome bits generated by the Am29C660 are designated as follows:

- 32-bit configuration: SX, S0, S1, S2, S4, S8, S16
- 64-bit configuration: SX, S0, S1, S2, S4, S8, S16, S32
- Pin Name: SC_0, SC_1, SC_2, SC_3, SC_4, SC_5, SC_6, SC_7.

32-Bit Word Configuration

Data Field Format

The 32-bit format consists of 32 data bits and 7 check bits and is referred to as the 32/39 code. The format is shown in Figure 1.

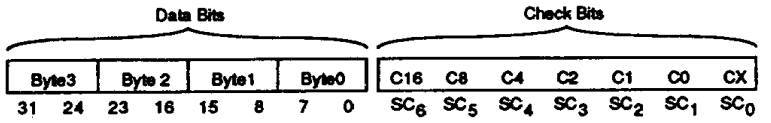


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Figure 1. 32-Bit Data Word Format

Chip Configuration

A single Am29C660 EDC Circuit connected as shown in Figure 2 is all that is necessary to perform single-bit error correction and double-bit error detection on a 32-bit data field. In this configuration, only seven check bits are required. Therefore, CB_7 is a "don't care" and CODE $ID_{0,1} = 00$.

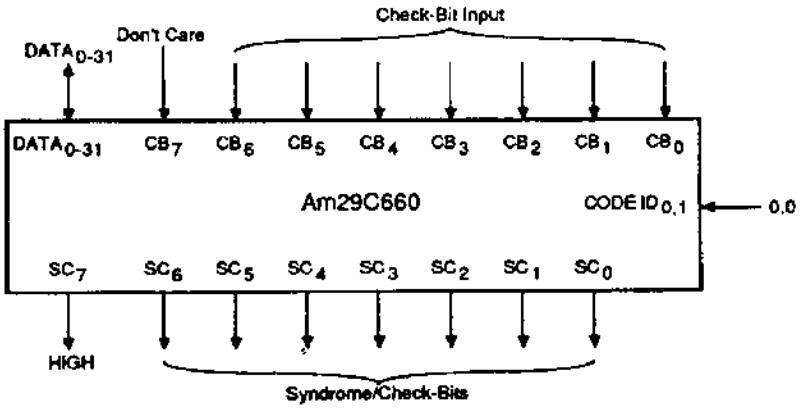

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Figure 2. 32-Bit Configuration

Generate Mode

In this mode, check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs SC_{0-6}. SC_7 is a logic "1" or HIGH.

Check bits are generated according to a modified Hamming Code. Details of the code for check bit generation are shown in Tables 4-1 and 4-2. Check bits are generated as either an XOR or XNOR of 16 of the 32 bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Figure 3 shows the data flow in the Generate Mode.

Table 4-1. 32-Bit Configuration Check Bit Encoding (Data Bits 0–15)

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C_0	Even (XOR)	X	X	X		X		X		X		X		X			
C_1	Odd (XNOR)	X			X	X			X		X	X			X		X
C_2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_8	Even (XOR)									X	X	X	X	X	X	X	X
C_{16}	Even (XOR)	X	X	X	X	X	X	X	X								

Table 4-2. 32-Bit Configuration Check Bit Encoding (Data Bits 16–31)

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C_0	Even (XOR)	X	X	X		X		X		X		X		X			
C_1	Odd (XNOR)	X			X	X			X		X	X			X		X
C_2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_8	Even (XOR)									X	X	X	X	X	X	X	X
C_{16}	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the sixteen data bits noted by an "X" in the table.

Detect Mode

In this mode the device will compare the check bits generated from the contents of the Data Input Latch with the contents of the Check Bit Latch, and will detect all single- and double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULTERROR}}$ and $\overline{\text{ERROR}}$ go LOW. Both error indicators are HIGH if there is no error.

The syndrome bits which are generated during error detection are available on the outputs SC_{0-6}. SC_7 remains HIGH. The syndrome bits may be decoded to determine if a bit error was detected and for a single-bit error, which of the data or check bits is in error. Table 5 shows the syndrome bit decoding for the 32-bit data word configuration. If no error is detected, the syndrome bits will all be zeros (except SC_7 which is tied to a logical "1").

Table 5. Syndrome Bit Decoding Matrix

Syndrome Bits				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* = No errors detected
Number = The bit number of the single bit-in-error
T = Two errors detected
M = More than two errors detected

Detect/Correct Mode

In this mode, the EDC functions the same way as in the Detect Mode except that the correction network is enabled to correct, by complementing, any single-bit error in the Data Input Latch before placing the data on the inputs of the Data Output Latch. If a multiple error is detected, the output of the correction network is undefined. If a single-bit error occurs to a check bit, there is no automatic correction. If a check bit correction is desired, it can be done by placing the device in the Generate Mode to produce the correct check bit sequence for the data in the Data Input Latch.

Pass-Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch, and the contents of the Check bit Latch are placed on the output SC_{0-6} (SC_7 is a logical "1"). $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ are forced HIGH in this mode (inactive).

Diagnostic Generate Mode

This is one of the three special Diagnostic Modes selected by the control inputs DIAG $MODE_{0,1}$. This mode is similar to the normal Generate Mode except that the check bits are not generated from the contents of the Data Input Latch. They are instead taken directly from the contents of the Diagnostic Latch. Table 6 shows the Diagnostic Latch coding format. Figures 5 and 6 illustrate the flow of data during the two diagnostic modes.

Diagnostic Detect, Diagnostic Detect/Correct Modes

These two special Diagnostic Modes are also selected by the control inputs DIAG $MODE_{0,1}$. These modes are similar to the normal Detect and Detect/Correct Modes except that the check bits are taken from the Diagnostic Latch, rather than from the Check Bit Input Latch.

Initialize Mode

In this mode the inputs of the Data Output Latch are forced to all zeros. The syndrome bit outputs SC_{0-6} are generated to correspond to the all-zero data on the Data Output Latch. SC_7 is tied high. The $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs are forced HIGH in this mode. The Initialize Mode is useful after power-up when RAM contents are random. The EDC may be placed in this mode and its outputs written into all memory addresses under processor control.

Internal Control Mode

This mode is selected by the external control inputs CODE ID_{0-1}. When in the Internal Control Mode, the Am29C660 takes the CODE ID_{0-1}, DIAG $MODE_{0-1}$, and CORRECT control signals from the Diagnostic Latch rather than from the external input lines.

Table 6. 32-Bit Diagnostic Latch Coding Format

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	CODE ID_0
9	CODE ID_1
10	DIAG $MODE_0$
11	DIAG $MODE_1$
12	CORRECT
13-31	Don't Care

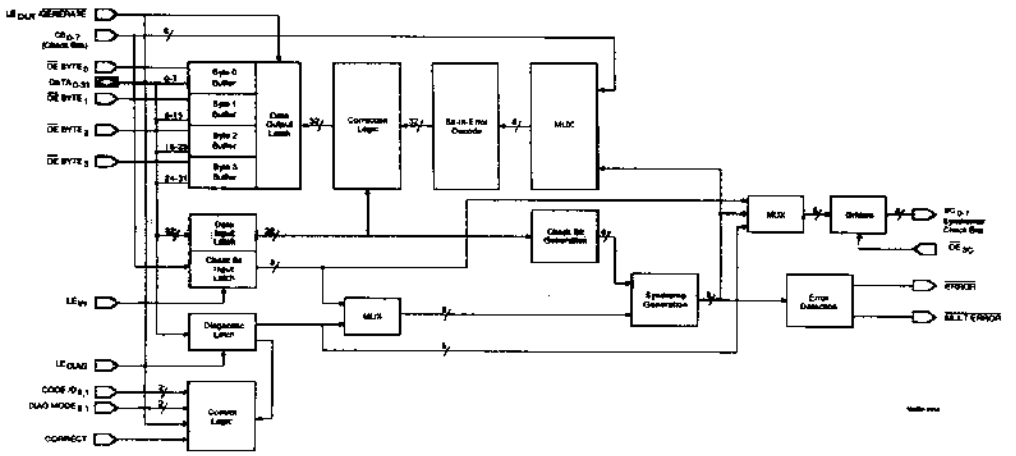

Figure 3. Check Bit Generation Data Path

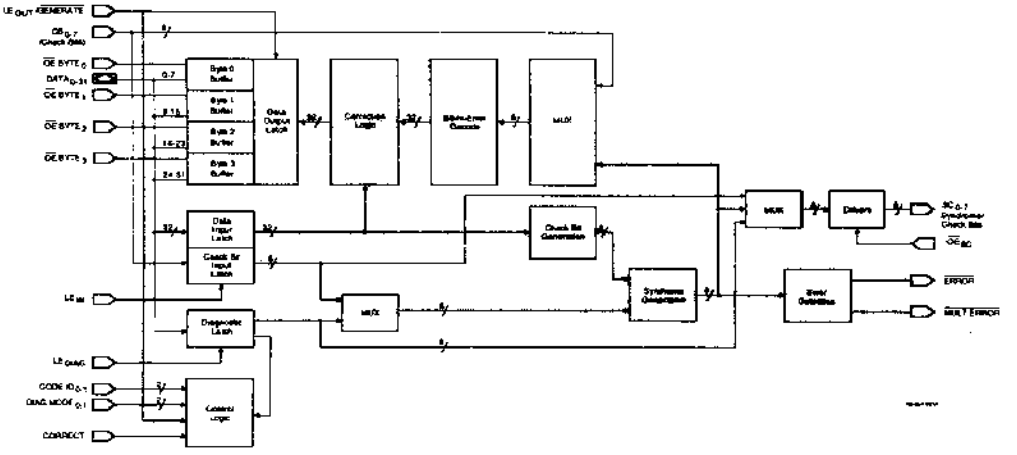

Figure 4. Error Detection and Correction Data Path

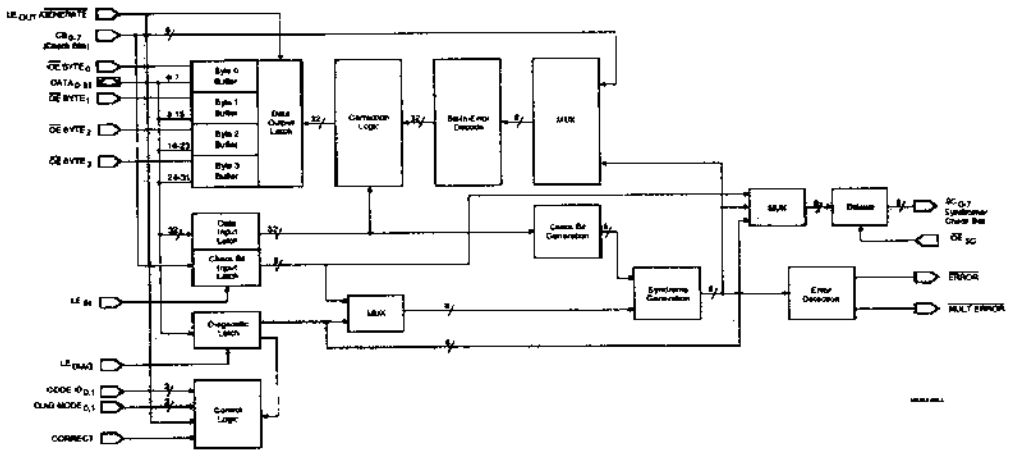

Figure 5. Diagnostic Check Bit Generation Data Path

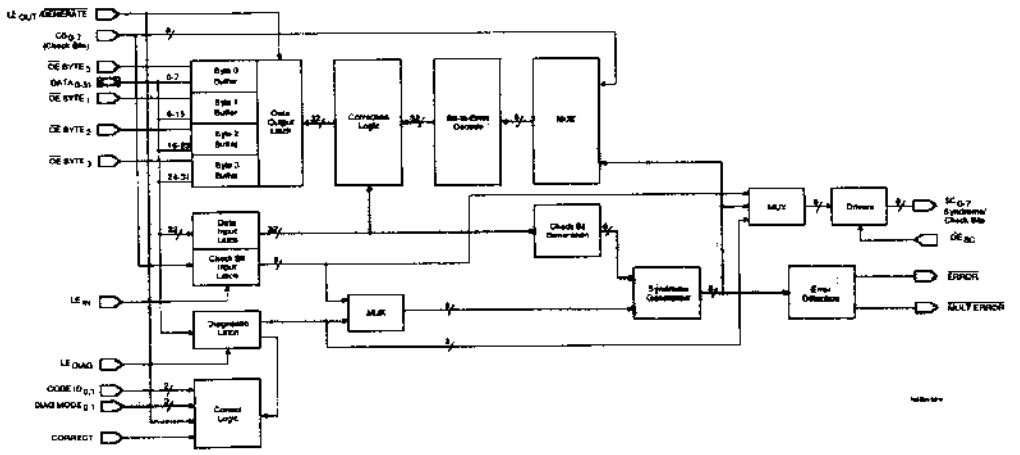

Figure 6. Diagnostic Detect and Correct Data Path

64-Bit Data Word Configuration

Data Field Format

The 64-bit format consists of 64 data bits and 8 check bits and is referred to as the 64/72 code. The format is shown in Figure 7.

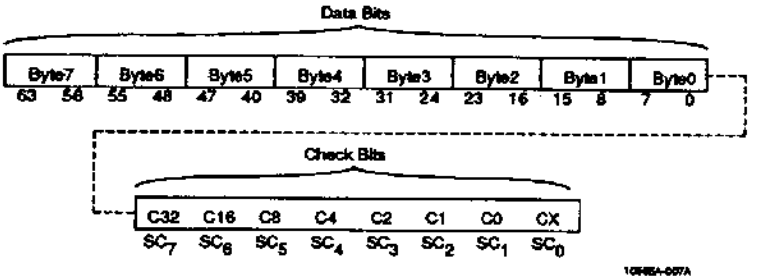

Figure 7. 64-Bit Data Word Format

Chip Configuration

Two Am29C660 EDC Circuits connected as shown in Figure 8, provide all the necessary logic for all single-bit error detection correction, all double-bit error detection, and some triple-bit error detection on a 64-bit data field. In this configuration, eight check bits are required. CODE $ID_{0,1}$ control signal inputs distinguish the upper 32 bits from the lower 32 bits as shown in Table 1.

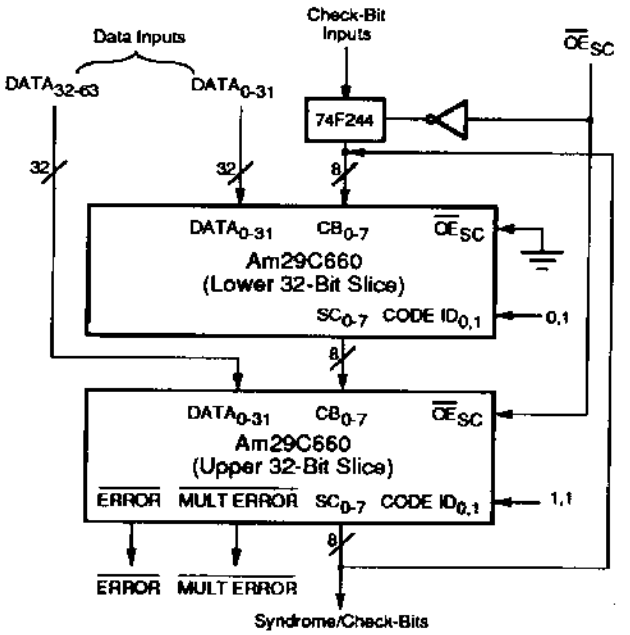

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Figure 8. 64-Bit Configuration

The valid syndrome bits and the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ output signals are taken from the upper EDC slice. The lower EDC slice has its $\overline{OE}_{SC}$ input tied to ground (logic "0") and its SC_{0-7} outputs connected to the respective CB_{0-7} inputs of the upper EDC slice. The 32 most significant data bits, $DATA_{32-63}$, are connected to the data lines of the upper EDC slice. All the latch enables and control signals must be input to both the upper and the lower EDC slices.

In the Detect/Correct Mode, the valid syndrome bits from the upper EDC slice must be read into the lower EDC slice via the check bit inputs of the lower EDC slice. They are selected by an internal MUX as inputs to the bit-in-error decoder (see Block Diagram). External buffering and output enabling of the check bit lines is required as shown in Figure 8. The $\overline{OE}_{SC}$ signal to the upper EDC slice can be used to control the enabling of the check bits to the lower EDC slice. The external check bits to the lower EDC slice are disabled.

Generate Mode

In this mode, check bits will be generated that correspond to the contents of the Data Input Latch. The generated check bits are placed on the SC_{0-7} outputs of the upper EDC slice.

Check bits are generated according to a modified Hamming Code. Details of the code for check bit generation are shown in Tables 7-1 through 7-4. Check bits are generated as either an XOR or XNOR of 32 of the 64 bits. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Table 7-1. 64-Bit Configuration Check Bit Encoding (Data Bits 0–15)

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C_0	Even (XOR)	X	X	X		X		X		X		X		X			
C_1	Odd (XNOR)	X			X	X			X		X	X			X		X
C_2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_8	Even (XOR)									X	X	X	X	X	X	X	X
C_{16}	Even (XOR)	X	X	X	X	X	X	X	X								
C_{32}	Even (XOR)	X	X	X	X	X	X	X	X								

Table 7–2. 64-Bit Configuration Check Bit Encoding (Data Bits 16–31)

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C_0	Even (XOR)	X	X	X		X		X		X		X		X			
C_1	Odd (XNOR)	X			X	X			X		X	X			X		X
C_2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_8	Even (XOR)									X	X	X	X	X	X	X	X
C_{16}	Even (XOR)									X	X	X	X	X	X	X	X
C_{32}	Even (XOR)									X	X	X	X	X	X	X	X

Table 7-3. 64-Bit Configuration Check Bit Encoding (Data Bits 32–47)

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C_0	Even (XOR)	X	X	X		X		X		X		X		X			
C_1	Odd (XNOR)	X			X	X			X		X	X			X		X
C_2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_8	Even (XOR)									X	X	X	X	X	X	X	X
C_{16}	Even (XOR)	X	X	X	X	X	X	X	X								
C_{32}	Even (XOR)									X	X	X	X	X	X	X	X

Table 7-4. 64-Bit Configuration Check Bit Encoding (Data Bits 48–63)

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C_0	Even (XOR)	X	X	X		X		X		X		X		X			
C_1	Odd (XNOR)	X			X	X			X		X	X			X		X
C_2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_8	Even (XOR)									X	X	X	X	X	X	X	X
C_{16}	Even (XOR)									X	X	X	X	X	X	X	X
C_{32}	Even (XOR)	X	X	X	X	X	X	X	X								

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

Detect Mode

In this mode, the device will compare the check bits generated from the contents of the Data Input Latch with the contents of the Check Bit Latch. All single- and double-bit errors and some triple-bit errors will be detected. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ will go LOW. Both error indicators will be HIGH if no errors are detected. The valid $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ signals are from the upper EDC slice.

The syndrome bits which are generated during error detection are available on the outputs SC_{0-7} of the upper EDC slice. The syndrome bits may be decoded to determine if a bit error was detected, and for a single-bit error, which of the data or check bits is in error. Table 8 shows the syndrome bit decoding for the 64-bit data word configuration. If no error is detected, the syndrome bits will all be zeros.

In the Detect Mode, the contents of the Data Input Latch are driven directly into the inputs of the Data Output Latch without correction.

Table 8. 64-Bit Syndrome Bit Decoding Matrix

Syndrome Bits																			
				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																	
0	0	0	0		*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* = No errors detected
Number = The bit number of the single bit-in-error
T = Two errors detected
M = More than two errors detected

Detect/Correct Mode

In this mode, the EDC functions the same way as in the Detect Mode except that the correction network is enabled to correct, by complementing, any single-bit error in the Data Input Latch before placing the data on the inputs of the Data Output Latch. If a multiple error is detected, the output of the correction network is undefined. If a single-bit error occurs to a check bit, there is no automatic correction. If a check bit correction is desired, it can be done by placing the device in the Generate Mode to produce the correct check bit sequence for the data in the Data Input Latch.

For data correction, both the upper EDC slice and the lower EDC slice require access to the syndrome bits SC_{0-7} of the upper EDC slice. the EDC slice has access to these syndrome bits through an internal data path. The syndrome bits must be read through the CB_{0-7} inputs for the lower EDC slice as shown in Figure 8. In the Detect/Correct Mode, the valid SC_{0-7} outputs of the upper EDC slice must be enabled so that they are available for reading in through the CB_{0-7} inputs of the lower EDC slice.

Pass-Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Outpu t Latch, and the contents of the Check bit Latch are placed on the output SC_{0-6} (SC_7 is a logical"1"). $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode (inactive).

Diagnostic Generate Mode

This is one of the three special Diagnostic Modes selected by the control inputs DIAG $MODE_{0,1}$. This mode is similar to the normal Generate Mode except that the check bits are not generated from the contents of the Data Input Latch. They are instead taken directly from the contents of the Diagnostic Latch. Table 9 shows the Diagnostic Latch coding format.

Table 9. 64-Bit Diagnostic Latch Coding Format

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Diagnostic Check Bit 32
8	CODE ID_0, Lower 32-Bit Slice
9	CODE ID_1, Lower 32-Bit Slice
10	DIAG $MODE_0$, Lower 32-Bit Slice
11	DIAG $MODE_1$, Lower 32-Bit Slice
12	CORRECT, Lower 32-Bit Slice
13-31	Don't Care
32-39	Don't Care
40	CODE ID_0, Upper 32-Bit Slice
41	CODE ID_1, Upper 32-Bit Slice
42	DIAG $MODE_0$, Upper 32-Bit Slice
43	DIAG $MODE_1$, Upper 32-Bit Slice
44	CORRECT, Upper 32-Bit Slice
45-63	Don't Care

Diagnostic Detect, Diagnostic Detect /Correct Modes

These two special Diagnostic Modes are also selected by the control inputs DIAG $MODE_{0,1}$. These modes are similar to the normal Detect and Detect/Correct Modes except that the check bits are taken from the Diagnostic Latch, rather than from the Check Bit Input Latch.

Initialize Mode

In this mode the inputs of the Data Output Latch are forced to all zeros. The syndrome bit outputs SC_{0-6} are generated to correspond to the all-zero data on the Data Output Latch. SC_7 is tied high. The $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs are forced HIGH in this mode. The Initialize Mode is useful after power-up when RAM contents are random. The EDC may be placed in this mode and its outputs written into all memory addresses under processor control.

Internal Control Mode

This mode is selected by the external control inputs CODE ID_{0-1}. When in the Internal Control Mode, the Am29C660 takes the CODE ID_{0-1}, DIAG $MODE_{0-1}$, and CORRECT control signals from the Diagnostic Latch rather than from the external input lines.

Table 10. Key AC Calculations For The 64-Bit Configuration

64-Bit Propagation Delay		Component Delays from Am29C660 AC Specifications	Example for Am29C660E
From	To		
$DATA_{0-31}$	Check Bit Outputs	(Data to SC, CODE ID 10) + (Check Bit to SC, CODE ID 11)	11 + 9 = 20 ns
$DATA_{0-31}$	Corrected Data Outputs	(Data to SC, + CODE ID 10) + (Check Bit to SC, CODE ID 11) + (Check Bit to Data, CODE ID 10)	11 + 9 + 10 = 30 ns
$DATA_{0-31}$	Syndrome Outputs	(Data to SC, CODE ID 10) + (Check Bit to SC, CODE ID 11)	11 + 9 = 20 ns
$DATA_{0-31}$	$\overline{ERROR}$ Outputs	(Data to SC, CODE ID 10) + (Check Bit to $\overline{ERROR}$, CODE ID 11)	11 + 7 = 18 ns
$DATA_{0-31}$	$\overline{MULT\ ERROR}$ Outputs	(Data to SC, CODE ID 10) + (Check Bit to $\overline{MULT\ ERROR}$, CODE ID 11)	11 + 9 = 20 ns

APPLICATIONS

System Design Considerations

To obtain optimum performance and maximum design flexibility, AMD's Dynamic Memory Management System has been divided into functional building blocks. For 32-bit error detecting/correcting systems, these building blocks include the Am29C660 EDC Circuit, Am29C668 4M Configurable Dynamic Memory Controller/Driver, and the Am2971A 100-MHz Enhanced Programmable Event Generator or delay lines as the timing reference. Together these chips can perform traditional EDC, Flow-Thru or Fly-By, or AMD's Scrubbing EDC cycle.

High-Performance Parallel Operation

For maximum memory system performance, the EDC should be used in the Check-Only (or Fly-By) configuration shown in Figure 9. With this configuration, the memory system operates as fast with EDC as it would without.

On reads from memory, data is read out from the DRAMs directly to the data bus (same as in a non-EDC system). At the same time, the data is read into the EDC to check for errors. If an error exists, the EDC's error flags ($\overline{ERROR}$, $\overline{MULT\ ERROR}$) are used to interrupt the CPU and/or to stretch the memory cycle. If no error is detected, no slowdown is required.

If an error is detected, the EDC generates corrected data for the processor. At the designer's option, the correct data may be written back into memory; error logging and diagnostic routines may also be run under processor control.

The Check-Only configuration allows data reads to proceed as fast with EDC as without. Only if an error is detected is there any slowdown, but even if the memory system had an error every hour this would mean only one error every 3 – 4 billion memory cycles. Therefore, even with a very high error rate, EDC in a Check-Only configuration has essentially zero impact on memory system speed.

On writes to memory, check bits must be generated before the full memory word can be written into memory. Using the Am29C983 Multiple Bus Exchange allows the data word to be buffered on the memory board while check bits are generated. This makes the check bit generate time transparent to the processor.

EDC in the Data Path

The simplest configuration for the Am29C660 is to have the EDC circuit directly in the data path, as shown in Figure 10 (Flow-Thru configuration). In this configuration, data read from memory is always corrected prior to putting the data on the data bus. The advantages are simpler operation and no need for mid-cycle interrupts. The disadvantage is that memory system speed is slowed by the amount of time it takes for error correction on every cycle.

Usually the Flow-Thru configuration will be used with MOS microprocessors which have ample memory timing budgets. Most high-performance processors will use the high-performance parallel configuration shown in Figure 9 (Fly-By).

Memory Scrubbing During Refresh

Scrubbing is an error correction technique that examines the entire memory during system refresh cycles, thus causing little or no impact on performance yet providing high data reliability since errors cannot accumulate.

Single-bit errors are by far the most common in a dynamic memory system, and are always correctable by the EDC. Double-bit errors occur far less frequently than single-bit errors (100-to-1 or greater) and are always detected by the EDC, but not corrected.

In a memory system, soft errors occur only one at a time. A double-bit error in a data word occurs when a single soft error is left uncorrected and is followed by another error in the data word within hours, days, or weeks after the first occurrence.

Scrubbing the memory periodically avoids almost all double-bit errors. In the scrubbing operation, every data word in memory is periodically checked by the EDC for single-bit errors. If one is found, it is corrected and the correct data word is written back into memory. Errors are not allowed to accumulate, and thus most double-bit errors are avoided.

The scrubbing operation is generally done as a background routine when the memory is not being used by the processor. If memory is scrubbed frequently, errors that are detected and corrected during processor accesses need not be immediately written back into memory. Instead, the error will be corrected in memory during scrubbing. This reduces the time delay involved in a processor access of an incorrect memory word.

On each refresh-with-scrub cycle, one memory location is read, checked for errors, and if necessary, corrected before being written back into memory. For a sixteen-megaword memory (2^{24} locations) with one refresh every 16 microseconds, the AMD Memory Management chip set will scrub the entire memory of single-bit errors every minute. If multiple-bit errors are encountered during a scrub cycle, $\overline{WE}$ is suppressed.

With the occurrence of an error, a read/modify/write (R/M/W) cycle is performed. The duration of a R/M/W cycle is typically longer than a normal read or write cycle. During refresh operations, a row in each bank is accessed by energizing the $\overline{RAS}$ line. This refreshes all the locations in that row. If an error is detected, a write operation is performed in that bank at the location of the error. This is accomplished by energizing the $\overline{CAS}$ line in that bank for that location. The entire checking operation is performed within the refresh cycle. A wait state may need to be issued to extend the cycle should an error be discovered. However, the system reliability will be increased because soft errors will not be able to accumulate in areas of memory that are not frequently accessed.

When performing refresh without scrubbing, all four $\overline{RAS}$ lines go LOW but the $\overline{CAS}$ lines remain HIGH or inactive. A refresh with scrubbing will activate all four $\overline{RAS}$ lines as before and a single $\overline{CAS}$ line. Errors that are detected during scrubbing cycles do not cause interrupts or bus-error ($\overline{BERR}$) signal assertions.

Figure 11 shows a sixteen-megaword memory system with error detection and correction.

Check Bit Correction

The EDC detects single bit errors whether the error is a data bit or a check bit. Data bit errors are automatically corrected by the EDC. To generate corrected check bits once a single check bit error is detected, the EDC need only be switched to GENERATE mode (data in the DATA INPUT LATCH is valid).

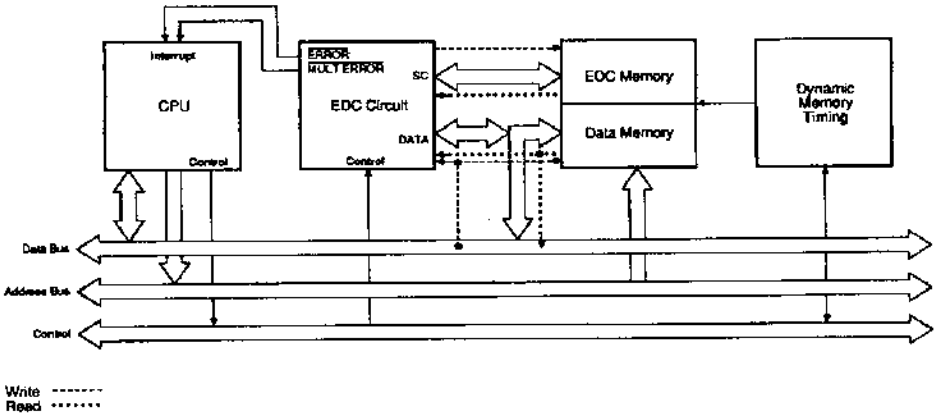
The syndromes generated by the EDC may be decoded to determine whether the single bit error is a check bit.

In many memory systems, a check bit error will be ignored on the memory read and corrected during a periodic "scrubbing" of memory (see section in System Design Considerations).

Multiple Errors

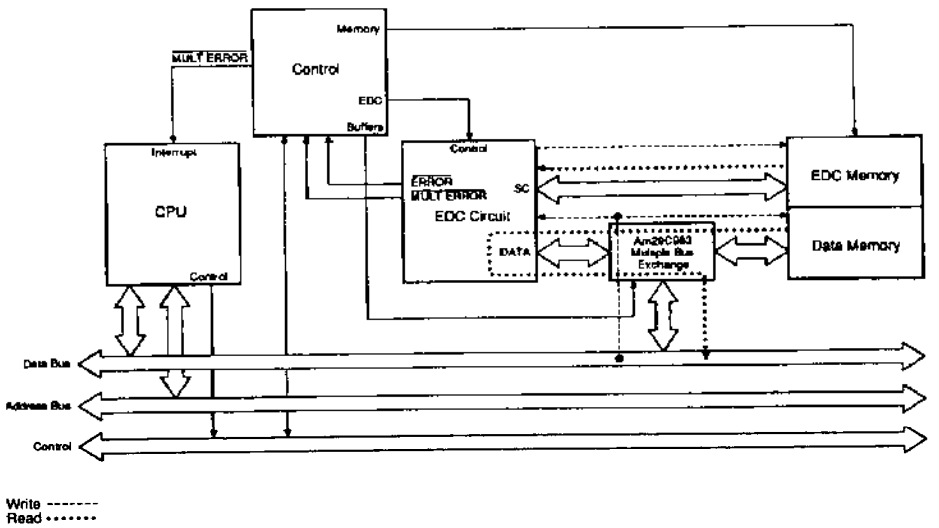
The bit-in-error decode logic uses syndrome bit S0 through S32 to correct errors, SX is only used in developing the multiple error signal. This means that some multiple errors will cause a data bit to be inverted.

For example, in the 16-bit mode if data bits 8 and 13 are in error the syndrome 111100 (SX, S0, S1, S4, S8) is produced. This is flagged a double error by the error detection logic, but the bit-in-error decoder only receives syndrome 11100 (S0, S1, S2, S4, S8), which it decodes as a single error in data bit 0 and inverts that bit. If it is desired to inhibit this version the multiple error output may be connected to the correct input as in Figure 13. This will inhibit correction when a multiple error occurs. Extra time delay may be introduced in the data to correct data path when this is done.



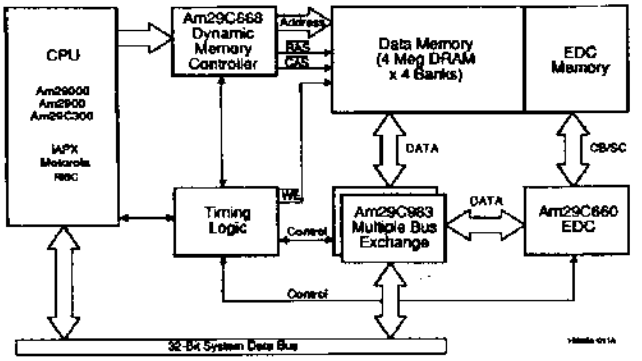
10565-009A

Figure 9. Check-Only Configuration



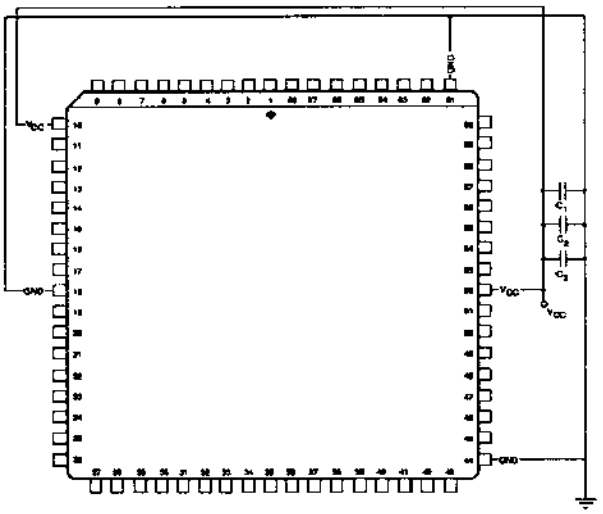
10565-010A

Figure 10. Correct-Always Configuration



10565-011A

Figure 11. Sixteen-Megaword Memory System with EDC



10565-012A

Note:

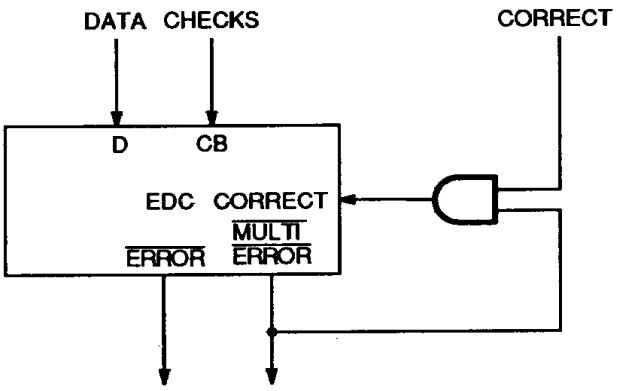
$C_1 = 1.0\mu F$, $C_2 = 0.1\mu F$, $C_3 = 0.01\mu F$.

The C_1, C_2, C_3 capacitors should be used to shunt low- and high-frequency noise from V_{CC}. Do not replace with one capacitor. Place capacitors as close to the device as possible.

Figure 12. Device Decoupling-V_{CC} and Ground Pin Connections

Table 11. 32-Bit Word/Check Bit Examples

Example 32-Bit Word								Corresponding Check Bits	
D_{31}							D_0	C_X	C_{16}
0101	0101	0101	0101	0101	0101	0101	0101	0011000	
1010	1010	1010	1010	1010	1010	1010	1010	0011000	
0001	0000	1100	0111	0111	1101	0111	1111	1101110	
0000	0011	0011	1101	1000	0101	0100	0000	1110011	
1111	1111	1111	0000	0000	0000	1111	1110	0101001	



10565-013A

Figure 13. Inhibition of Data Modification

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65 to +150°C

Temperature (Case)

Under Bias . . . . . –55 to +125°C

Supply Voltage to Ground Potential

Continous . . . . . –0.5 to +7.0 V

DC Voltage Applied to Outputs For

HIGH Output State . . . . . –0.5 V to V_{CC} Max.

DC Input Voltage . . . . . –0.5 to +5.5 V

DC Input Current . . . . . –30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) 0 to + 70°C

Supply Voltage . . . . . +4.75 to +5.25 V

Military (M) Devices

Case Temperature (T_C) . . . . . –55 to +125°C

Supply Voltage . . . . . +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND			−5.0	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −300 µA	V_{CC}−0.2		V
			MIL I_{OH} = −8 mA	2.4		
			COM'L I_{OH} = −15 mA	2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300 µA		0.2	V
			MIL I_{OL} = 8 mA		0.5	
			COM'L I_{OL} = 15 mA		0.5	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = Max.	V_O = 0 V		−10	µA
			V_O = V_{CC} (Max.)		10	
I_{OS}	Output Short-Circuit Current	V_{CC} = Min., V_O = 0 V (Note 2)		−30		mA
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max., V_{CC}−0.2 V ≤ V_{IN}, V_{IN} ≤ 0.2V, f_{OP} = 0			5.0	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL HIGH) (Note 4)	V_{CC} = Max., V_{IN} = 3.4 V, f_{OP} = 0			0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max., V_{CC}−0.2 V ≤ V_{IN}, V_{IN} ≤ 0.2 V, Outputs Open, $\overline{OE}$ = LOW	MIL		6.5	mA/ MHz
			COM'L		6	
I_{CC}	Total Power Supply Current (Note 5)	V_{CC} = Max., f_{OP} = 10 MHz, Outputs open, $\overline{OE}$ = LOW, 50% Duty cycle, V_{CC}−0.2 V ≤ V_{IN}, V_{IN} ≤ 0.2 V	MIL		70	mA
			COM'L		65	
		V_{CC} = Max., f_{OP} = 10 MHz, Outputs open, $\overline{OE}$ = LOW, 50% Duty cycle, V_{IH} = 3.4 V, V_{IL} = 0.4 V	MIL		70	
			COM'L		65	

Notes:
1. For conditions shown as Min. or Max., use appropriate value specified under Operating Range for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
3. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
4. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4 V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
5. Total Power Supply Current is the sum of the Quiescent Current and the Dynamic Current (at either CMOS or TTL input levels). For all conditions, the Total Power Supply Current can calculated by using the following equation:

$$I_{CC} = I_{CCQ} + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{OP})$$

D_H = Data duty cycle TTL HIGH period (V_{IN} = 3.4 V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{OP} = Operating frequency in Megahertz.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typical	Unit
C_{IN} (CB)	Input Capacitance (CB)	TA = 25°C	5	pF
C_{OUT} (SC)	Output Capacitance (SC)	f = 1 MHz	6	pF
$C_{I/O}$ (Data)	I/O Capacitance		6	pF

Note:
1. These parameters are not tested in production and are not guaranteed, but are evaluated at initial characterization and at any time the design is modified where capacitance may be effected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Notes 1 and 2)

The following table specifies the guaranteed device performance over the Commercial operating range of 0°C to +70°C (ambient), with V_{CC} 4.75 to 5.25 V. All input switching is between 0 V and 3 V at 1 V/ns, and measurements are made at 1.5 V. All outputs have maximum DC load. All units are in nanoseconds (ns).

No.		Parameter Symbol	Data Path Description		Am29C660		Am29C660A		Am29C660B		Am29C660C	
			From Input	To Output	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1	A	t_{PD}	$DATA_{0-31}$ (Note 3)	SC_{0-7}		37		27		25		18
	B			$DATA_{0-31}$ (Note 2)		49		36		30		24
	C			$\overline{ERROR}$		40		30		25		16
	D			$\overline{MULT\ ERROR}$		45		33		27		20
2	A	t_{PD}	CB_{0-7} (CODE ID 00, 11)	SC_{0-7}		22		16		14		14
	B			$DATA_{0-31}$		46		34		30		21
	C			$\overline{ERROR}$		26		19		17		13
	D			$\overline{MULT\ ERROR}$		31		23		20		16
3	A	t_{PD}	CB_{0-7} (CODE ID 10)	SC_{0-7}		22		16		16		15
	B			$DATA_{0-31}$		30		20		18		16
4	A	t_{PD}	$\overline{GENERATE}$	SC_{0-7}		29		21		21		18
	B			$\overline{ERROR}$		30		25		23		9
	C			$\overline{MULT\ ERROR}$		30		25		23		11
5		t_{PD}	CORRECT (Not Internal Control Mode)	$DATA_{0-31}$		31		23		23		16
6	A	t_{PD}	$DIAG\ MODE_{0,1}$ (Not Internal Control Mode)	SC_{0-7}		23		17		17		16
	B			$DATA_{0-31}$		35		26		26		26
	C			$\overline{ERROR}$		27		20		20		11
	D			$\overline{MULT\ ERROR}$		33		24		24		20
7	A	t_{PD}	$CODE\ ID_{0,1}$	SC_{0-7}		25		18		18		18
	B			$DATA_{0-31}$		35		26		26		23
	C			$\overline{ERROR}$		29		21		21		17
	D			$\overline{MULT\ ERROR}$		35		26		26		21
8	A	t_{PD}	LE_{IN} (From Latched to Transparent)	SC_{0-7}		37		27		27		22
	B			$DATA_{0-31}$		51		38		38		28
	C			$\overline{ERROR}$		41		30		30		19
	D			$\overline{MULT\ ERROR}$		45		33		33		22
9		t_{PD}	LE_{OUT} (From Latched to Transparent)	$DATA_{0-31}$		17		12		12		12
10	A	t_{PD}	LE_{DIAG} (From Latched to Transparent; Not Internal Control Mode)	SC_{0-7}		21		15		15		15
	B			$DATA_{0-31}$		38		29		29		24
	C			$\overline{ERROR}$		26		19		19		15
	D			$\overline{MULT\ ERROR}$		30		22		22		19

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

No.		Parameter Symbol	Data Path Description		Am29C660		Am29C660A		Am29C660B		Am29C660C	
			From Input	To Output	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
11	A	t_{PD}	Internal Control Mode: LE DIAG (From Latched to Transparent)	SC_{0-7}		22		16		16		16
	B			$DATA_{0-31}$		42		32		32		22
	C			$\overline{ERROR}$		26		19		19		16
	D			$\overline{MULT\ ERROR}$		33		24		24		18
12	A	t_{PD}	Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	SC_{0-7}		22		16		16		16
	B			$DATA_{0-31}$ (Note 2)		42		32		32		25
	C			$\overline{ERROR}$		27		20		20		13
	D			$\overline{MULT\ ERROR}$		34		25		25		16
13		t_{SET}	$DATA_{0-31}$ (Note 4)	LE_{IN}	6		5		4		3	
14		t_{HOLD}			4		4		4		4	
15		t_{SET}	CB_{0-7} (Note 4)		5		5		4		2	
16		t_{HOLD}			4		4		4		4	
17		t_{SET}	$DATA_{0-31}$ (Note 4)	LE_{OUT}	30		23		19		6	
18		t_{HOLD}			0		0		0		0	
19		t_{SET}	CB_{0-7} (Note 4) (CODE ID 00, 11)		20		15		15		8	
20		t_{HOLD}			0		0		0		0	
21		t_{SET}	CB_{0-7} (Note 4) (CODE ID 10)		20		15		15		14	
22		t_{HOLD}			0		0		0		0	
23		t_{SET}	CORRECT (Note 4)		16		11		11		8	
24		t_{HOLD}			0		0		0		0	
25		t_{SET}	DIAG $MODE_{0,1}$ (Note 4)		23		17		17		17	
26		t_{HOLD}			0		0		0		0	
27		t_{SET}	CODE $ID_{0,1}$ (Note 4)		23		17		17		10	
28		t_{HOLD}			0		0		0		0	
29		t_{SET}	LE_{IN} (Note 4)		31		25		20		19	
30		t_{HOLD}			0		0		0		0	
31		t_{SET}	$DATA_{0-31}$ (Note 4)	LE_{DIAG}	6		5		4		3	
32		t_{HOLD}			3		3		3		3	
33		t_{EN}	$\overline{OE}$ BYTE$_{0-3}$ (Note 5)	$DATA_{0-31}$		27		23		23		8
34		t_{DIS}				23		19		19		11
35		t_{EN}	$\overline{OE}$ SC (Note 5)	SC_{0-7}		28		24		24		17
36		t_{DIS}				24		20		20		13
37		t_{PW}	Minimum Pulse Width: LE_{IN}, LE_{OUT}, LE_{DIAG}		12		9		9		6	

Notes:

1. C_L = 50 pF.
2. Certain parameters are combinational propagation delay calculations.
3. Data In or LE_{IN} to Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Setup and Hold times relative to Latch Enables (Latching up data).
5. Output disable tests specified with C_L = 5 pF and measured to 0.5 V change of output voltage level. Testing is performed at C_L = 50 pF and correlated to C_L = 5 pF.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Notes 1 and 2)

No.		Parameter Symbol	Data Path Description		Am29C660D		PRELIMINARY Am29C660E		Unit
			From Input	To Output	Min.	Max.	Min.	Max.	
1	A	t_{PD}	$DATA_{0-31}$ (Note 3)	SC_{0-7}		14		11	ns
	B			$DATA_{0-31}$ (Note 2)		18		14	ns
	C			$\overline{ERROR}$		12		9	ns
	D			$\overline{MULT\ ERROR}$		15		12	ns
2	A	t_{PD}	CB_{0-7} (CODE ID 00, 11)	SC_{0-7}		11		9	ns
	B			$DATA_{0-31}$		16		12	ns
	C			$\overline{ERROR}$		10		7	ns
	D			$\overline{MULT\ ERROR}$		12		9	ns
3	A	t_{PD}	CB_{0-7} (CODE ID 10)	SC_{0-7}		12		9	ns
	B			$DATA_{0-31}$		12		10	ns
4	A	t_{PD}	$\overline{GENERATE}$	SC_{0-7}		14		12	ns
	B			$\overline{ERROR}$		7		6	ns
	C			$\overline{MULT\ ERROR}$		8		7	ns
5		t_{PD}	CORRECT (Not Internal Control Mode)	$DATA_{0-31}$		12		10	ns
6	A	t_{PD}	DIAG $MODE_{0,1}$ (Not Internal Control Mode)	SC_{0-7}		12		11	ns
	B			$DATA_{0-31}$		20		15	ns
	C			$\overline{ERROR}$		10		8	ns
	D			$\overline{MULT\ ERROR}$		15		14	ns
7	A	t_{PD}	CODE $ID_{0,1}$	SC_{0-7}		14		12	ns
	B			$DATA_{0-31}$		18		14	ns
	C			$\overline{ERROR}$		13		12	ns
	D			$\overline{MULT\ ERROR}$		16		15	ns
8	A	t_{PD}	LE_{IN} (From Latched toTransparent)	SC_{0-7}		17		15	ns
	B			$DATA_{0-31}$ (Note 2)		21		17	ns
	C			$\overline{ERROR}$		14		12	ns
	D			$\overline{MULT\ ERROR}$		17		13	ns
9		t_{PD}	LE_{OUT} (From Latched toTransparent)	$DATA_{0-31}$		9		8	ns
10	A	t_{PD}	LE_{DIAG} (From Latched to Transparent; Not Internal Control Mode)	SC_{0-7}		12		11	ns
	B			$DATA_{0-31}$		18		14	ns
	C			$\overline{ERROR}$		12		11	ns
	D			$\overline{MULT\ ERROR}$		14		12	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

No.		Parameter Symbol	Data Path Description		Am29C660D		PRELIMINARY Am29C660E		Unit
			From Input	To Output	Min.	Max.	Min.	Max.	
11	A	t_{PD}	Internal Control Mode: LE_{DIAG} (From Latched to Transparent)	SC_{0-7}		12		11	ns
	B			$DATA_{0-31}$		17		14	ns
	C			$\overline{ERROR}$		12		10	ns
	D			$\overline{MULT\ ERROR}$		14		12	ns
12	A	t_{PD}	Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	SC_{0-7}		12		10	ns
	B			$DATA_{0-31}$ (Note 2)		19		15	ns
	C			$\overline{ERROR}$		10		9	ns
	D			$\overline{MULT\ ERROR}$		12		11	ns
13		t_{SET}	$DATA_{0-31}$ (Note 4)	LE_{IN}	3		3		ns
14		t_{HOLD}			3		3		ns
15		t_{SET}	CB_{0-7} (Note 4)		2		2		ns
16		t_{HOLD}			3		3		ns
17		t_{SET}	$DATA_{0-31}$ (Note 4)	LE_{OUT}	5		5		ns
18		t_{HOLD}			0		0		ns
19		t_{SET}	CB_{0-7} (Note 4) (CODE ID 00, 11)		11		11		ns
20		t_{HOLD}			0		0		ns
21		t_{SET}	CB_{0-7} (Note 4) (CODE ID 10)		6		6		ns
22		t_{HOLD}			0		0		ns
23		t_{SET}	CORRECT (Note 4)		6		6		ns
24		t_{HOLD}			0		0		ns
25		t_{SET}	$DIAG\ MODE_{0,1}$ (Note 4)		13		13		ns
26		t_{HOLD}			0		0		ns
27		t_{SET}	$CODE\ ID_{0,1}$ (Note 4)		8		8		ns
28		t_{HOLD}			0		0		ns
29		t_{SET}	LE_{IN} (Note 4)		14		14		ns
30		t_{HOLD}			0		0		ns
31		t_{SET}	$DATA_{0-31}$ (Note 4)	LE_{DIAG}	3		3		ns
32		t_{HOLD}			3		3		ns
33		t_{EN}	$\overline{OE}\ BYTE_{0-3}$ (Note 5)	$DATA_{0-31}$		7	2	5	ns
34		t_{DIS}				8	2	8	ns
35		t_{EN}	$\overline{OE}_{SC}$ (Note 5)	SC_{0-7}		8	2	5	ns
36		t_{DIS}				10	2	8	ns
37		t_{PW}	Minimum Pulse Width: LE_{IN}, LE_{OUT}, LE_{DIAG}		5		5		ns

Notes:

1. C_L = 50 pF.
2. Certain parameters are combinational propagation delay calculations.
3. Data In or LE_{IN} to Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Setup and Hold times relative to Latch Enables (Latching up data).
5. Output disable tests specified with C_L = 5 pF and measured to 0.5 V change of output voltage level. Testing is performed at C_L = 50 pF and correlated to C_L = 5 pF.

SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 1 and 2)

The following table specifies the guaranteed device performance over the Military and Extended–Commercial operating ranges of – 55°C to + 125°C (case), with Vcc 4.5 to 5.5 V and 4.75 to 5.25 V, respectively. All input switching is between 0 V and 3 V at 1 V/ns and measurements are made at 1.5 V. All outputs have maximum DC load. All units are in nanoseconds (ns).

No.		Parameter Symbol	Data Path Description		Am29C660C	
			From Input	To Output	Min.	Max.
1	A	t_{PD}	$DATA_{0-31}$ (Note 3)	SC_{0-7}		22
	B			$DATA_{0-31}$ (Note 2)		29
	C			$\overline{ERROR}$		21
	D			$\overline{MULT\ ERROR}$		24
2	A	t_{PD}	CB_{0-7} (CODE ID 00, 11)	SC_{0-7}		17
	B			$DATA_{0-31}$		23
	C			$\overline{ERROR}$		16
	D			$\overline{MULT\ ERROR}$		18
3	A	t_{PD}	CB_{0-7} (CODE ID 10)	SC_{0-7}		17
	B			$DATA_{0-31}$		18
4	A	t_{PD}	$\overline{GENERATE}$	SC_{0-7}		20
	B			$\overline{ERROR}$		10
	C			$\overline{MULT\ ERROR}$		12
5		t_{PD}	CORRECT (Not Internal Control Mode)	$DATA_{0-31}$		17
6	A	t_{PD}	$DIAG\ MODE_{0,1}$ (Not Internal Control Mode)	SC_{0-7}		18
	B			$DATA_{0-31}$		29
	C			$\overline{ERROR}$		12
	D			$\overline{MULT\ ERROR}$		23
7	A	t_{PD}	$CODE\ ID_{0,1}$	SC_{0-7}		21
	B			$DATA_{0-31}$		26
	C			$\overline{ERROR}$		20
	D			$\overline{MULT\ ERROR}$		24
8	A	t_{PD}	LE_{IN} (From Latched toTransparent)	SC_{0-7}		24
	B			$DATA_{0-31}$		32
	C			$\overline{ERROR}$		21
	D			$\overline{MULT\ ERROR}$		25
9		t_{PD}	LE_{OUT} (From Latched to Transparent)	$DATA_{0-31}$		13
10	A	t_{PD}	LE_{DIAG} (From Latched to Transparent; Not Internal Control Mode)	SC_{0-7}		18
	B			$DATA_{0-31}$		27
	C			$\overline{ERROR}$		17
	D			$\overline{MULT\ ERROR}$		21

SWITCHING CHARACTERISTICS over MILITARY operating range (Continued)

No		Parameter Symbol	Data Path Description		Am29C660C	
			From Input	To Output	Min.	Max.
11	A	t_{PD}	Internal Control Mode: LE_{DIAG} (From Latched to Transparent)	SC_{0-7}		19
	B			$DATA_{0-31}$		25
	C			$\overline{ERROR}$		18
	D			$\overline{MULT\ ERROR}$		21
12	A	t_{PD}	Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	SC_{0-7}		18
	B			$DATA_{0-31}$ (Note 2)		29
	C			$\overline{ERROR}$		14
	D			$\overline{MULT\ ERROR}$		18
13		t_{SET}	$DATA_{0-31}$ (Note 4)		3	
14		t_{HOLD}		LE_{IN}	4	
15		t_{SET}	CB_{0-7} (Note 4)		2	
16		t_{HOLD}			4	
17		t_{SET}	$DATA_{0-31}$ (Note 4)		7	
18		t_{HOLD}			0	
19		t_{SET}	CB_{0-7} (Note 4) (CODE ID 00, 11)		10	
20		t_{HOLD}			0	
21		t_{SET}	CB_{0-7} (Note 4) (CODE ID 10)		10	
22		t_{HOLD}			0	
23		t_{SET}	CORRECT (Note 4)	LE_{OUT}	9	
24		t_{HOLD}			0	
25		t_{SET}	$DIAG\ MODE_{0,1}$ (Note 4)		19	
26		t_{HOLD}			0	
27		t_{SET}	$CODE\ ID_{0,1}$ (Note 4)		12	
28		t_{HOLD}			0	
29		t_{SET}	LE_{IN} (Note 4)		21	
30		t_{HOLD}			0	
31		t_{SET}	$DATA_{0-31}$ (Note 4)	LE_{DIAG}	3	
32		t_{HOLD}			3	
33		t_{EN}	$\overline{OE}\ BYTE_{0-3}$ (Note 5)	$DATA_{0-31}$		17
34		t_{DIS}				15
35		t_{EN}	$\overline{OE}_{SC}$ (Note 5)	SC_{0-7}		18
36		t_{DIS}				15
37		t_{PW}	Minimum Pulse Width: LE_{IN}, LE_{OUT}, LE_{DIAG}		6	

Notes:

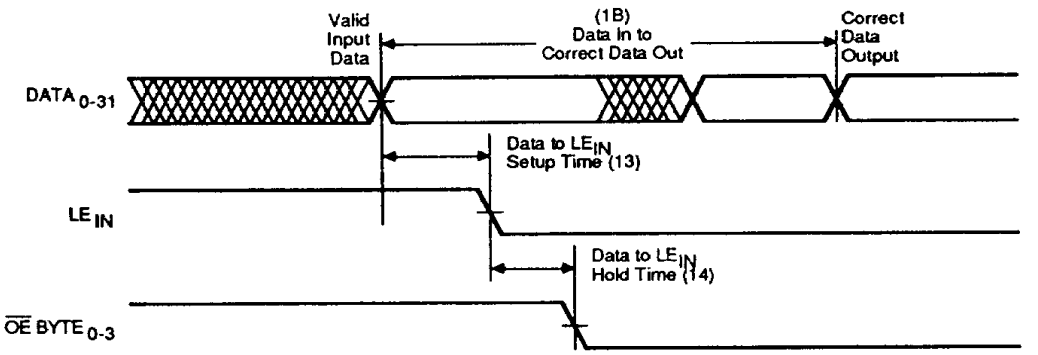
1. $C_L = 50$ pF.
2. Certain parameters are combinational propagation delay calculations.
3. Data In or LE_{IN} to Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Setup and Hold times relative to Latch Enables (Latching up data).
5. Output disable tests specified with $C_L = 5$ pF and measured to 0.5 V change of output voltage level. Testing is performed at $C_L = 50$ pF and correlated to $C_L = 5$ pF.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

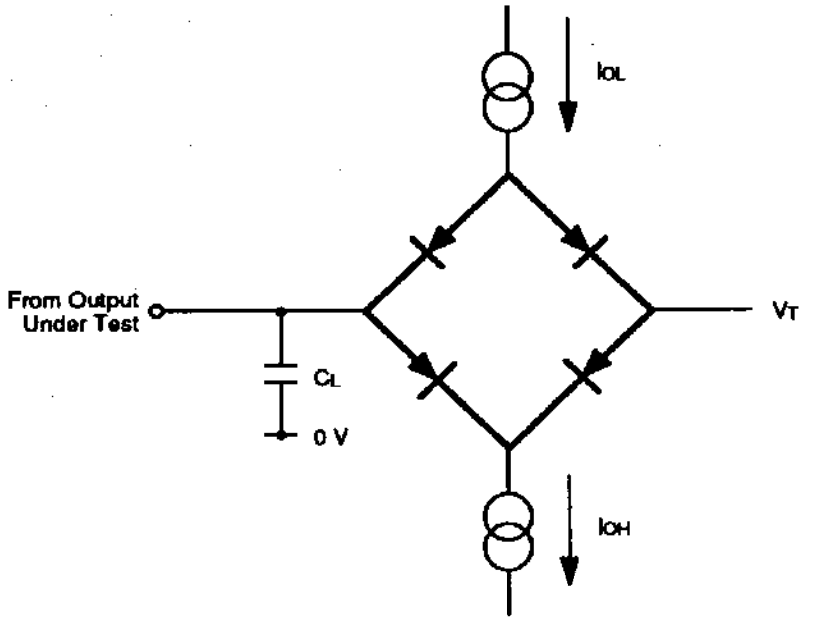
SWITCHING WAVEFORM



10565-017A

DATA$_{0-31}$/LE$_{IN}$ to Correct Data Out

SWITCHING TEST CIRCUIT

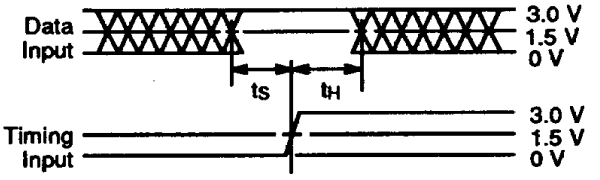


10565C-012A

Notes:

1. C_L = 50 pF for all tests except output enable/disable (includes scope probe, wiring and stray capacitance without device in test fixture).
2. C_L = 5 pF for output enable/disable tests
3. V_T = 1.5 V.

SWITCHING TEST WAVEFORMS

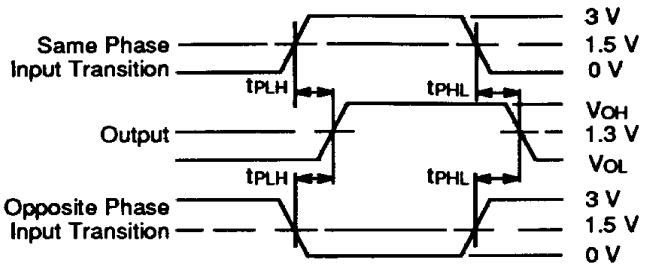


10565C-013A

Notes:

1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

Setup and Hold Times



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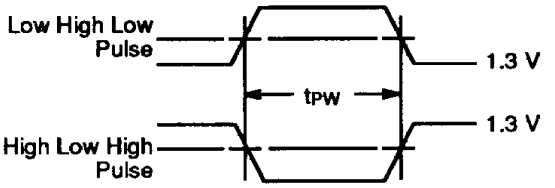
Propagation Delay



01767-010A

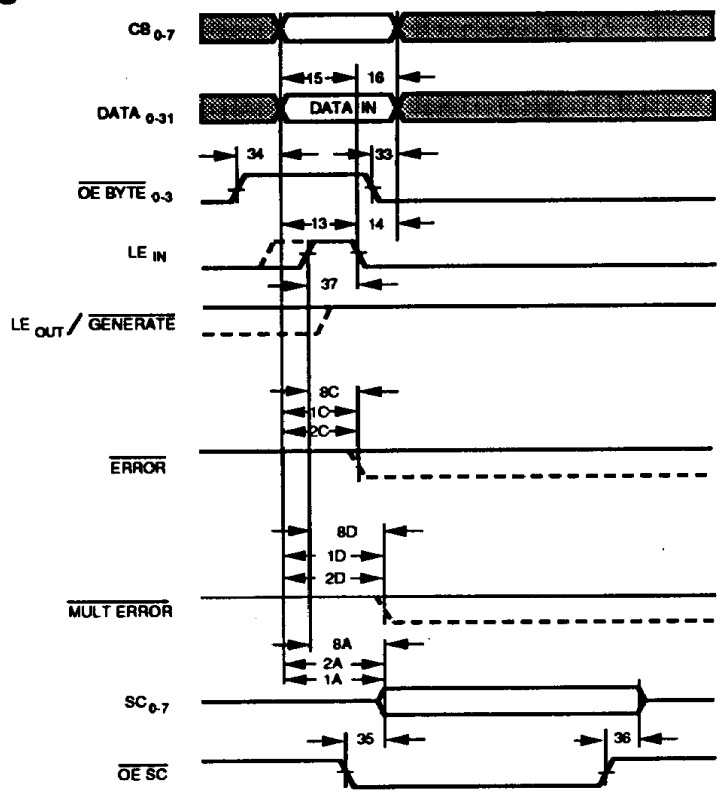
Pulse Width

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

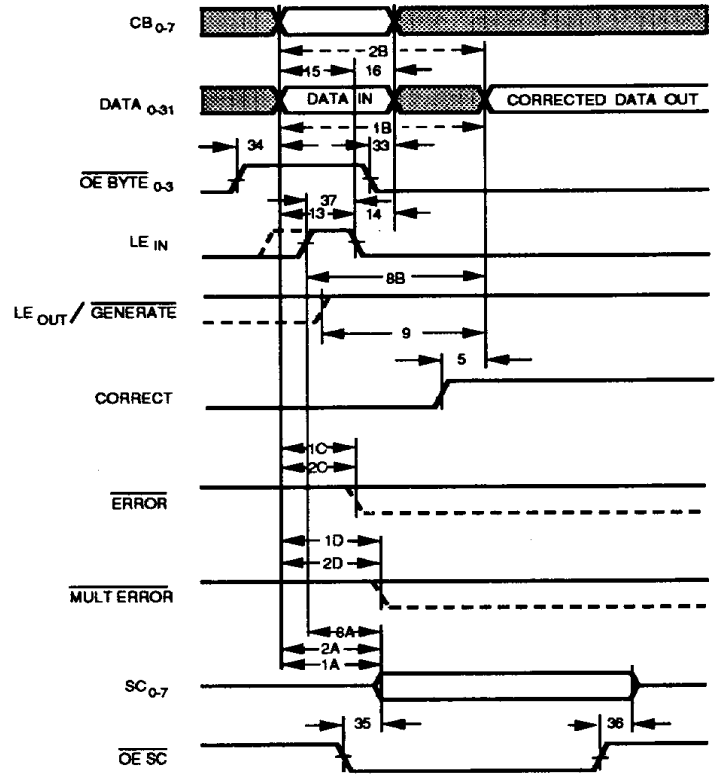
1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Changing the CODE ID inputs can cause loss of data in some of the Am29C660 internal latches. Specifically, the entire checkbit latch and bits 6 and 7 of the diagnostic latch are indeterminate after a change in CODE ID inputs. Logic simulations should store "x" (i.e., "don't care") in these bits after CODE ID change. Test programs should reload these registers before they are used.
7. Proper device grounding is critical when device testing. Multi-layer performance boards with radial decoupling between power and ground planes is recommended. Wiring unused interconnect pins to the ground plane is recommended. The ground plane must be sustained from the performance board to the device under test interface board. To minimize inductance, heavy-gauge stranded wire with twisted pairs should be used for power wiring.

TIMING DIAGRAMS



10565C-015A

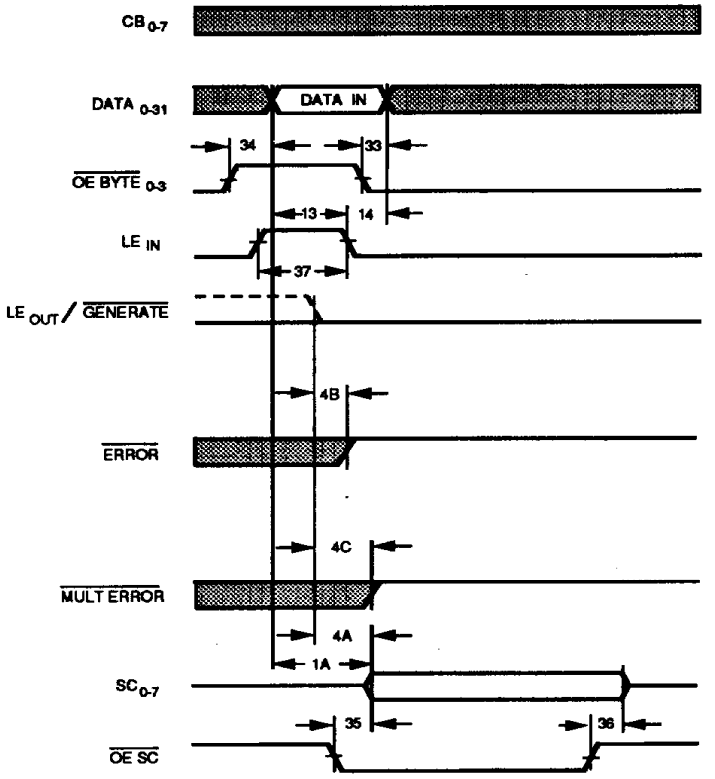
Detect Mode



10565C-016A

Correct Mode

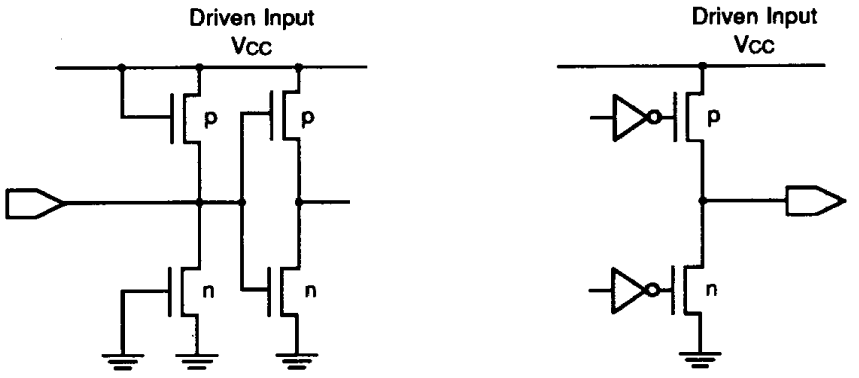
TIMING DIAGRAMS (Continued)



10565C-017A

Generated Mode

EQUIVALENT INPUT/OUTPUT CIRCUIT DIAGRAMS



10565C-018A