Am27S181/27S181A
Am27S281/27S281A

8,192-Bit (1024x8) Bipolar PROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts — enhances reliability through total system heat reduction
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Rapid recovery from power-down state provides minimum delay

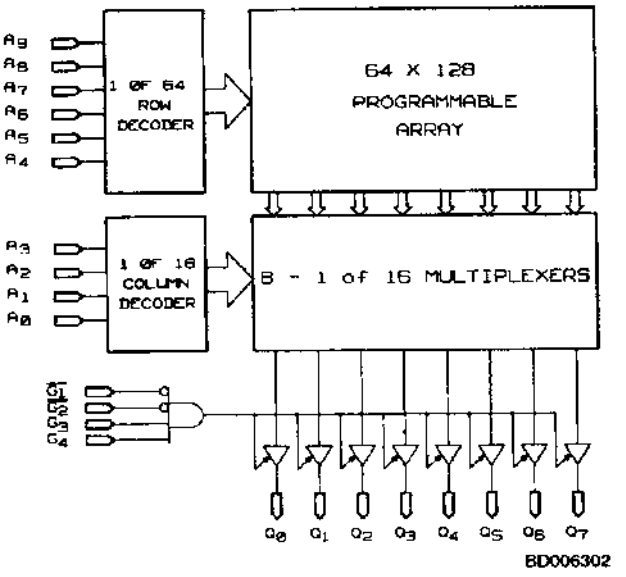
GENERAL DESCRIPTION

The Am27S181 (1024 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs which are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by both active LOW ($\overline{G_1}$ and $\overline{G_2}$) and active HIGH (G_3 and G_4) output enables.

This device is also available in a 300-mil. lateral-center DIP (Am27S281).

BLOCK DIAGRAM



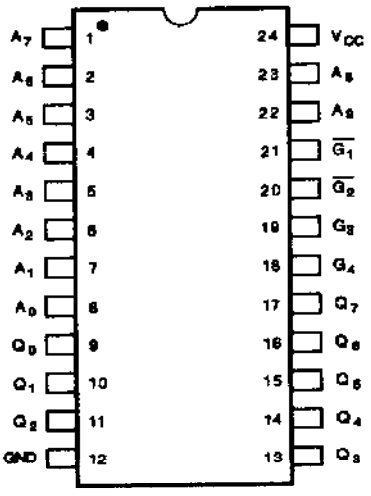
PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S181A, Am27S281A		Am27S181, Am27S281	
Address Access Time	35 ns	50 ns	60 ns	80 ns
Operating Range	C	M	C	M

Publication # 03182 Rev. D Amendment /0
Issue Date: January 1989

CONNECTION DIAGRAMS
Top View

DIP



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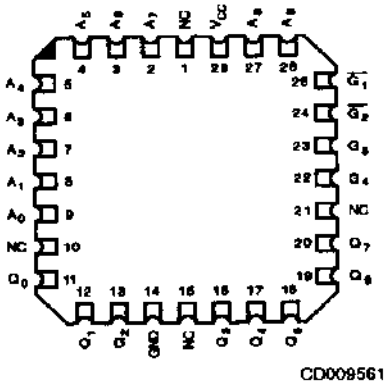
LCCs**



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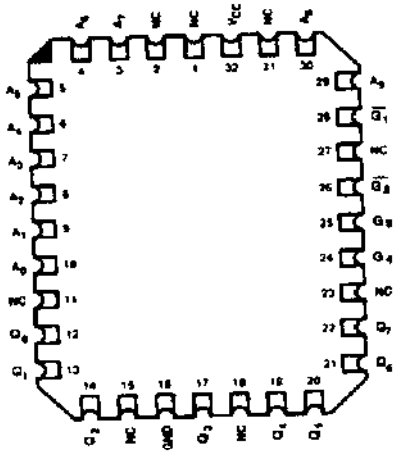

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*Also available in a 300-mil DIP and a 24-pin Flatpack. Pinout identical to those listed here for the 600-mil DIP.

**Also available in a 28-Pin Square PLCC. Pinout identical to the 28-Pin LCC.

Note: Pin 1 is marked for orientation.

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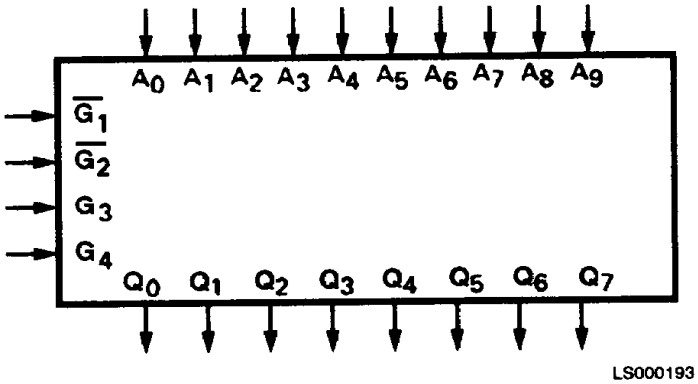
LOGIC SYMBOL



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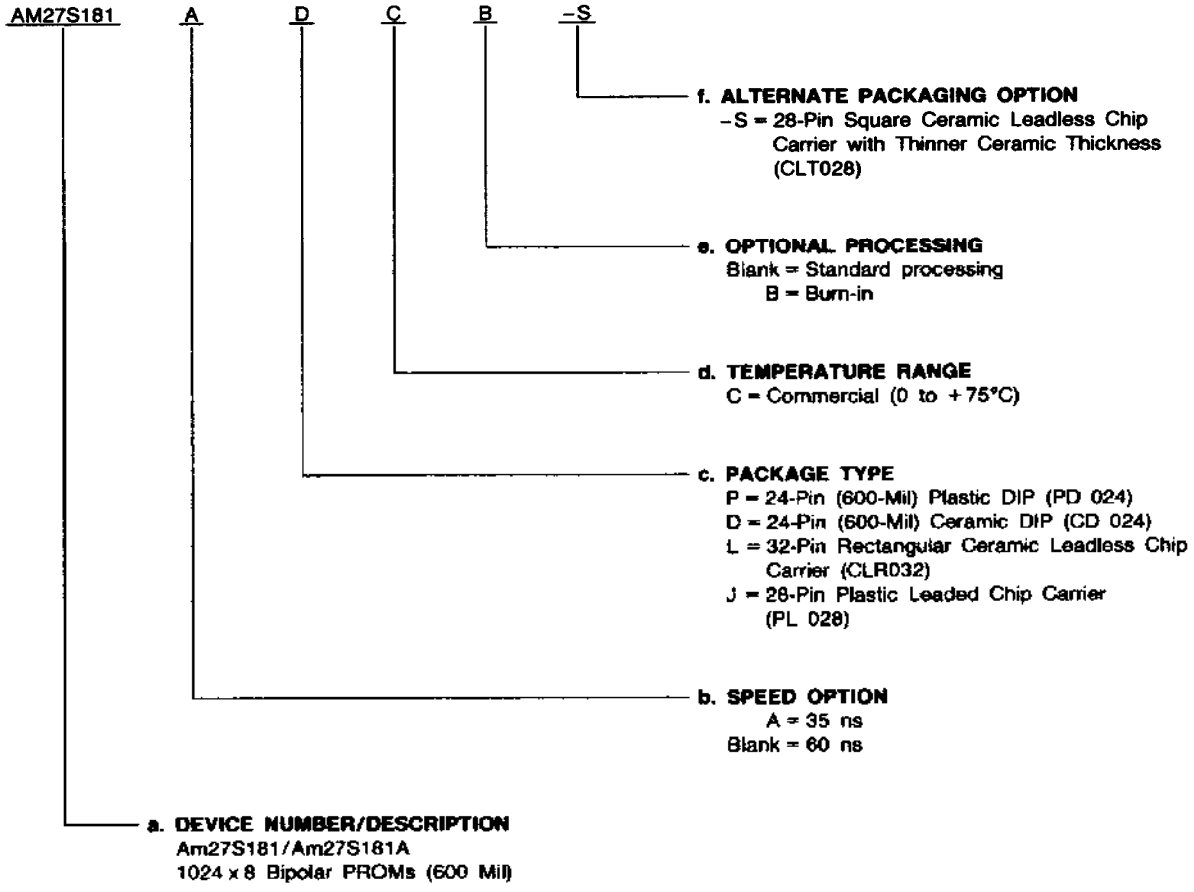
ORDERING INFORMATION

(Am27S181/181A)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing
f. Alternate Packaging Option



Valid Combinations	
AM27S181	PC, PDB, DC, DCB, LC, LCB, LC-S, LCB-S, JC, JCB
AM27S181A	

Valid Combinations

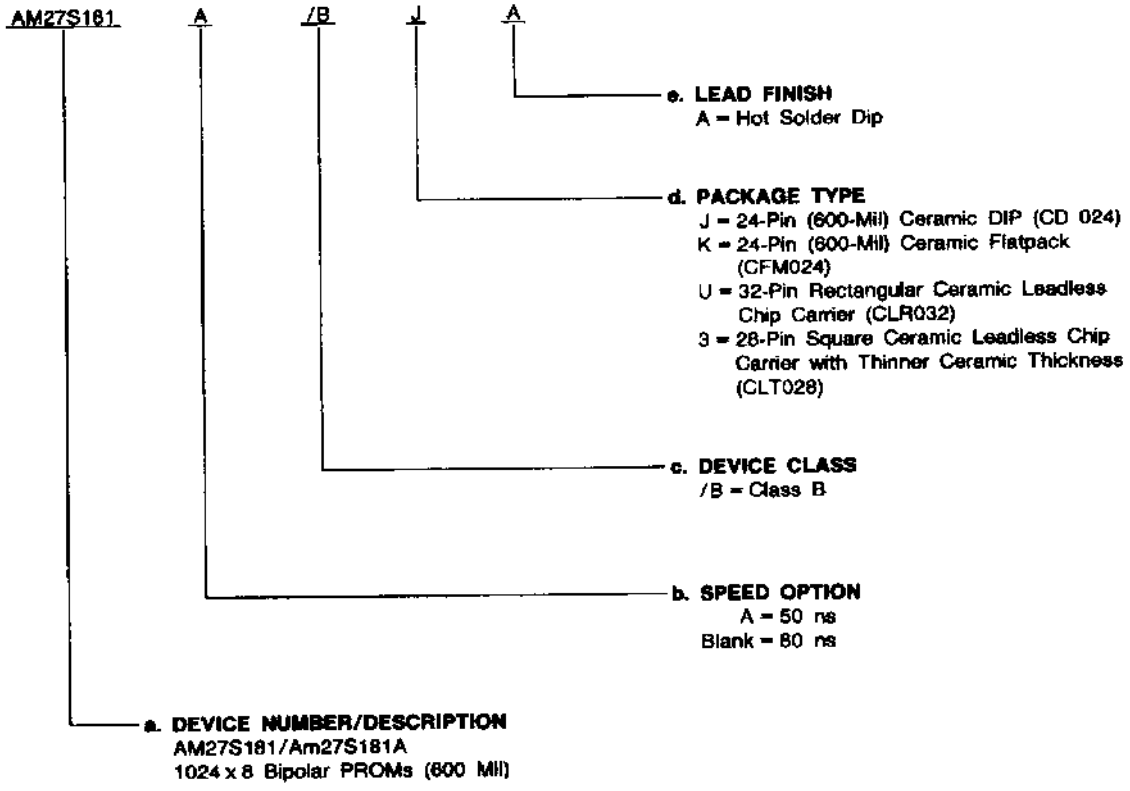
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

(Am27S181/181A)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27S181	/BJA, /BKA, /BUA, /B3A
AM27S181A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

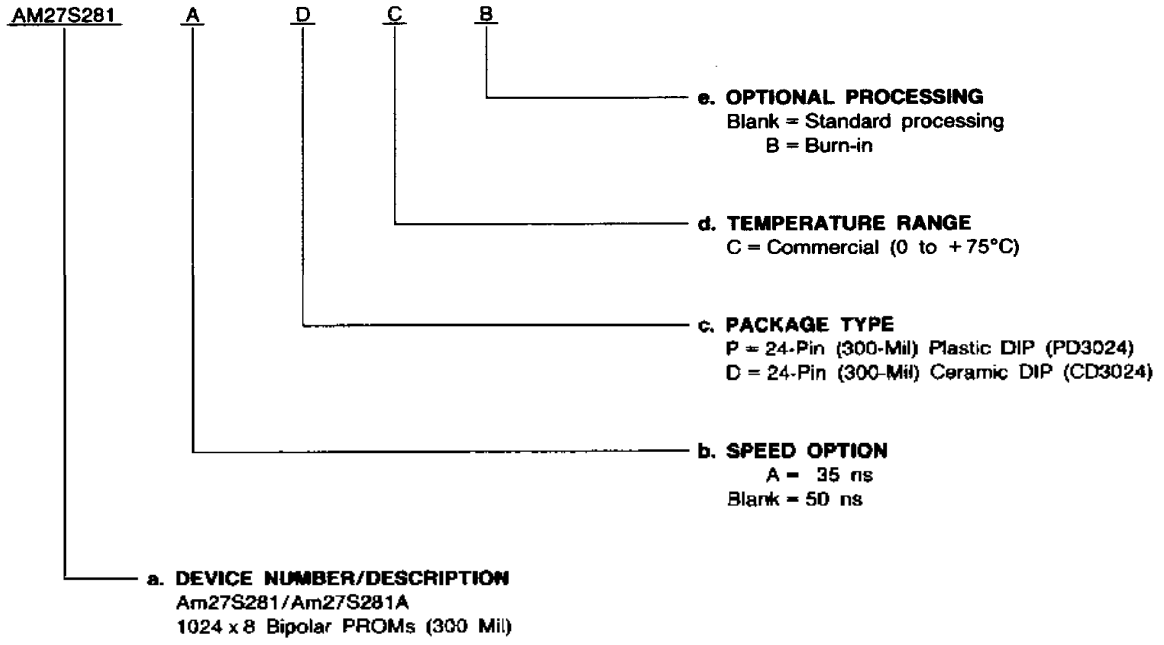
ORDERING INFORMATION

(Am27S281/281A)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27S281	PC, PCB, DC, DCB
AM27S281A	

Valid Combinations

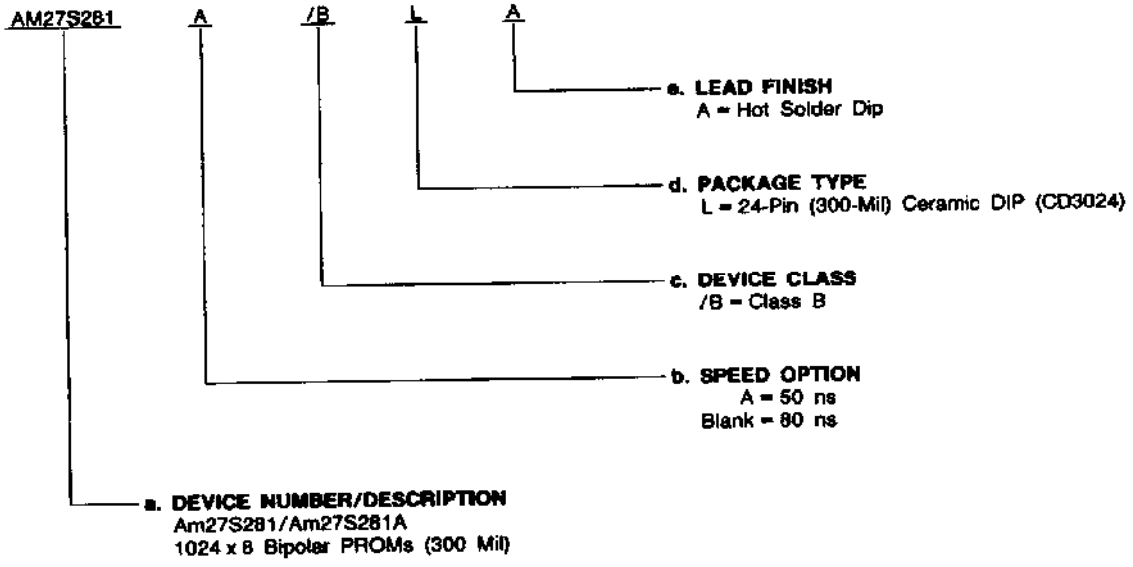
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

(Am27S281/281A)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27S281	/BLA
AM27S281A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The 10-bit field presented at the address inputs selects one of 1,048 memory locations to be read from.

$Q_0 - Q_7$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G}$, $\overline{G}_2$, G_3, G_4 Output Enable
Provides direct control of the Q output buffers. Outputs disabled force all outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G}_1 \cdot \overline{G}_2 \cdot G_3 \cdot G_4$$

$$\text{Disable} = \overline{G}_1 \cdot \overline{G}_2 \cdot G_3 \cdot G_4 = G_1 + G_2 + \overline{G}_3 + \overline{G}_4$$

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins

GND Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 V to +5.25 V

Military (M) Devices*
Case Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 1)	COM'L	−20		−90	mA
			MIL	−15		−90	
I_{CC}	Power Supply Current	All Inputs = GND				185	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	V
I_{CEX}	Output Leakage Current	V_{CC} = Max. $\overline{V_{G1}}$ = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 2) V_{CC} = 5 V, T_A = 25°C			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 2) V_{CC} = 5 V, T_A = 25°C			8.0		

Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.
2. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

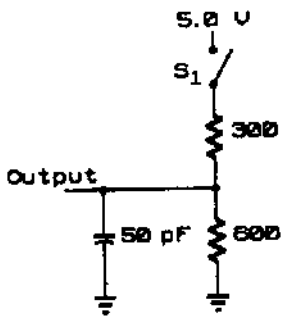
SWITCHING CHARACTERISTICS (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

No.	Parameter Symbol	Parameter Description	Version	COM'L Max.	MIL Max.	Unit
1	TAVQV	Address Valid to Output Valid Access Time	A	35	50	ns
			STD	60	80	
2	TGVQZ TEVQZ	Delay from Output Enable Valid to Output Hi-Z	A	25	30	ns
			STD	40	50	
3	TGVQV TEVQV	Delay from Output Enable Valid to Output Valid	A	25	30	ns
			STD	40	50	

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in Figure A.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in Figure B.

SWITCHING TEST CIRCUITS



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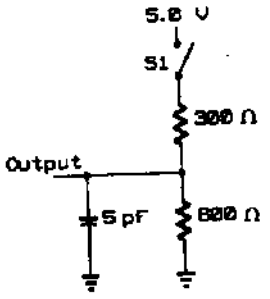
A. Output Load for all Switching tests except TGVQZ



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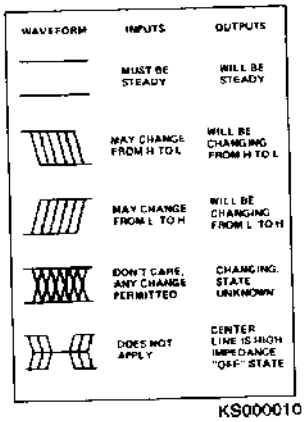
B. Output Load for TGVQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.
S_1 is closed for all other Switching tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING WAVEFORM

KEY TO SWITCHING WAVEFORMS



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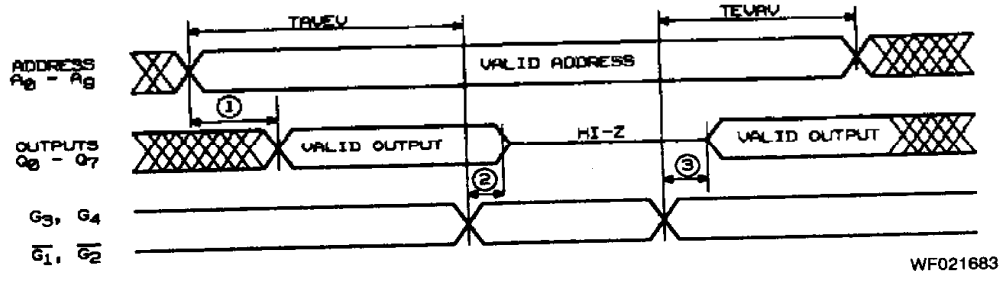

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