

# Am27S07

64-Bit Noninverting-Output Bipolar RAM



Am27S07

Advanced Micro Devices

## DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit low power Schottky RAMs
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27S07)
- Electrically tested and optically inspected die for the assemblers of hybrid products

## GENERAL DESCRIPTION

The Am27S07 is a 64-bit RAM built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and is ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select (CS) input and three-state outputs.

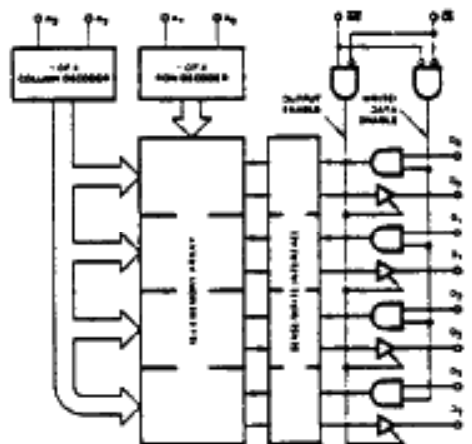
An active LOW Write line ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs  $D_0$  to  $D_3$  is written into the addressed memory word and preconditioned the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four noninverting outputs  $O_0$  to  $O_3$ .

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

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## BLOCK DIAGRAM



80000560

## MODE SELECT TABLE

Input		Data Output Status $O_{0-3}$	Mode
CS	$\overline{WE}$		
L	L	Output Disabled	Write
L	H	Selected Word	Read
H	X	Output Disabled	Deselect

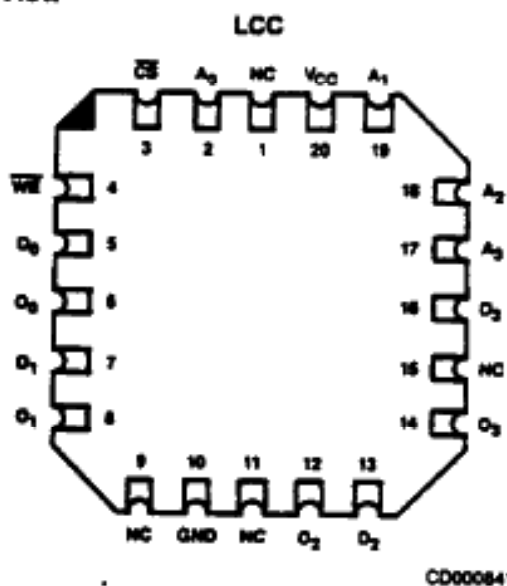
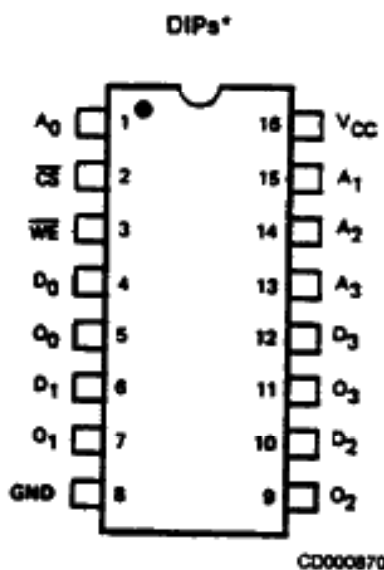
H = HIGH  
L = LOW  
X = Don't Care

## PRODUCT SELECTOR GUIDE

Access Time	25 ns	30 ns	35 ns	50 ns
$I_{CC}$	70 mA	70 mA	70 mA	70 mA
Temperature Range	C	M	C	M
Three-State Part Number	27S07A		27S07	

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Issue Date: February 1989

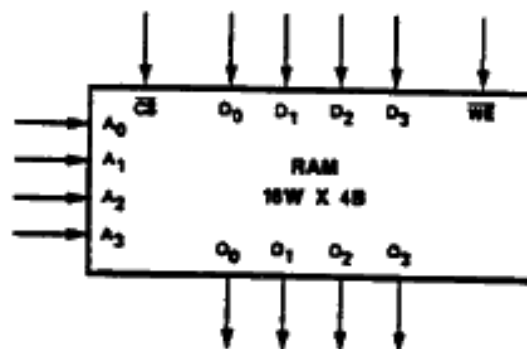
### CONNECTION DIAGRAMS Top View



\*Also available in 16-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



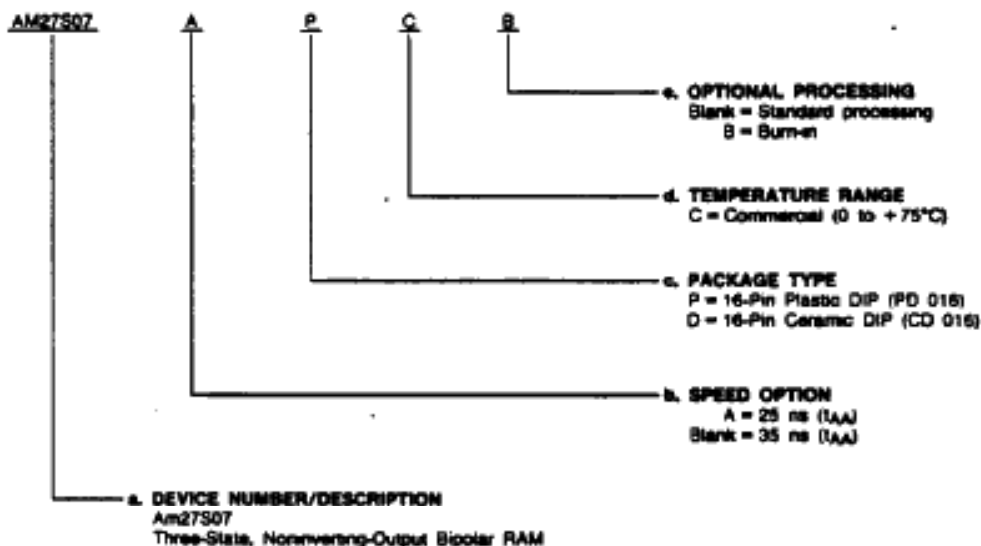
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## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM27S07	PC, PCB, DC, DCB
AM27S07A	

#### Valid Combinations

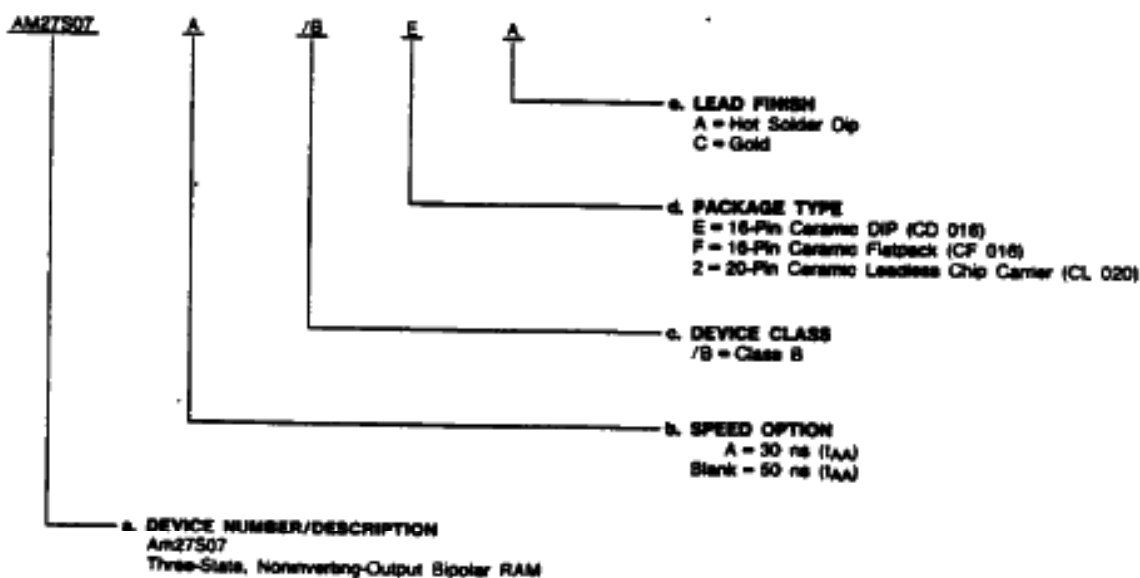
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM27S07	/BEA, /BFA,
AM27S07A	/B2A

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 9, 10, 11.

### ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs .....	-0.5 V to +V <sub>CC</sub> Max.
DC Input Voltage .....	-0.5 V to +5.5 V
Output Current into Outputs .....	20 mA
DC Input Current .....	-30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

### OPERATING RANGES

Commercial (C) Devices	
Temperature .....	0 to +75°C
Supply Voltage .....	+4.75 V to +5.25 V
Military* (M) Devices	
Temperature .....	-55 to +125°C
Supply Voltage .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

(See Note 5)

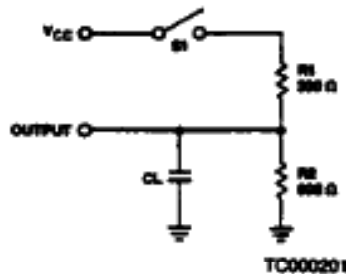
\*Military Product 100% tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

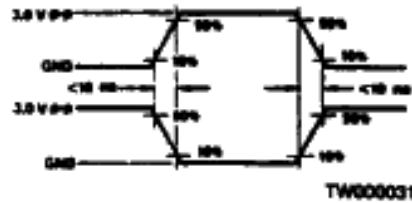
Parameter Symbol	Parameter Description	Test Conditions	Am27507			Unit
			Min.	Typ.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., V <sub>IH</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -5.2 mA COMPL	2.4	3.2	
			I <sub>OH</sub> = -2.0 mA MIL			
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., V <sub>IH</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 16 mA		350	450
			I <sub>OL</sub> = 20 mA		380	500
V <sub>IH</sub>	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)	2.0			V
V <sub>IL</sub>	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)			0.8	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IH</sub> = 0.40 V	WE, D <sub>0</sub> -D <sub>3</sub> , A <sub>0</sub> -A <sub>3</sub>		-15	-250
			CS		-30	-250
I <sub>SC</sub> (Note 3)	Output Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V		-20	-45	-90
I <sub>CC</sub>	Power Supply Current	All Inputs = GND Outputs = Open V <sub>CC</sub> = Max.			50	70
V <sub>CL</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IH</sub> = -18 mA			-0.85	-1.2
I <sub>CEX</sub>	Output Leakage Current	V <sub>CS</sub> = V <sub>IH</sub> or V <sub>WE</sub> = V <sub>IL</sub> , V <sub>OUT</sub> = 2.4 V, V <sub>CC</sub> = Max.			0	40
		V <sub>CS</sub> = V <sub>IH</sub> or V <sub>WE</sub> = V <sub>IL</sub> , V <sub>OUT</sub> = 0.4 V, V <sub>CC</sub> = Max.			-40	0

- Notes: 1. Typical limits are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.  
 2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
 4. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T<sub>A</sub> = T<sub>C</sub> = T<sub>J</sub>.  
 θ<sub>JA</sub> ≈ 50°9w (with moving air) for Ceramic DIP.  
 θ<sub>JC</sub> ≈ 10 - 17°9w for Flatpack and leadless chip carrier.

**SWITCHING TEST  
CIRCUIT**



**SWITCHING TEST  
WAVEFORM**



**KEY TO SWITCHING  
WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE 'OFF' STATE

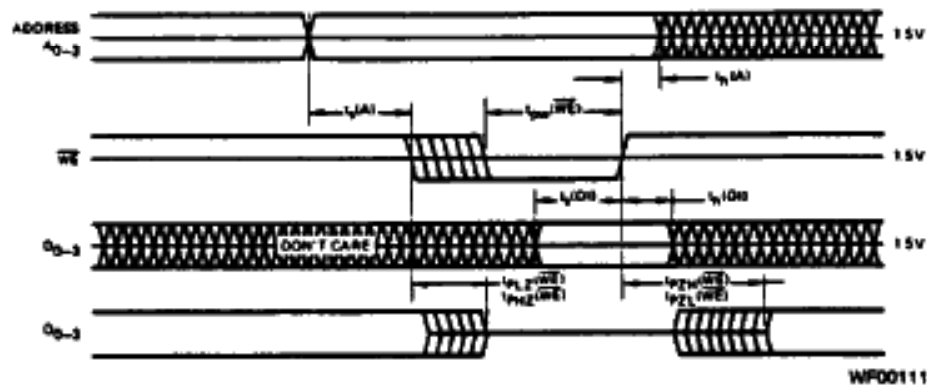
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**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am27S08A/27S07A				Am27S06/27S07				Units
			C Devices		M Devices		C Devices		M Devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	$t_{PLH}(A)$	Delay from Address to Output		25		30		35		50	ns
2	$t_{PHL}(A)$										
3	$t_{PZH}(CS)$	Delay from Chip Select (LOW) to Active Output and Correct Data		15		20		17		25	ns
4	$t_{PZL}(CS)$										
5	$t_{PZH}(WE)$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery-See Note 1)		20		25		35		40	ns
6	$t_{PZL}(WE)$										
7	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	0		0		0		0		ns
8	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		0		0		ns
9	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	20		25		25		25		ns
10	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		0		0		ns
11	$t_{pw}(WE)$	MIN Write Enable Width Pulse to Insure Write	20		25		25		25		ns
12	$t_{PHZ}(CS)$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)		15		20		17		25	ns
13	$t_{PLZ}(CS)$										
14	$t_{PLZ}(WE)$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)		20		25		25		35	ns
15	$t_{PHZ}(WE)$										

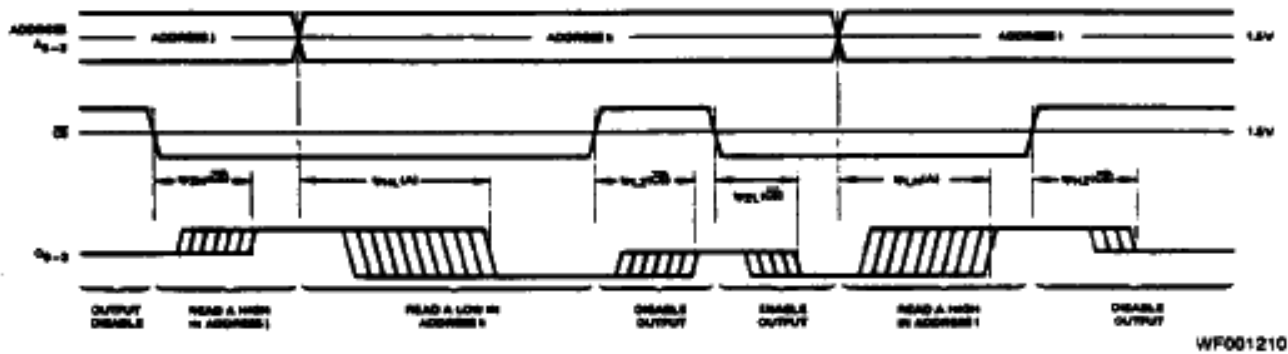
- Notes: 1. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)  
 2.  $t_{PLH}(A)$  and  $t_{PHL}(A)$  are tested with  $S_1$  closed and  $C_L = 30\text{ pF}$  with both input and output timing referenced to 1.5 V.  
 3. For 3-state output,  $t_{PZH}(WE)$  and  $t_{PZH}(CS)$  are measured with  $S_1$  open,  $C_L = 30\text{ pF}$  and with both the input and output timing referenced to 1.5 V.  $t_{PZL}(WE)$  and  $t_{PZL}(CS)$  are measured with  $S_1$  closed,  $C_L = 30\text{ pF}$  and with both the input and output timing referenced to 1.5 V.  $t_{PHZ}(WE)$  and  $t_{PHZ}(CS)$  are measured with  $S_1$  open and  $C_L < 5\text{ pF}$  and are measured between the 1.5 V level on the input to the  $V_{OH} - 500\text{ mV}$  level on the output.  $t_{PLZ}(WE)$  and  $t_{PLZ}(CS)$  are measured with  $S_1$  closed and  $C_L < 5\text{ pF}$  and are measured between the 1.5 V level on the input and the  $V_{OL} + 500\text{ mV}$  level on the output.

### SWITCHING WAVEFORMS



#### Write Mode

**Write Cycle Timing.** The cycle is initiated by an address change. After  $t_1(A)$  min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse,  $t_5(A)$  min must be allowed before the address may be changed again. The output will be floating for the Am27S07 while the write enable is LOW.



#### Read Mode

**Switching delays from address and chip select inputs to the data output.** For the Am27S07 disabled output is "OFF", represented by a single center line.