CMOS Continuous Edge Graphics RAM-DACs (CEG/DACs)

ADV7141/ADV7146/ADV7148*

2

FEATURES

Proprietary Antialiasing Function
Dejagging of Lines, Arcs, Circles, Fonts, etc.
Effective 24-Bit True Color Performance
Dynamic Palette Load (DPL) Function
Plug-in Upgrade for Standard VGA RAM-DACs
ADV478/ADV471, ADV476 (ADV®) & Inmos 171/176†
Fully PS/2†, VGA† and 8514/A† Compatible
66 MHz Pipelined Operation
Triple 8-Bit/6-Bit D/A Converters
256 × 24 (18) Color Palette RAM
On-Board Gamma-Correction
On-Board Antisparkle Circuit
RS-343A/RS-170 Compatible Outputs
External Voltage or Current Reference
Standard MPU Interface
+5 V CMOS Monolithic Construction

APPLICATIONS

High Resolution Color Graphics
True Color Graphics
Digital Typography (Smooth Fonts)
Scientific Visualization
3-D Solids Modeling
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES

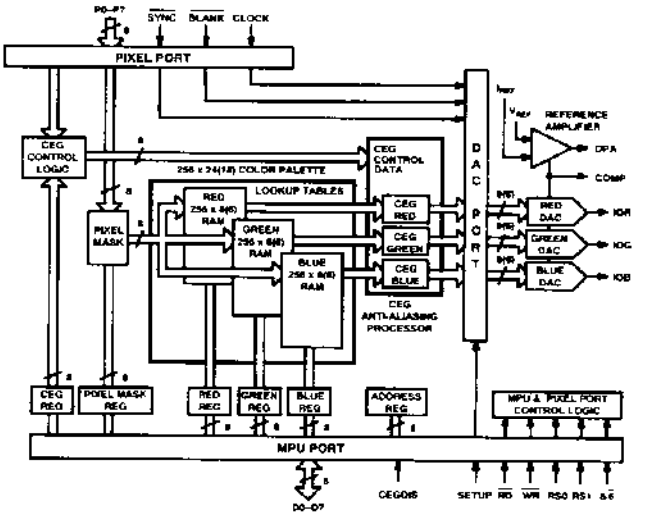
66 MHz
50 MHz
35 MHz

GENERAL DESCRIPTION

The Analog Devices' Continuous Edge Graphics† RAM-DAC (CEG†/DAC) dramatically improves image quality of standard analog color systems, by eliminating the jagged edges of computer generated images (antialiasing) and by providing an extended color palette for 3D modeling. This increased performance is achieved while at the same time maintaining full pin and functional compatibility with existing video RAM-DACs and color palettes used in VGA graphics systems.

The CEG/DAC implements a proprietary antialiasing or "dejagging" function. This is used to smooth the jagged edges associated with lines, circles and other nonrectangular objects displayed on a regular CRT screen. The part also allows for the effective display of 24-bit true color images on a standard 8-bit system, without the requirement of increased memory. More than 740,000 colors can be simultaneously displayed on an 8-bit/pixel system as against the 256 colors normally associated with 8-bit/pixel systems. This is achieved by a combination of the antialiasing function and a unique dynamic palette load

FUNCTIONAL BLOCK DIAGRAM



(DPL) feature. DPL allows for color palette writes (color alterations) during a single frame image.

The CEG/DAC combines a color lookup table (CLUT), three matched video speed computational units and associated control logic as well as three digital-to-analog converters (DACs). These all combine to significantly enhance the video image display quality of standard 8-bit/pixel graphics systems.

The ADV7148 and ADV7141 are pin and functional compatible with the ADV478 and ADV471, with the exception that the ADV7148 and the ADV7141 do not contain the overlay palette. The ADV7146 is pin and functional compatible with the ADV476 and the Inmos IMSG171/176.

CEG requires two closely connected components—the CEG/DAC chip and the software driver. Conventional antialiasing schemes are implemented entirely in software and operate on the pixel data in the graphics pipeline, resulting in a significant speed performance penalty. In contrast, the CEG software driver takes application software information and encodes the frame buffer with a sequence of data and commands for the CEG/DAC. The CEG/DAC hardware performs all of the antialiasing calculations. In this way, the visual benefits of antialiased graphics are provided with a minimal increase in software overhead.

*Protected by U.S. Patent Nos. 4,482,893 and 4,704,605.
†Inmos is a trademark of Inmos Ltd.
Personal System/2, VGA and 8514/A are trademarks of International Business Machines Corp.
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ADV is a registered trademark of Analog Devices, Inc.

ADV7141/ADV7146/ADV7148—SPECIFICATIONS (V_{AA}[1] = 5 V; SETUP = 8/$\overline{6}$ = V_{AA}; V_{REF} = 1.235 V (ADV7148/ADV7141); I_{REF} = −8.39 mA (ADV7146); R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity[3]	±1 (±1/2)	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale	
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	7	pF max	f = 1 MHz, V_{IN} = 2.4 V
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	50	μA max	
Floating-State Leakage Capacitance	7	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	20	mA max	
Output Current			
White Level Relative to Blank/Black	17.4/20.40	mA min/mA max	Typically 19.05 mA
White Level Relative to Black[4]	16.5/18.50	mA min/mA max	Typically 17.62 mA, SETUP = V_{AA}
Black Level Relative to Blank[4]	0.95	mA min	Typically 1.44 mA, SETUP = V_{AA}
(Pedestal = 7.5 IRE)	1.90	mA max	
Black Level Relative to Blank	0	μA min	Typically 5 μA, SETUP = GND
(Pedestal = 0 IRE)	50	μA max	
Blank Level[4]	6.29	mA min	Typically 7.62 mA
(Sync Enabled)	8.96	mA max	
Blank Level	0	μA min	Typically 5 μA
(Sync Disabled)	50	μA max	
Sync Level[4]	0	μA min	Typically 5 μA
	50	μA max	
LSB size	69.1	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	0/+1.5	V min/V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	
VOLTAGE REFERENCE			ADV7148 & ADV7141 Only
Voltage Reference Range	1.14/1.26	V min/V max	
Input Current, I_{VREF}	10	μA typ	
CURRENT REFERENCE			ADV7146 Only
Input Current (I_{REF}) Range	−3/−10	mA min/mA max	
Voltage at I_{REF}	V_{CC} − 3/V_{CC}	V min/max	
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	66 MHz Parts
	4.50/5.50	V min/V max	50 & 35 MHz Parts
Supply Current, I_{AA}	350	mA max	Typically 200 mA
Power Supply Rejection Ratio	0.5	%/% max	f = 1 kHz, COMP = 0.1 μF
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[5, 6]	30	dB typ	
Glitch Impulse[5, 6]	75	pV secs typ	
DAC to DAC Crosstalk[7]	−23	dB typ	

NOTES
[1] ±5% for 66 MHz parts; ±10% for 50 MHz & 35 MHz parts.
[2] Temperature range (T_{min} to T_{max}): 0 to +70°C.
[3] Tested to 8-bit linearity (tested to 6-bit linearity, ADV7146 only).
[4] ADV7141 and ADV7148 only.
[5] Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.
[6] TTL input values are 0 to 3 volts, with input rise/fall times ≈ 3 ns, measured at the 10% and 90% points. Timing reference points at 50% for inputs and outputs.
[7] DAC to DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = 5 V; SETUP = $\overline{8}/\overline{6}$ = V_{AA}; V_{REF} = 1.235 V (ADV7148/ADV7141); I_{REF} = −8.39 mA (ADV7146); R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All Specifications T_{min} to T_{max}[3] unless otherwise noted.)

Parameter	66 MHz Version	50 MHz Version	35 MHz Version	Units	Conditions/Comments
f_{max}	66	50	35	MHz	Clock Rate
t_1	10	10	15	ns min	RS0–RS1 Setup Time
t_2	10	10	15	ns min	RS0–RS1 Hold Time
t_3[4]	2	2	2	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4[4]	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5[5]	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6[5]	5	5	5	ns min	Read Data Hold Time
t_7	10	10	15	ns min	Write Data Setup Time
t_8	15	15	15	ns min	Write Data Hold Time
t_9	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_{10}	6 × t_{13}	6 × t_{13}	6 × t_{13}	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{11}	3	3	4	ns min	Pixel & Control Setup Time
t_{12}	3	3	4	ns min	Pixel & Control Hold Time
t_{13}	15	20	28	ns min	Clock Cycle Time
t_{14}	5	6	7	ns min	Clock Pulse Width High Time
t_{15}	5	6	9	ns min	Clock Pulse Width Low Time
t_{16}	30	30	30	ns max	Analog Output Delay
t_{17}	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{18}[6]	13	20	28	ns max	Analog Output Settling Time
t_{SK}	2	2	2	ns max	Analog Output Skew
t_{PD}					Pipeline Delay
Compatibility Mode	3 × t_{13}	3 × t_{13}	3 × t_{13}	ns min	
CEG Mode	6 × t_{13}	6 × t_{13}	6 × t_{13}	ns min	

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, D0–D7 output load ≤50 pF. See timing notes in Figure 2.
[2]±5% for 66 MHz parts; ±10% for 50 MHz & 35 MHz parts; t_{15} measured at V_{AA} = 5 V for 66 MHz parts.
[3]Temperature Range (T_{min} to T_{max}): 0 to +70°C.
[4]t_3 and t_4 are measured with the load circuit of Figure 3 and defined as the time required for an output to cross 0.4 V or 2.4 V.
[5]t_5 and t_6 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the times, t_5 and t_6, quoted in the timing characteristics are the true values for the device and as such are independent of external bus loading capacitances.
[6]Settling time does not include clock and data feedthrough.
Specifications subject to change without notice.

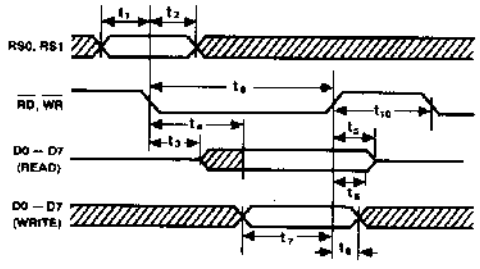


Figure 1. MPU Read/Write Timing

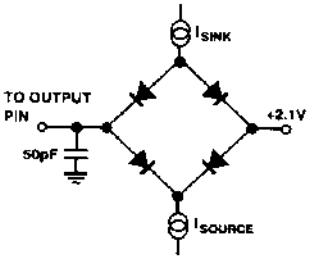


Figure 3. Load Circuit for Bus Access and Relinquish Time

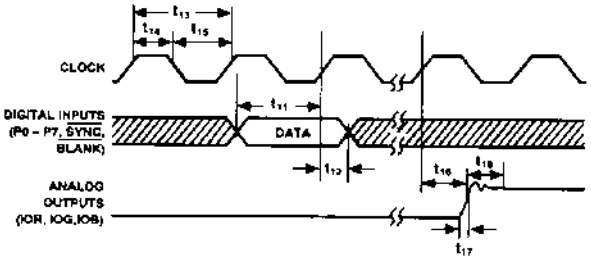


Figure 2. Video Input/Output Timing

NOTES
1. OUTPUT DELAY MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1 LSB.
3. OUTPUT RISE/FALL TIME MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
POWER SUPPLY	V_{AA}				
66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
AMBIENT OPERATING TEMPERATURE	T_A	0		+70	°C
OUTPUT LOAD	R_L		37.5		Ω
VOLTAGE REFERENCE CONFIGURATION					
Voltage Reference	V_{REF}	1.14	1.235	1.26	Volts
CURRENT REFERENCE CONFIGURATION					
I_{REF} CURRENT	I_{REF}				
STANDARD RS-343A		−3	−8.39	−10	mA
PS/2 Compatible		−3	−8.88	−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ABSOLUTE MAXIMUM RATINGS

V_{AA} to GND . . . . . −0.5 V to +7 V
Voltage on Any Digital Pin . . . . GND −0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −45°C to +125°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . . +220°C
IOR, IOG, IOB to GND[1] . . . . . 0 V to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

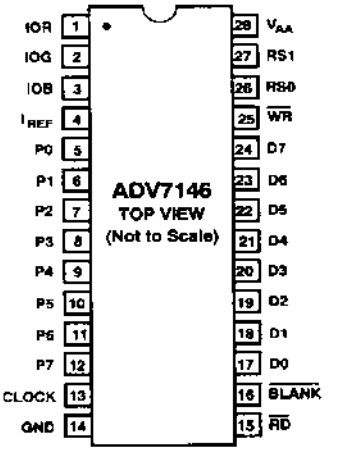
ORDERING GUIDE

Model[1]	Speed	Resolution[2]	Package Option[3, 4]
ADV7146KN66	66 MHz	6-Bit	N-28
ADV7146KN50	50 MHz	6-Bit	N-28
ADV7146KN35	35 MHz	6-Bit	N-28
ADV7141KP66	66 MHz	6-Bit	P-44A
ADV7141KP50	50 MHz	6-Bit	P-44A
ADV7141KP35	35 MHz	6-Bit	P-44A
ADV7148KP66	66 MHz	8-Bit/6-Bit	P-44A
ADV7148KP50	50 MHz	8-Bit/6-Bit	P-44A
ADV7148KP35	35 MHz	8-Bit/6-Bit	P-44A

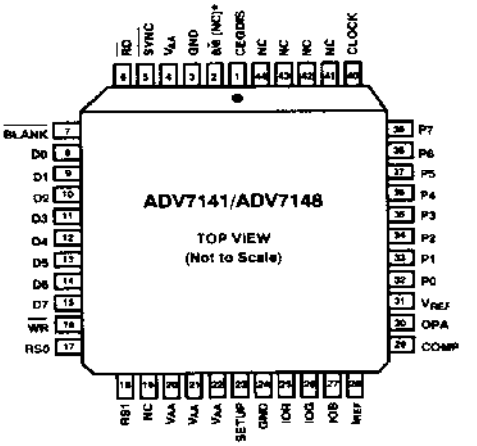
NOTES
[1]All devices are specified for 0°C to +70°C operation.
[2]Refers to "Compatibility Mode." In "CEG Mode," resolution for all options is 8 bits.
[3]28-pin DIP devices are packaged in 28-pin 0.6" plastic dual-in-line packages. 44-pin PLCC devices are packaged in 44-pin plastic leaded (J-lead) chip carriers.
[4]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

PIN CONFIGURATIONS

28-Pin DIP



44-Pin PLCC



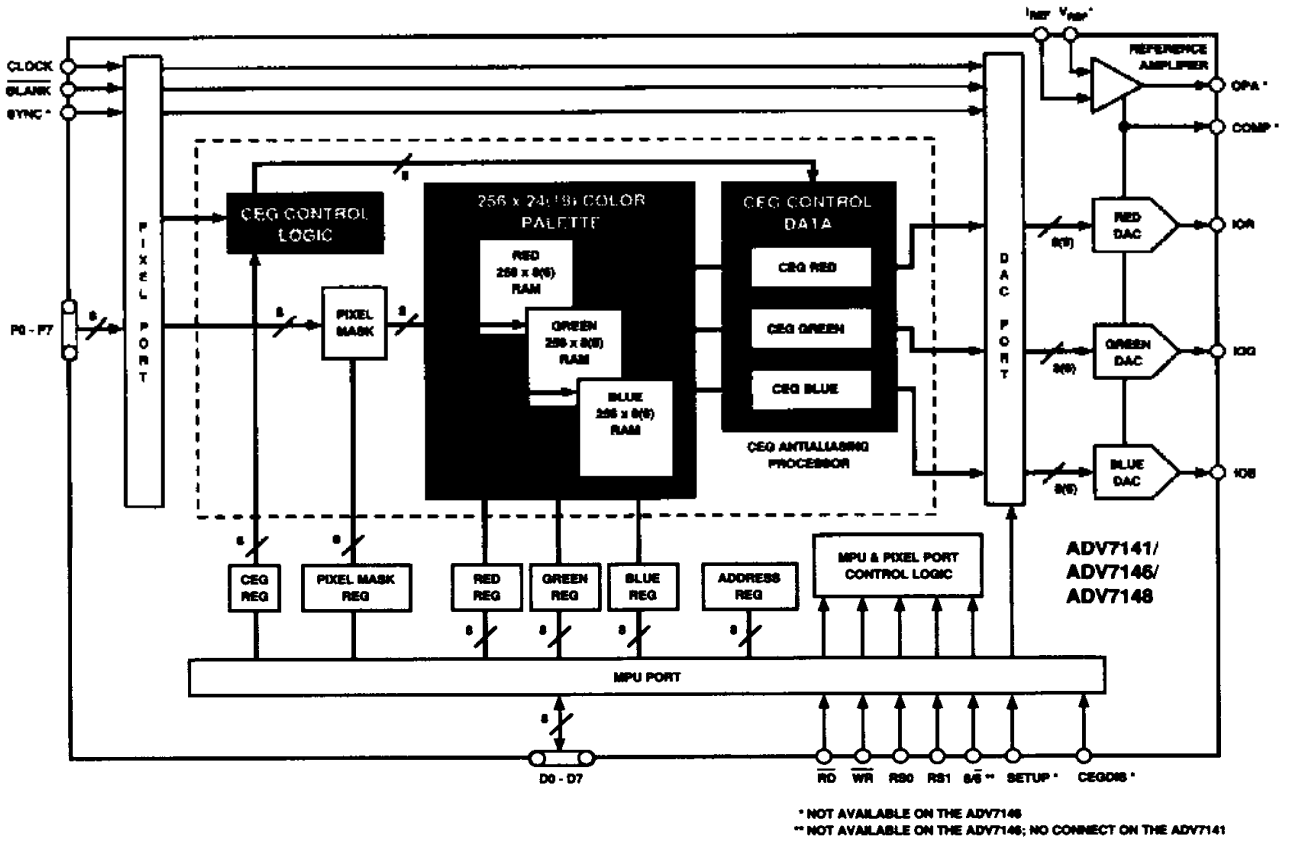
NC = NO CONNECT: THESE PINS MAY BE LEFT UNCONNECTED
* (NC) INDICATES THE ADV7141 ONLY

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{BLANK}$	Composite blank control input (TTL compatible). A Logic 0 drives the analog outputs to the blanking level. It is latched on the rising edge of CLOCK. When $\overline{BLANK}$ is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal (ADV7141/ADV7148 only).
$\overline{SYNC}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs. $\overline{SYNC}$ does not override any other control or data input, therefore it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK (ADV7141/ADV7148 only).
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, $\overline{SYNC}$, and $\overline{BLANK}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable.
I_{REF}	Current Reference input (Current Reference configuration)/Full-scale adjust control (Voltage Reference configuration). When using an external voltage reference, a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: $R_{SET}(\Omega) = K \times 1{,}000 \times V_{REF}(v)/I_{OUT}(mA)$ K is defined in the table below, along with corresponding R_{SET} values for doubly terminated 75 Ω loads. When using an external current reference, the relationship between I_{REF} and the full-scale output current on each output is: $I_{REF}(mA) = I_{OUT}(mA)/K$
COMP	Compensation pin. If an external voltage reference is used, this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1 μF ceramic capacitor must always be used to bypass this pin to V_{AA} (ADV7141/ADV7148 *only*).
V_{REF}	Voltage reference input. If an external voltage reference is used, it must supply this input with a 1.2 V (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 μF ceramic capacitor must always be used to decouple this input to V_{AA} (ADV7141/ADV7148 *only*).
OPA	Reference amplifier output. If an external voltage reference is used, this pin must be connected to COMP. When using an external current reference, this pin should be left floating (ADV7141/ADV7148 *only*).
V_{AA}	Analog power. All V_{AA} pins must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{WR}$	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{WR}$, and RS0–RS1 are latched on the falling edge of $\overline{WR}$ during MPU write operations.
$\overline{RD}$	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0–RS1 are latched on the falling edge of $\overline{RD}$ during MPU read operations.
RS0, RS1	Register select inputs (TTL compatible). RS0–RS1 specify the type of read or write operation being performed.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
$8/\overline{6}$	8-bit/6-bit select input (TTL compatible). This input specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant bit (MSB) while for 6-bit operation, D5 is the MSB. D6 and D7 are ignored during 6-bit operation. All parts operate in 8-bit format while in CEG mode. 6-Bit operation is the default VGA mode on the ADV7146 and ADV7141. The $8/\overline{6}$ bit must be set to Logical 0 on the ADV7148 to make it VGA compatible. If left unconnected, this pin remains in a low state.
CEGDIS	CEG disable (TTL compatible). Driving this pin active high disables all CEG functions. Software will detect a non-CEG device if this pin is high (ADV7141/ADV7148 only). If left unconnected, this pin remains in a low state.

Mode	Pedestal	K	R_{SET} (Ω)*
6-Bit	7.5 IRE	3.170	147
8-Bit	7.5 IRE	3.195	147
6-Bit	0 IRE	3.000	147
8-Bit	0 IRE	3.025	147

*For PS/2 applications (i.e., 0.7 V into 50 Ω with no SYNC), a 182 Ω R_{SET} resistor is recommended.



Functional Block Diagram of CEG/DAC

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

Composite Sync Signal (SYNC)
The position of the composite video signal which synchronizes the scanning process.

Composite Video Signal
The video signal with or without setup, plus the composite SYNC signal.

Gray Scale
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Setup
The difference between the reference black level and the blanking level.

Sync Level
The peak level of the composite SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

ANTIALIASING

Antialiasing is a technique used to smooth the jagged edges associated with lines, circles, and other nonrectangular objects represented on a CRT screen. Without antialiasing, each pixel (picture element) on a CRT is either "on" or "off." If the edge of a smooth shape passes through a pixel, the software is forced to approximate the edge as best it can (i.e., the pixel is "on" if more than half of the pixel is covered by the object). Even when a large number of pixels are used to represent an object, the eye quickly detects the series of "on" and "off" dots along the picture edge.

CEG achieves antialiasing by allowing the software to choose not only the discrete palette colors, but also a linear mix of those colors. For example, if only 1/3 of the pixel is covered by an object, the pixel would be displayed in the ratio of 33:67 between the object color and the background color. The eye perceives the new boundary as a completely smooth edge. The software driver defines the value of every pixel on a shape boundary, thereby dramatically increasing the perceived resolution of any computer display. By mixing colors in real time, the CEG/DAC can generate up to 800,000 simultaneously displayable colors without altering the contents of the standard 256 color look-up-table.

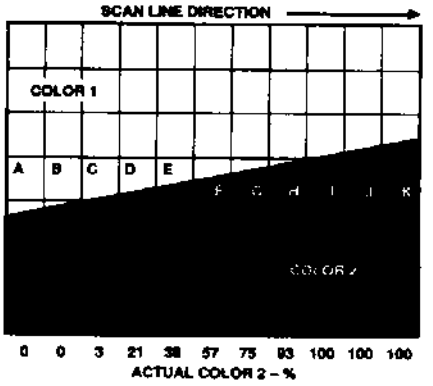


Figure 4. An Edge Crossing Scan Line

Figure 4 shows an enlargement of an object edge, with each square representing a screen pixel. An object is drawn in Color 2 on a background of Color 1—the actual colors are determined by the contents of the CLUT.

Without CEG, pixels labelled "A" through "E" will be displayed as Color 1 (Figure 5). Pixels are defined as Color 2 when more than 50% of the pixel is defined by that color, as shown in pixels "F" through "J." CEG blends colors to more closely approximate the intended color boundary as shown in Figure 6.

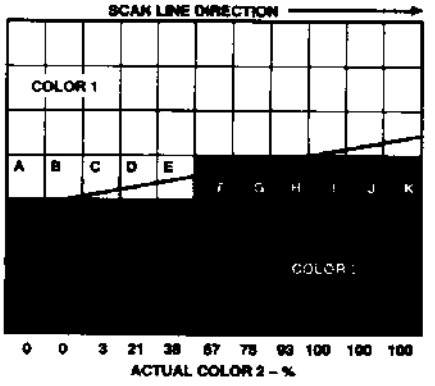


Figure 5. Traditional Pixel Coverage (Aliasing)

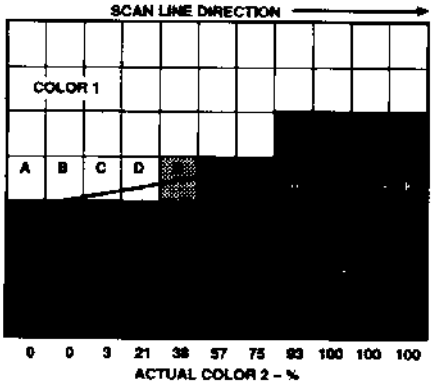


Figure 6. Dejagging or Antialiasing Using CEG

CEG FUNCTIONAL DESCRIPTION

CEG uses two data ports, a pixel port and an MPU data port. Three analog signals are produced which can directly drive the red, green, and blue inputs of a standard analog display monitor. The CEG/DAC consists of four major blocks: CEG logic, three 8-bit DACs, 256 × 24 lookup table RAM, and MPU control.

The CEG/DAC is a real-time signal processor which interprets data in the frame buffer as either colors, mix commands, or both. CEG uses a special sequence of lookup table accesses to enable and disable the CEG logic. The nonCEG mode allows full backward compatibility with current video palette products. The circuit is powered-up in nonCEG mode. CEG-aware software activates CEG modes and provides the advantages of alias-free images.

In nonCEG systems and software applications, the CEG/DAC behaves identical to normal palette DACs, providing complete physical and functional compatibility with all VGA compatible PCs. The CEG/DAC is available in packages compatible with the most popular palette DACs, including ADV471, ADV476, and ADV478 devices.

MPU Data Port

The MPU data port allows the system processor to access the color palette address register, color palette RAM and pixel mask register. Register selection is identical to the associated non-CEG, VGA compatible parts.

If the CEG device is operating in 8-bit mode, all 8 bits of the lookup table color data register are significant. In 6-bit modes, lookup table color data should be written and read back right-justified to/from D5–D0. During readback, in 6-bit modes, D6 and D7 are forced to Logic 0.

Pixel Port

Pixel information is latched into the CEG/DAC via the pixel port. For each clock cycle, the state of the P7–P0, BLANK and SYNC define the state of the DAC outputs.

Pixel port inputs are logically "AND"ed with the contents of the pixel mask register, for simple animation applications. The pixel mask register is accessed via the MPU interface. In general, the pixel mask register should be set to FFH for any of the CEG modes. See Appendix A for sample code to access the pixel mask register.

Two selectable features in CEG mode are "partial shading" and "pixel replication." Certain video controllers repeat each pixel twice in low resolution modes. In these modes, the pixel data is sampled every other CLOCK.

Systems which use only 4 bits per pixel should be connected to P3–P0, tying P7–P4 to ground. This type of system must use the "partial shading" Advanced-4 Method, which allows 8 colors (0–7) and 8 mix commands (8–15) in increments of 12%.

CEG PROGRAMMING BASICS

CEG Computation

When CEG is active, the CEG/DAC computes a real time weighted average on each of the primary colors which are read out of the palette RAM. This calculation, as represented by the generalized diagram of Figure 7, is expressed by the following equation:

$$P_{MC} = [(Color\ B \times Mix) + (Color\ A \times (31-Mix) + 16)]\ 131$$

where: P_{MC} = mixed color.

Or alternatively, it can be described by:

Mixed color = (ratio of previous color × previous color) + (ratio of new color × new color)

The mixed colors, one mixed color each for red, green and blue are then input to a gamma correction circuit. The output of this circuit drive each of the three RGB-DACs.

CEG MODES

Although there is one algorithm in the CEG/DAC, there are three ways of encoding the pixels in the frame buffer, namely, the Basic-8, Advanced-4 and Advanced-8 methods. These are described as follows:

Basic-8	16 drawing colors with 8 mixes plus explicit loading of new or old color (suitable for CAD type applications where few colors are needed).
Advanced-4	8 drawing colors with 8-mix shading (suitable for antialiasing in 4-bits/pixel systems).
Advanced-8	223 drawing colors with full 32-mix shading (suitable for 3-D solid modeling and true-color image rendition).

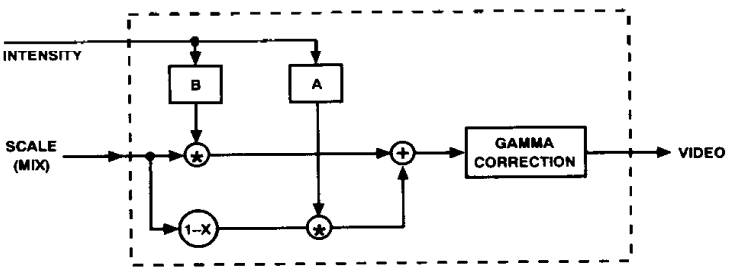


Figure 7. Block Diagram Representation of the CEG Algorithm

CIRCUIT DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the ADV7141/ADV7146/ADV7148 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM, pixel mask register and address register.

The RS0–RS1 select inputs specify whether the MPU is accessing the address register, color palette RAM, or pixel mask register, as illustrated in Table I. The 8-bit address register is used to address the color palette RAM.

Table I. Control Input Truth Table

RS1	RS0	Addressed by MPU
0	0	Address Register (RAM Write Mode)
1	1	Address Register (RAM Read Mode)
0	1	Color Palette RAM
1	0	Pixel Read Mask Register

To write color data, the MPU writes the address register with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green and blue). During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for VGA backward compatible data). This color value is then written to the location in the palette RAM pointed to by the address register. The address register then increments and points to the next palette RAM location which the MPU may modify by simply writing another sequence of red, green and blue data. See Appendix A for sample code to write to the palette.

To read color data, the MPU loads the address register with the address of the color palette RAM location to be read. The MPU performs three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0–RS1 to select the color palette RAM. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data. See Appendix A for sample code to read from the palette.

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH.

For 8-bit operation, D0 is the LSB, and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

See Compatibility section for details of 6/8-bit operation.

Table II. Address Register (ADDR) Operation

	Value	RS1	RS0	Addressed by MPU
ADDRa, b Counts Modulo 3	00			Red Value
	01			Green Value
	10			Blue Value
ADDR0–7 Counts Binary	00H–FFH	0	1	Color Palette RAM

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. As only one pixel clock cycle is required to complete the transfer, the color palette RAM may be accessed at any time with no noticeable disturbance on the display screen.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0–7), incremented following a blue read or write cycle, are accessible to the MPU, and are used to address color palette RAM locations, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing.

Frame Buffer Interface

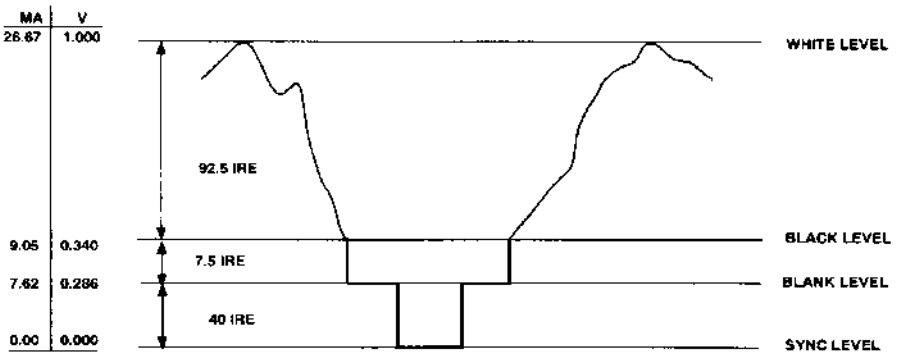
The P0–P7 inputs are used to address the color palette RAM, as shown in Table III.

Table III. Pixel Input Truth Table (Pixel Read Mask Register = FFH)

P0–P7	Addressed by Frame Buffer
00H	Color Palette RAM Location 00H
01H	Color Palette RAM Location 01H
.	.
FFH	Color Palette RAM Location FFH

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits in compatibility mode) of color information to the three D/A converters.

(See Application Note entitled "Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs" available from Analog Devices, Publication No. E1316-15-10/89.)



NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 8. ADV7141/ADV7148 RGB Video Output Waveform (SETUP = V_{AA})

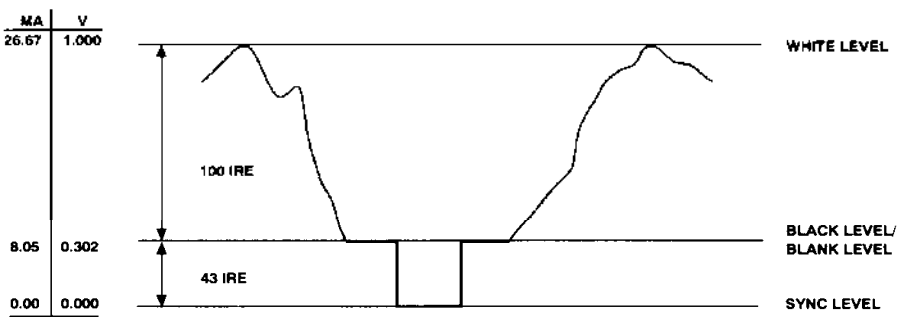
Table IV. ADV7141/ADV7148 RGB Video Output Truth Table (SETUP = V_{AA})

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	Data ÷ 9.05	1	1	Data
DATA-SYNC	Data ÷ 1.44	0	1	Data
BLACK	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK	7.62	1	0	xxH
SYNC	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67 mA.
External voltage or current reference adjusted for 26.67 mA full-scale output.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 8, 9 and 10. Tables IV, V and VI detail how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

The SETUP input, on the ADV7141 and ADV7148, is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.



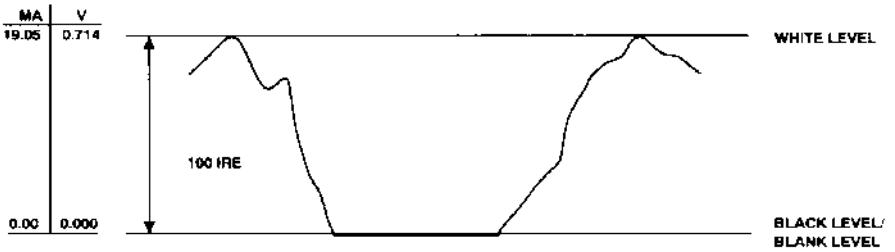
NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 9. ADV7141/ADV7148 RGB Video Output Waveform (SETUP = GND)

Table V. ADV7141/ADV7148 RGB Video Output Truth Table (SETUP = GND)

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	Data + 8.05	1	1	Data
DATA-SYNC	Data	0	1	Data
BLACK	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK	8.05	1	0	xxH
SYNC	0	0	0	xxH

NOTE
[1]Typical with full-scale IOG = 26.67 mA.
External voltage or current reference adjusted for 26.67 mA full-scale output.



NOTES
1. CONNECTED WITH A 75 Ω DOUBLY TERMINATED LOAD.
2. EXTERNAL CURRENT REFERENCE ADJUSTED FOR 19.05 mA FULL SCALE OUTPUT.
3. RS - 343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 10. ADV7146 RGB Video Output Waveform

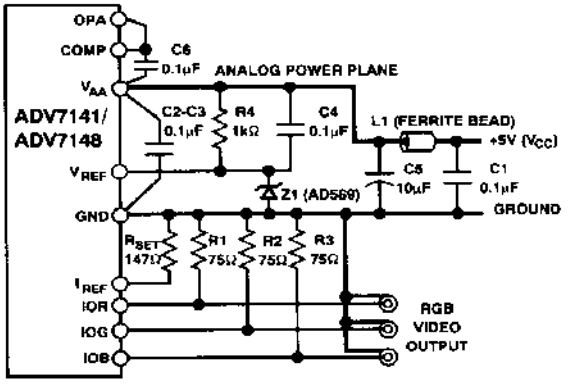
Table VI. ADV7146 RGB Video Output Truth Table

Description	I_{OUT} (mA)[1]	$\overline{BLANK}$	DAC Input Data
WHITE Level	19.05	1	FFH
VIDEO	Video	1	Data
BLACK Level	0	1	00H
BLANK Level	0	0	xxH

NOTE
[1]Typical with full-scale IOR, IOG, IOB = 19.05 mA, I_{REF} = 8.88 mA.

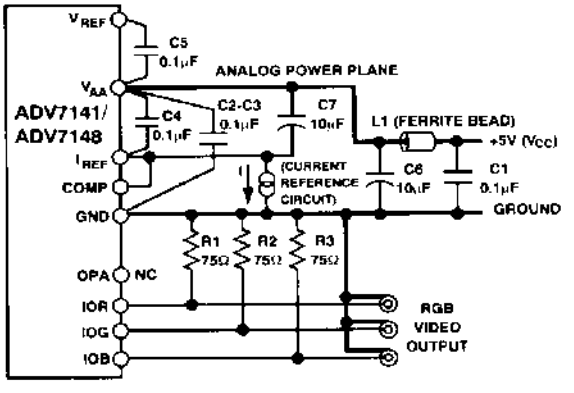
PC BOARD LAYOUT CONSIDERATIONS

The ADV7141, ADV7146 and ADV7148 CEG/DACs are optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of these parts, it is imperative that great care be given to the PC board layout. Figures 11, 12 and 13 show recommended connection diagrams for the ADV7141/ADV7148 in voltage reference and current reference modes and the ADV7146.



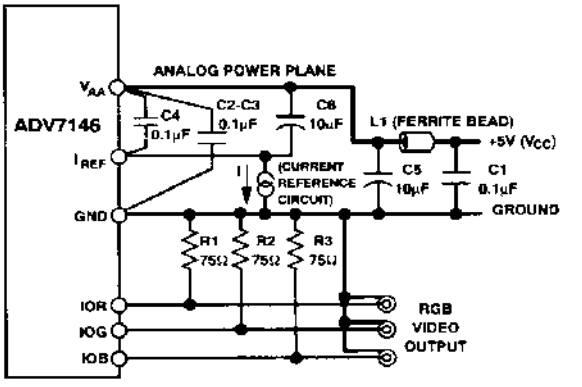
COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	
C6	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	147Ω 1% METAL FILM RESISTOR	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589JH

Figure 11. ADV7148/ADV7141 Typical Connection Diagram and Component List (Voltage Reference Configuration)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	
C6–C7	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 12. ADV7148/ADV7141 Typical Connection Diagram and Component List (Current Reference Configuration)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1µF CERAMIC CAPACITOR	
C5–C6	10µF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 274300111 OR/ MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 13. ADV7146 Typical Connection Diagram and Component List (Current Reference Configuration)

The layout should be optimized for lowest noise on the CEG/DAC power and ground lines. This is achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all the CEG/DAC ground pins, current/voltage reference circuitry, power supply bypass circuitry, the analog output traces, any output amplifiers and all the digital signal traces leading up to the CEG/DAC.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one digital circuitry. The analog power plane should encompass all the CEG/DAC power pins and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 11, 12 and 13. This bead should be located within three inches of the part.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all the CEG/DACs power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors.

Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. Each of the two groups of V_{AA} (ADV7141/AD7148) should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the CEG/DAC contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the CEG/DAC should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the CEG/DAC should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The CEG/DAC should be located as close as possible to the output connectors thus minimizing noise pick-up and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the CEG/DAC so as to minimize reflections.

Additional information on PCB design is available in an Application Note entitled "Design and Layout of a Video Graphics System for Reduced EMI." This application note is available from Analog Devices, Publication No. E1309–15–10/89.

REGISTER LEVEL PROGRAMMING OF THE CEG/DAC

Compatibility

CEG/DACs are available in several plug-in compatible replacements for most popular palette DACs including the Analog Devices ADV471, ADV476 and ADV478, the Inmos IMSG171 and IMSG176 and the Brooktree BT471 and BT478. All are compatible with standard VGA controllers.

The CEG/DAC powers-up in compatibility mode with the CEG circuitry bypassed. CEG mode is enabled with a software key sequence of reserved palette accesses. See Appendix A for a software example of setting the CEG mode.

In compatibility mode the ADV7141 and ADV7146 always use six bits for each red, green and blue palette component. The ADV7148 uses either 6 or 8 bits, depending on the setting of the 8/$\overline{6}$ pin (see Table VII below).

Table VII. CEG/DAC Bits per Color Component

	Compatibility Mode		CEG Mode
CEG/DAC	6-Bit Colors	8-Bit Colors	8-Bit Colors
ADV7141	*		*
ADV7146	*		*
ADV7148	*	*	*

In 6-bit compatibility mode the CEG/DAC shifts color data as it writes to and reads from the palette. The microprocessor writes right justified data in bits D5 to D0 into the palette. In the palette the data is stored left justified with bits D1 and D0 set to 0. During palette read operations the data is returned to the microprocessor in bits D5 to D0 with bits D7 and D6 set to 0.

The CEG mode byte, which is written to the blue palette location 223, is also shifted when it is written, but not when read.

All eight bits of the palette data register are significant when CEG is enabled. Set the CEG mode before writing CEG 8-bit palette information to avoid the shifting operations that occur when the chip is in compatibility mode.

The Encoding Methods

The Continuous Edge Graphics Level 3 specification describes in detail the two advanced encoding methods. Table VIII lists the characteristics of each CEG encoding method.

Basic-8 encoding provides 16 colors with 8 mixes, plus explicit loading of the A or B color registers. The Basic-8 method is appropriate for applications where 8-bits per pixel are available and a moderate number of colors are required, such as CAD applications.

Table VIII. CEG Encoding Methods

Encoding Method	Bits per Pixel	Palette Colors	Mixes	CEG Colors	DPL	Notes
Basic-8	8	16 + 16	8	16 × 16 × 8 = 2048		Mixes and Colors in the Same Pixel
Advanced-4	4	8	8	8 × 8 × 7/2 = 224	Yes	Mixes and Colors in Different Pixels
Advanced-8	8	223	32	223 × 222 × 32/2 = 792,096	Yes	Mixes and Colors in Different Pixels

The two Advanced methods store colors and op codes in different pixels. The Advanced-4 encoding supports 4-bits-per-pixel graphics, making it the CEG method to use in 4-bit systems such as the standard IBM VGA. Advanced-4 provides eight palette colors and eight mixes. Advanced-8 provides 223 drawing colors with full 32-mix shading. Use the Advanced-8 encoding method when there is a requirement for many colors, such as solid model rendering and computer imaging.

In the Advanced methods, an entry in the palette can also be reserved for the DPL op code. The dynamic palette further expands the number of colors available.

Basic-8 Encoding

The Basic-8 method encodes the 16 drawing colors and eight mixes into the eight bit pixel as shown in Figure 14. Table IX below shows the mix ratios that correspond to each pixel value in the mix field.

P7	P6	P5	P4	P3	P2	P1	P0
<--- MIX 0–7 --->			<------> REGISTER	<---- COLOR 0–15 ---->			

Figure 14. Pixel Encoding for Basic-8

Table IX. Basic-8 Mix Values

Mix Value	Ratio Color A	Ratio Color B
0	31/31	0/31
1	27/31	4/31
2	22/31	9/31
3	18/31	13/31
4	13/31	18/31
5	9/31	22/31
6	4/31	27/31
7	0/31	31/31

The register bit selects whether the color is placed in the A register or the B register. When the register bit is set to 0, the A register is used. When the register bit is set to 1, the B register is used. The register bit also selects which portion of the palette is accessed by the color field, because the A and B registers use different palette ranges.

The color field of the pixel data refers to the first 16 colors in the palette (Colors 0–15) when the register bit equals 0 (for the A register). When the register bit equals 1 (for the B register), the color field refers to the second 16 colors in the palette (colors 16 to 31). To find the palette location for the B register, add 16 to the color bits in P0–P3 (e.g., when the register bit = 1, color 0 refers to palette location 16). Generally, these two palette banks are loaded with the same sets of colors, but different colors can be used to increase the possible number of colors.

Advanced Encoding

In the two Advanced encoding methods, the pixel contains either a color or an op code. Mix op codes operate on the colors in the A and B registers. The companion publication, Continuous Edge Graphics Level 3, describes how the two colors are stored in the registers and how they are displayed. The Advanced-4 encoding method combines eight palette colors with eight mixes in the 4-bit pixel, providing 224 CEG colors. The 4 LSBs of the pixel value refer to either palette locations 0–7 or a mix op code as shown in Table X below.

As shown in the Figure 15, when using the Advanced-4 encoding, inputs P3–P0 contain data and inputs P7–P4 are ignored.

P7	P6	P5	P4	P3	P2	P1	P0
<— NOT CONSIDERED —>				<– COLOR OR OP CODE –>			

Figure 15. Pixel Encoding for Advanced-4

Table X. Advanced-4 Mix Values

Mix Value	Ratio Color A	Ratio Color B	Description
0			Palette Color 0
1	-	-	Palette Color 1
2	-	-	Palette Color 2
3	-	-	Palette Color 3
4	-	-	Palette Color 4
5	-	-	Palette Color 5
6	-	-	Palette Color 6
7	-	-	Palette Color 7 or DPL Op Code
8	31/31	0/31	Mix Op Code
9	27/31	4/31	Mix Op Code
10	22/31	9/31	Mix Op Code
11	18/31	13/31	Mix Op Code
12	13/31	18/31	Mix Op Code
13	9/31	22/31	Mix Op Code
14	4/31	27/31	Mix Op Code
15	0/31	31/31	Mix Op Code

Advanced-8 encoding uses 8-bit pixels and offers 223 palette colors with 32 mixes, resulting in 792,096 CEG colors. The eight bits of the pixel value refer to either a color in the palette or to an op code as shown in Table XI.

Table XI. Advanced-8 Mix Values

Mix Value	Ratio Color A	Ratio Color B	Description
0–190	-	-	Palette Colors
191	-	-	Palette Color or DPL Op Code
192	31/31	0/31	Mix Op Code
193	30/31	1/31	Mix Op Code
194	29/31	2/31	Mix Op Code
195	28/31	3/31	Mix Op Code
.	.	.	. .
.	.	.	. .
221	2/31	29/31	Mix Op Code
222	1/31	30/31	Mix Op Code
223	0/31	31/31	Mix Op Code
224–255	-	-	Palette Colors

DYNAMIC PALETTE LOADING (DPL)

The two Advanced CEG encoding methods can use dynamic palette loading, allowing the CEG/DAC to load palette colors from the bit map. With DPL enabled, an entry from the color palette is reserved as the DPL op code (7 in Advanced-4, 191 in Advanced-8). The data following this op code describes the new color to load and specifies the palette address. Note that CEG/DAC addresses are ANDed with the pixel mask register. To avoid misaddressing a DPL entry, load the mask with 255. See Mask Register for more information.

The DPL op code and data are not displayed on the screen. Instead, the color value preceding the DPL op code is repeated in place of the palette load sequence pixels. The two pixels preceding the DPL op code must be of the same kind (two colors or two mixes). For example, Color 1 Color 2 DPL is a valid sequence but Color Mix DPL is not.

DPL Examples

In the Advanced-8 encoding method, a DPL sequence requires five pixels, one for the op code, three for the new color and one for the palette address. Table XII below shows the sequence.

Table XII. DPL Op Code Sequence for Advanced-8

Pixel No.	1	2	3	4	5
Contents	DPL Op Code	New Red	New Green	New Blue	Palette Address

In 4-bits-per-pixel graphics two pixels are needed to specify one 8-bit color value. Therefore, in the Advanced-4 encoding, a DPL requires eight pixels; one for the op code, six for the new color (two each red, green and blue), and one for the palette address. Table XII shows the DPL op code sequence.

Figure 16 shows an example of a DPL op code sequence in the Advanced-4 encoding method and how the op code alters the palette and affects the display. In this example the color at palette address 2 is reassigned with the DPL. As the new color is loaded into the palette the CEG chip displays the pixel color to the left of the op code, Color 3, on the screen. After CEG loads the new color (shown as R2G2B2) at palette address 2, it is displayed whenever Color 2 is used.

Pixel Replication Compensation

Some VGA controllers repeat each pixel twice in low resolution displays (such as 320 × 200). The CEG chip, however, expects pixels in sequences and therefore it provides pixel replication compensation to undo this duplication. When pixel replication compensation is enabled, the CEG/DAC chip samples P7–P0 on every second CLOCK to ignore the repeated data (see Figure 17). Because the CEG/DAC is reversing a duplication made by the controller hardware, the compensation does not affect the graphics programmer. The bit map is written as before.

If the scan line period (video time plus $\overline{\text{BLANK}}$ time) has an even number of clock cycles, then even numbered pixels are displayed. That is, after the end of $\overline{\text{BLANK}}$, the first pixel is ignored, the second displayed, the third ignored, the fourth displayed etc. If the scan line period has an odd number of clock periods, then the first pixel after the end of $\overline{\text{BLANK}}$ is displayed, and the second is also displayed, and thereafter only even numbered pixels are displayed (the fourth, the sixth, etc.).

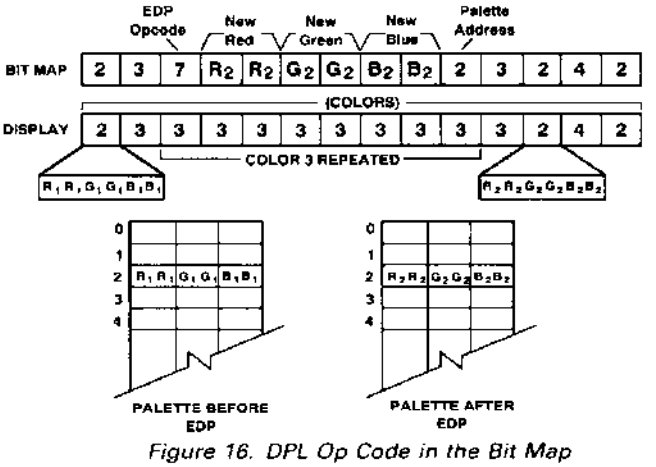


Figure 16. DPL Op Code in the Bit Map

Table XIII. DPL Op Code Sequence for Advanced-4

Pixel No.	1	2	3	4	5	6	7	8
Contents	DPL Op code	New Red	New Red	New Green	New Green	New Blue	New Blue	Palette Address
Color bits		R7–R4	R3–R0	G7–G4	G3–G0	B7–B4	B3–B0	

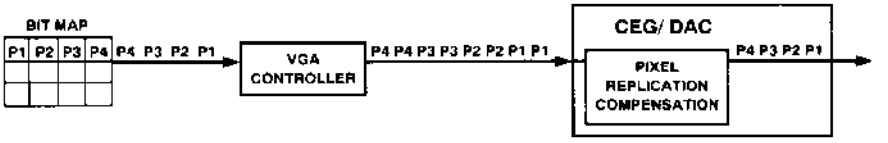


Figure 17. Pixel Replication Compensation

CEG/DAC MODES

The CEG/DAC supports a number of modes. A mode is a combination of attributes. The possible attributes are:

- CEG Encoding (Basic-8 or Advanced-4 or Advanced-8)
- Dynamic Palette Loading (DPL)
- Pixel Replication Compensation

The mode is selected under software control by a key sequence followed by a mode byte.

Enabling CEG

The CEG/DAC employs an unused sequence of palette accesses to enable the CEG logic. This long sequence was specially designed to prevent accidental mode changes. To enable the CEG/DAC the software must perform the following steps:

1. Write a palette read address (222).
2. Write three specific bytes of palette RAM data.
3. Repeat Steps 1 and 2 twice more.

There are eight bytes of special palette RAM data followed by the CEG mode byte. The mode byte determines the CEG functionality. Table XIV shows the special palette RAM data and the mode byte. The CEG/DAC Modes table shows the mode byte values. Appendix A contains sample software routines to set the VGA CEG/DAC mode.

Table XIV. CEG Key Sequence (Decimal Values)

Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
67	69	71	69	68	83	85	78	Mode

The key sequence must be written exactly as shown and cannot be interrupted by any other palette accesses. The entire key sequence must be reentered to change CEG modes. If the key sequence is wrong or the CEGDIS pin is high, the chip remains in compatibility mode. After the mode is set it can be read from palette location 223 blue. Note that, as with other palette data, the mode byte is shifted as it is written to the palette (see Compatibility section).

Table XV shows the CEG/DAC modes. Unpredictable results can occur if a mode not listed in the table is used.

Table XV. CEG/DAC Modes

Mode	CEG Encoding Method	DPL	Pixel Replication
5	Basic-8		
6	Basic-8		*
9	Advanced-4		
10	Advanced-4		*
11	Advanced-4	*	
13	Advanced-8		
14	Advanced-8		*
15	Advanced-8	*	

Writing palette data to location 223 immediately disables CEG operations and returns the device to full power-up compatibility mode (there are no side effects to this and no need to clear any registers). Appendix A contains sample software that clears the CEG/DAC mode and returns the hardware to its initial power-up compatibility mode (in a VGA system).

Gamma Correction

The CEG/DAC automatically applies full gamma correction in all CEG modes. Gamma correction is required to compensate for the nonlinear relationship between the CEG/DAC outputs and the CRT display. To avoid any incompatibility, gamma correction is disabled in compatibility mode. The CEG/DAC uses a gamma value of 2.3 to perform this correction.

Identifying a CEG/DAC

Software determines whether a CEG/DAC is present by reading the mask register. Whenever a CEG mode set is selected, the four most significant bits of the mask register become write only. When read, these four MSBs do not relay the contents of the mask, but rather, give information about the CEG hardware installed.

Mask register Bit D7 is reserved and Bits D6–D4 read back the revision code of the CEG/DAC chip. The revision number always contains at least one "0" to allow software to distinguish CEG/DAC chips from other DACs. An ordinary palette DAC returns the full eight bits of the mask register.

In other words, by enabling CEG, loading the mask register with 255 and then reading the mask register, the software can determine whether or not the hardware uses a CEG/DAC. Devices that return the value loaded (those which read back 255) do not have CEG. Those that return a different value use a CEG/DAC. Appendix A contains sample software which determines the version by inspecting the mask register.

APPENDIX A. CEG SAMPLE CODE

The following code samples are available on diskette

Setting the CEG/DAC Mode

```
SET_CEG_MODE:   ; Set the CEG/DAC mode by entering a key sequence.
                ; 8086/286/386/486 assembler for a CEG/DAC in a VGA
                ; Desired MODE is passed in AL
        PUSH    DX              ; Save DX
        PUSH AX                 ; Save MODE for later
RVRT    equ     00001000b       ; Vertical retrace bit
        MOV     DX,     03DAH   ; Set to Video status port
SYNC0:  IN      AL,     DX      ; Get from Status Port
        TEST    AL,     RVRT    ; Are we in vertical retrace ?
        JNZ     SYNC0           ; Yes, wait until we aren't
SYNC1:  IN      AL,     DX      ; Get from status port
        TEST    AL,     RVRT    ; Are we in vertical retrace ?
        JZ      SYNC1           ; No, loop until we are
ENTER_KEY:
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write data address in DX
        MOV     AL,     67      ; Write key byte 1
        OUT     DX,     AL
        MOV     AL,     69      ; Write key byte 2
        OUT     DX,     AL
        MOV     AL,     71      ; Write key byte 3
        OUT     DX,     AL
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write data address in DX
        MOV     AL,     69      ; Write key byte 4
        OUT     DX,     AL
        MOV     AL,     68      ; Write key byte 5
        OUT     DX,     AL
        MOV     AL,     83      ; Write key byte 6
        OUT     DX,     AL
        MOV     DX,     03C7H   ; Set up DAC for read from 222
        MOV     AL,     222
        OUT     DX,     AL
        MOV     DX,     03C9H   ; Put write address in DX
        MOV     AL,     85      ; Write key byte 7
        OUT     DX,     AL
        MOV     AL,     78      ; Write key byte 8
        OUT     DX,     AL
        POP     AX              ; Retrieve desired MODE
        OUT     DX,     AL      ; Write the MODE
        POP     DX              ; Restore DX
        RET                     ; return from subroutine
```

Clearing the CEG/DAC Mode

```
CLEAR_CEG_MODE:
                                        ; Clear CEG mode and return to
                                        ; power-up compatibility mode

; 8086/286/386/486 assembler code to clear the CEG/DAC mode and
; return the hardware to its initial power-up Compatibility mode
; (in a VGA system)

;           To clear CEG mode:
;           1) Wait for the Beginning of a vertical retrace
;           2) Write to palette location 223d

            PUSH  DX                    ; Save DX
            PUSH  AX                    ; Save MODE for later

RVRT        equ   00001000b             ; Vertical retrace bit

; Trigger during vertical retrace so DPLs won't interrupt reset

            MOV   DX,     03DAH         ; Set to Video status port

SYNC0:      IN    AL,     DX            ; Get from Status Port
            TEST  AL,     RVRT          ; Are we in vertical retrace ?
            JNZ   SYNC0                 ; Yes, wait until we aren't

SYNC1:      IN    AL,     DX            ; Get from status port
            TEST  AL,     RVRT          ; Are we in vertical retrace ?
            JZ    SYNC1                 ; No, loop until we are
                                        ; Safe to write
            MOV   DX,     03C8H
            MOV   AL,     223           ; Set write address
            OUT   DX,     AL

            MOV   DX,     03C9H
            MOV   AL,     0             ; Clear CEG mode
            OUT   DX,     AL            ; Write the byte

            POP   AX                    ; Restore AX
            POP   DX                    ; Restore DX
            RET
```

Determining the CEG/DAC Version (Reading the Mask Register)

```
GET_VERSION:                            ; Identify CEG version number

; 8086\286\386\486 assembler code for the VGA sequence to
; determine the version by inspecting the mask register

            MOV   AL,     013DH         ; Any legal mode will do
            CALL  SET_CEG_MODE          ; Set the mode

            MOV   DX,     03C6H         ; Set DX to mask reg. address
            MOV   AL,     255           ; Write mask bits to all ones
            OUT   DX,     AL
            IN    AL,     DX            ; Read contents of mask reg
            SHR   AL,     1             ; Shift result to lowest bits
            SHR   AL,     1
            SHR   AL,     1
            SHR   AL,     1
            AND   AX,     7             ; Mask to keep only three bits

; The revision code is now in the low nibble of AL
; Valid revision codes are 0-6
; Revision code 7 indicates Non CEG compatible device
; This specification refers to chip revision 00
```

Writing the Palette

```
; 8086/286/386/486 assembler code for the VGA sequence to
; write to the palette
WRITE_PAL:                                  ; Write to Palette locations
                MOV   DX,   03C8h           ; Set up CEG/DAC for Write
                MOV   AL,   0               ; Will write location zero
                OUT   DX,   AL              ;
                MOV   DX,   03C9h           ; Put data address into DX
                OUT   DX,   AL              ; Write Red Byte          Location 0
                OUT   DX,   AL              ; Write Green Byte        Location 0
                OUT   DX,   AL              ; Write Blue Byte         Location 0
; Palette Address will Auto-increment – keep writing
                OUT   DX,   AL              ; Write Red Byte          Location 1
                OUT   DX,   AL              ; Write Green Byte        Location 1
                OUT   DX,   AL              ; Write Blue Byte         Location 1
```

Reading the Palette

```
; 8086/286/386/486 assembler code for the VGA sequence to
; read from the palette
READ_PAL:                                   ; Read From Palette locations
                MOV   DX,   03C7h           ; Set up CEG/DAC for read
                MOV   AL,   50              ; Will read from location 50
                OUT   DX,   AL              ;
                MOV   DX,   03C9h           ; Put Data address into DX
                IN    AL,   DX              ; Read Red Byte into AL
                IN    AH,   DX              ; Read Green Byte into AH
                IN    BL,   DX              ; Read Blue Byte into BL
; Palette Address will Auto-increment – keep reading
                IN    AL,   DX              ; Read Red Byte           Location 51
                IN    AH,   DX              ; Read Green Byte         Location 51
                IN    BL,   DX              ; Read Blue Byte          Location 51
```

Accessing the Pixel Mask Register

```
; 8086/286/386/486 assembler code for the VGA sequence to access the
; Pixel Mask Register
ACCESS_REG
                MOV   DX,   3C6h            ; Pixel Mask Register Port Address
                MOV   AL,   255             ; Write all ones to register
                OUT   DX,   AL              ;
                IN    DX,   AL              ; Read back contents of register
```